A Generalized Predictive Controlled T-type Power Inverter with a deterministic dc-link capacitor voltage balancing approach

A PROJECT REPORT

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ABSTRACT

The thesis consists of implementing a Generalized Predictive Control (GPC) strategy for controlling the output voltage of the T-type converter with output LC filter, whose control signals are modulated by a fast three-dimensional Space Vector Modulation (SVM). The GPC strategy used for the T-type converter involves developing a system of dynamic equations from the output LC filter and load, which is transformed to a Controlled Auto-Regressive and Moving-Average (CARIMA) model in order to obtain a sequence of control signals, so that a cost function is optimized and the reference is tracked.

The core of the thesis addresses the main problem of dc-link capacitor balancing. This is done by modeling the converter and deploying a mathematical analysis of the capacitor voltage difference dynamics, by singular perturbation approach. This analysis results in an explicit sinusoidal disturbance. Now, classical control theory is applied by using a Luenberger Observer (LO) in order to estimate the disturbance and encounter it, thereby keeping the dc-link capacitor voltage balanced in the due flow of the modulation and output voltage control. By this method, the output voltage across the filter capacitor is controlled, the dc-link capacitor voltage is balanced and the low-frequency voltage ripples present in the dc-link of the T-type converter are reduced to an acceptable level.

LIST OF TABLES

LIST OF FIGURES

imbalance condition

LIST OF ABBREVATIONS

AC　　　　– **A**lternating **C**urrent

DC　　　　– **D**irect **C**urrent

SVM　　　– **S**pace **V**ector **M**odulation

2D SVM　– **T**wo **D**imensional **S**pace **V**ector **M**odulation

3D SVM　– **T**hree **D**imensional **S**pace **V**ector **M**odulation

FFSVM　– **F**eed **F**orward **S**pace **V**ector **M**odulation

PWM　　– **P**ulse **W**idth **M**odulation

IGBT　　– **I**nsulated **G**ate **B**ipolar **T**ransistor

RB IGBT　– **R**everse **B**locking **I**nsulated **G**ate **B**ipolar **T**ransistor

MOS　　– **M**etal **O**xide **S**emiconductor

MOSFET　– **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor

CMOS　　– **C**omplementary **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor

SMPS　　– **S**witched **M**ode **P**ower **S**upplies

LED　　　– **L**ight **E**mitting **D**iode

UPS　　　– **U**ninterruptible **P**ower **S**upplies

NPP　　　– **N**eutral **P**oint **P**iloted

NPC　　　– **N**eutral **P**oint **C**lamped

MPC　　　– **M**odel **P**redictive **C**ontrol

GPC　　　– **G**eneralized **P**redictive **C**ontrol

VSI　　　– **V**oltage **S**ource **I**nverter

VSC　　　– **V**oltage **S**ource **C**onverter

EMC – **E**lectro-**M**agnetic **C**ompatibility

DCC – **D**iode **C**lamped **C**onverter

SDCS – **S**eparate **DC S**ource

CHB – **C**ascaded **H**-**B**ridge

FCC – **F**lying **C**apacitor **C**onverter

PS PWM – **P**hase **S**hifted **P**ulse **W**idth **M**odulation

LS PWM – **L**evel **S**hifted **P**ulse **W**idth **M**odulation

SV PWM – **S**pace **V**ector **P**ulse **W**idth **M**odulation

ANPC – **A**ctive **N**eutral **P**oint **C**lamped

SHE – **S**elective **H**armonic **E**limination

SHM – **S**elective **H**armonic **M**itigation

THD – **T**otal **H**armonic **D**istortion

RMS – **R**oot **M**ean **S**quare

GA – **G**enetic **A**lgorithm

CARIMA – **C**ontrolled **A**uto-**R**egressive and **M**oving-**A**verage

LO – **L**uenberger **O**bserver

KCL – **K**irchhoff's **C**urrent **L**aw

KVL – **K**irchhoff's **V**oltage **L**aw

PI – **P**roportional **I**ntegral

DSP – **D**igital **S**ignal **P**rocessor/**P**rocessing

GPIO – **G**eneral **P**urpose **I**nput **O**utput

EPWM – **E**nhanced **P**ulse **W**idth **M**odulation

FFD   – **F**irst **F**ault Detection

PCB   – **P**rinted **C**ircuit **B**oard

UVLO   – **U**nder **V**oltage **L**ock **O**ut

CRO   – **C**athode **R**ay **O**scilloscope

ICs   – **I**ntegrated **C**ircuits

LPF   – **L**ow **P**ass **F**ilter

CHAPTER 1

INTRODUCTION

Multilevel converters have become a common solution in applications like integration of renewable energies, electric drives, Uninterruptible Power Supplies (UPS), energy storage systems, etc. [1], [2]. The main reason for using these mature technologies are increased output voltage and reduced harmonic content. Although several multilevel converter topologies exists like Diode Clamped Converter (DCC), Cascaded H-bridge (CHB) converter and Flying Capacitor Converter (FCC), which are mainly used in many high power applications [3], [4], there is a demand of converters which are particularly suitable for low and medium power applications [5].

The Neutral Point Piloted (NPP) [6] converters, also known as T-type power converters are good choice of option, when used in low and medium power Photovoltaic (PV) systems. Other applications of these converters include compact electric drives, small unmanned drones, etc. The T-type power converter has the advantage of using an active bidirectional switch at the dc-link midpoint, thereby making the bridge-leg simpler and with lower number of power devices when compared to conventional Diode Clamped Converters (DCC). Additionally, the efficiency of T-type power converters is excellent for medium switching frequencies from 6 to 20 kHz, which makes it suitable for low power applications.

In our project, the NPP power converter is used as a Voltage Source Inverter (VSI) with output LC filter. The NPP inverter system mainly comprises the semiconductor switches, dc link capacitors, DC sources, filter & load, a modulator and controller. The controllers may be one or many and they mainly serve the purpose of controlling the output voltage and balancing the dc link capacitor voltages.

Model Predictive Control (MPC) is a family of control techniques, which gives fruitful results when applied to power converters [7], [8]. The MPC explicitly uses the system model to predict the output at future time instants, called horizons. A control sequence is calculated at every sampling time in order to minimize an objective function, so that the prediction horizon is displaced towards future. Generalized Predictive Control (GPC) [9] is one of the family members of MPC and it is an indirect control strategy, which tracks the reference in order to control the output voltage, thereby resulting in an effective voltage reference for the modulator.

In order to generate the firing pulses for the semiconductor switches the modulation algorithm is used. The two main modulation techniques are Pulse Width Modulation (PWM) [10] and Space Vector Modulation (SVM). In our project SVM is used. A two dimensional SVM [11] is used when the control strategy is defined in the $\alpha\beta$ stationary frame; where as either a three dimensional SVM [12] or a three dimensional feedforward SVM [13] is used when the control strategy is defined in the $\alpha\beta\gamma$ frame.

The dc link capacitor voltage balancing has been a serious challenging problem in multilevel power converters, since its inception. Although many efforts have been made to balance the dc link capacitor voltages [14], [15], researchers are still focusing on optimized solutions, that can eradicate other major issues like ripple reduction, harmonic current minimization and other qualitative parameters of the converter's performance. The sinusoidal disturbances originated from the harmonic currents, incurred during dc link capacitor switching have pulled the researcher's interest [16]. Despite the fascinating adaptive controllers [17], observers and estimators play a vital role in classical control theory, when it comes to deterministic and stochastic control approaches respectively. Once such good option to counter these sinusoidal disturbances, is the use of Luenberger observer [18], which

consequently solves the dc link capacitor voltage balancing problem.

In our project a simple redundancy approach is used when the control strategy is defined in the $\alpha\beta$ stationary frame; where as a deterministic approach is used when the control strategy is defined in the $\alpha\beta\gamma$ frame. In the control strategy defined in $\alpha\beta\gamma$ frame (or three component control), the γ-component is used to balance the dc-link capacitor voltages and to remove the lower order harmonics, occurred during capacitor switching to an acceptable level.

The thesis work primarily addresses the two possible cases in the T-type inverter system, i.e. the case of using separate DC voltage sources and the case of introducing the dc link capacitors. The former case does not need a dc link capacitor voltage balancing strategy and a simple two dimensional SVM scheme is used. The latter one needs a separate control strategy for balancing the dc link capacitors. This case is again discussed into two strategies of balancing the dc link capacitor voltages i.e. the redundancy approach and the deterministic approach. In redundancy approach a simple static relation is considered to solve the dc link capacitor voltage balancing issue, whereas in deterministic approach a Luenberger Observer control scheme is used. In redundancy approach a two dimensional SVM is used, whereas in deterministic approach both three dimensional SVM and three dimensional FFSVM are the possible modulation schemes. It is to be noted that in all the cases a Generalized Predictive Control (GPC) approach is used for tracking output voltage. The GPC calculates the control signals to track the desired output filter capacitor voltages. A comparison of the T-type inverter system's performance is made for the different approaches, in order to understand, investigate and realize the importance of the deterministic approach of capacitor voltage balancing method.

The thesis report mainly comprises eight chapters including the introductory chapter. The 2nd chapter gives a basic idea of multilevel inverters, its topologies, various modulation and control schemes. The next chapter throws light on the NPP power inverter, thereby stating its importance. The 4th chapter, named 'System description, modeling and control design' is the core work of the thesis, which initially describes the GPC strategy. It also discusses the T-type inverter system in case wise including its modulation-cum-control methodologies. This further includes modeling the inverter system for both GPC design and for deriving the dc link capacitor and inductor dynamics, which are the key concepts in deterministic approach. At the end of this chapter a comparison of the redundancy and the deterministic approaches are discussed. The 5th chapter describes the prototype design of the NPP converter and its evaluation. The advantages and applications are discussed in chapter 6. Chapter 7 is inferred with few conclusions and future work. Chapter 8 comprises the references cited.

CHAPTER 2

MULTILEVEL INVERTERS

Industrial applications utilize both high and medium power levels and this is fairly possible only with multilevel converters. So, one can extract many voltage levels from multilevel converters based on his/her application need or interest. The foremost reasons to go for multilevel inverters are to avoid step up transformer during each stage of power conversion and to reduce output harmonics. Such multilevel converters are widely used in integration of renewable energy resources, ships, aviation, traction, Uninterruptible Power Supplies (UPS), High Voltage Direct Current (HVDC) systems, Flexible AC Transmission System (FACTS), variable-frequency drives, electric vehicle drives and air conditioning applications.

By definition,
'Multilevel inverters are power converters composed by an array of semiconductors and capacitor voltage sources, that when properly controlled, can generate waveform output voltages with adjustable frequency and amplitude'.

Since the inception of multilevel converters [19] during 1975, research and development in multilevel converters have revolutionized much. Firstly, it all began with a simple three level power converter, which later led to development of different topologies and control methods [20]. These revolutions have mainly resulted in possible up-gradations of different topologies, modulation schemes, control methodologies, harmonics reduction possibilities and balancing of dc link capacitor voltages. The basic idea of multilevel converter is to get different output voltage levels by switching the semiconductor switches in an orderly fashion, resulting in a staircase output voltage, which is later inverted by a filter circuit to produce an AC output to be utilized by the load. Turning off a semiconductor switch is called commutation and this commutation is done in an orderly fashion, such that a different voltage levels are achieved at the output. Switching sequences of these semiconductor switches are generated by modulators, which are discussed in detail in section 2.2.
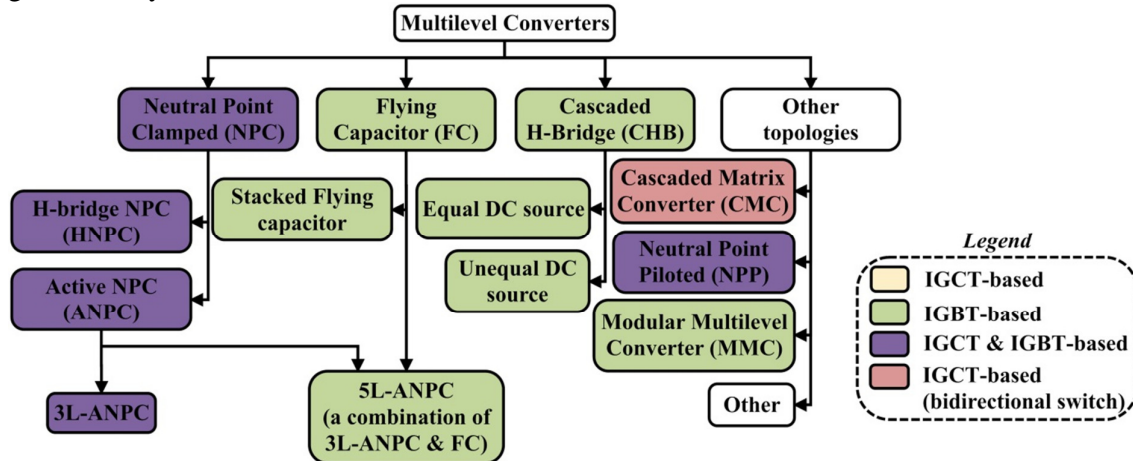
Fig. 2.1. Different multilevel converter topologies

The multilevel power converters have the following advantages:
➢ Reduced dv/dt stresses and electromagnetic compatibility (EMC) problems, which improves the staircase waveform quality.
➢ Smaller Common Mode (CM) voltage

- Low distortion of input current
- Operates at both fundamental and high switching frequencies
- Higher voltage operation (above classic semiconductor limits)
- Lower voltage distortion (more sinusoidal waveforms)
- Multilevel converters are well suitable for reactive power compensation.

Although multilevel converters are mature technologies, there is always a rising demand in new topologies, modulation schemes and control strategies to counteract one or more drawbacks of conventional one and to go on with a newly proposed converting technology.

2.1. INVERTER TOPOLOGIES

Although many topologies and its industrial applications are found in literature [21] [22], the three major multilevel converter types are Neutral Point Clamped (NPC) converter, Cascaded H-Bridge (CHB) converter and Flying Capacitor Converter (FCC). Figure 2.1 shows the classification of multilevel converters [23].

2.1.1. NEUTRAL POINT CLAMPED MULTILEVEL INVERTER

The Neutral Point Clamped (NPC) converter was initially proposed by Nabae, Takahashi, and Akagi in 1981 [24], which laid a foundation to the era of voltage source multilevel high power converters. Figure 2.2 shows a single phase NPC for which the switching states are given in Table 2.1. The lower leg switches are the complementary of those of the upper leg switches. The clamping diodes allow the connection of the phase output to the midpoint of the dc link i.e. neutral (N) and this paves a way for three voltage levels. It is to be noted that if 'L' is the number of levels in phase to neutral voltage (V_{aN}), then the number of steps in phase to phase voltage (V_{ab}) is '2L-1'. The blocking voltage of the power devices is equal to $V_{dc}/(L-1)$. NPCs are used for medium and high voltage applications. Integrated Gate Commutated Thyristors (IGCT) or Insulated Gate Bipolar Transistor (IGBT) is commercially used as switching devices. If the converter is for high voltage and high current applications, IGCT is a good choice of option. It is to be noted that IGBT has lower commutation losses and easy drivers, but it has high conduction losses.. Commercial NPCs include ACS 1000, SINAMICS SM120, Altivar 1000, etc. whose maximum power ranges from 10 to 40 MW.

Advantages of multilevel diode-clamped inverters:
- As all of the phases share a common dc bus, the capacitance requirement of the converter gets reduced. Due to this, NPC favors back-to-back regenerative applications.
- The capacitors can be pre-charged in a group.
- For fundamental switching frequency, the efficiency is high.
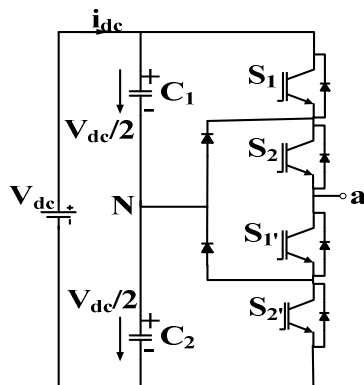
Fig. 2.2. A single phase NPC

Table.2.1 Switching states of a three level single phase NPC

Voltage V_{aN}	Switching states			
	S_1	S_2	$S_{1'}$	$S_{2'}$
$V_{dc}/2$	1	1	0	0
0	0	1	1	0
$-V_{dc}/2$	0	0	1	1

Disadvantages of multilevel diode-clamped inverters:
➢ Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without precise monitoring and control.
➢ The inner most devices are switched on for most of the time. To overcome this and maintain a nominal uniformity, the Active Neutral Point Clamped (ANPC) were introduced.
➢ The total number of clamping diodes required is quadratically related to the number of levels, which can be more complex for units with a high number of levels.

2.1.2. CASCADED H-BRIDGE INVERTER

The cascaded H-Bridge converters are first introduced during late 1960s [25], [26], which paved a way to think of using a separate DC source in multilevel converters. As the name 'CHB' defines the use of multiple units of H-bridge power cells, which are connected in series such that the output voltage is the sum of each inverter outputs. Each Separate DC Source (SDCS) is connected to a single-phase full-bridge or H-bridge inverter. A conventional H-bridge cell is shown in the figure 2.3, whose switching states are given in table 2.2. The lower leg switches in each CHB cell are the complementary of the upper leg switches. The H-bridge cells are connected in series to form multilevel cascaded converters. The connection can be symmetrical (using same dc source values) or asymmetrical (using different dc sources). Figure 2.4 shows the leg-scheme of a symmetrical five-level CHB converter, whose switching states are given in the table 2.3.

It is to be noted that, for a 'm' level symmetrical cascaded H-bridge converter the number of dc sources needed is (m-1)/2 & the maximum number of level of line-to-line output voltage is (2m-1). CHB converters are best suitable for large PV-plants, when used with an isolated DC-DC conversion stage [27]. They are ideal for renewable energy integration and traction systems. Commercial CHB converters are available in ABB, Arrow speed & Siemens (Perfect harmony).
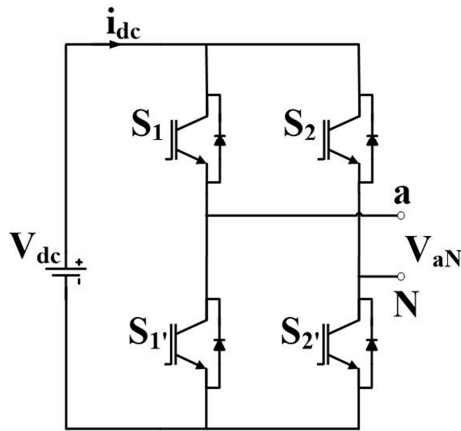
Fig. 2.3. Conventional H-bridge (3 Level, single phase) converter

Table.2.2 Switching states of a single phase three level H-Bridge converter

Voltage, V_{aN}	Switching states	
	S_1	S_2
$V_{dc}/2$	1	0
0	0	0
0	1	1
$- V_{dc}/2$	0	0

Advantages of cascaded H-bridge inverters:
➢ The modular structure or the multiple units of identical H-bridge power cell reduces the manufacturing cost.
➢ The number of possible output voltage levels is more than twice the number of dc sources.
➢ Less voltage THD and dv/dt when compared to two level converters operating at the same

voltage rating and switching frequency.
- H-bridge cells are cascaded to produce high AC voltages, which eliminates the problem of equal voltage sharing for series-connected devices.
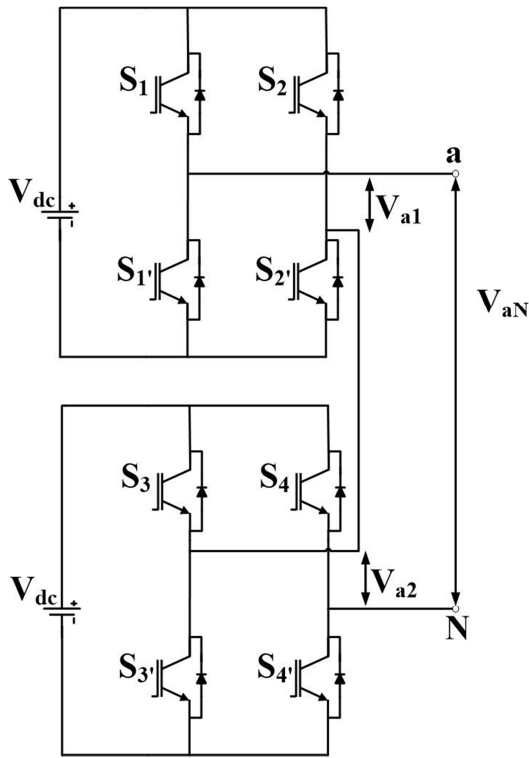
Fig. 2.4. Five-level single phase H-bridge converter

Table.2.3 Switching states of a Five level single phase H-Bridge Converter

Voltage, V_{aN}	Switching states				Individual cell output voltage	
	S_1	S_2	S_3	S_4	V_{a1}	V_{a2}
$2V_{dc}$	1	0	1	0	V_{dc}	V_{dc}
V_{dc}	1	0	1 / 0	1 / 0	V_{dc}	0
	1 / 0	1 / 0	1	0	0	V_{dc}
0	0	0	0	0	0	0
	0	0	1	1		
	1	1	0	0		
	1	1	1	1		
	1	0	0	1	V_{dc}	$-V_{dc}$
	0	1	1	0	$-V_{dc}$	V_{dc}
$-V_{dc}$	0	1	0 / 1	0 / 1	$-V_{dc}$	0
	0 / 1	0 / 1	0	1	0	$-V_{dc}$
$-2V_{dc}$	0	1	0	1	$-V_{dc}$	$-V_{dc}$

Disadvantage of cascaded H-bridge inverters:
- A large number of separate dc sources are required for CHB, which are usually obtained from a multi-phase diode rectifier by employing an expensive phase shifting transformer.

2.1.3. FLYING CAPACITOR MULTILEVEL INVERTER

The flying capacitors were first introduced by Meynard and Foch in 1992 [28]. As the name suggests, a capacitor is connected between the upper and the lower leg or between the two cells. In other words, the free-wheeling diodes in NPC are replaced by a capacitor. Figure 2.5 shows a three level single phase FC, which has two cells. Additional cells can be added to increase the number of output levels, but the nominal power of the converter remains the same. It is to be noted that for 'm' voltage level, flying capacitor needs 2(m-1) semiconductor switches, (m-1) DC bus capacitors and (m-1)(m-2)/2 number of balancing capacitors per phase. Table 2.4 shows the switching states of a three-level single phase FC. The phase redundancy switching state-zero voltage is used to control the floating capacitor voltage. A well-known commercial flying capacitor converter is Alstom VDM 6000. ABB's ACS 2000 is an example of hybrid FCC, which is a combination of a 3L-ANPC and a FCC.

Advantages of flying capacitor inverters:
- Unlike other inverters, switching combination redundancies even in inner voltage levels makes balancing the voltage levels of the capacitors easier and flexible with more switching combinations.
- Real and reactive power flow can be controlled making a possible voltage source converter candidate for high voltage dc transmission [29], [30].
- Large number of capacitors enables the inverter to ride through capabilities during power rage.
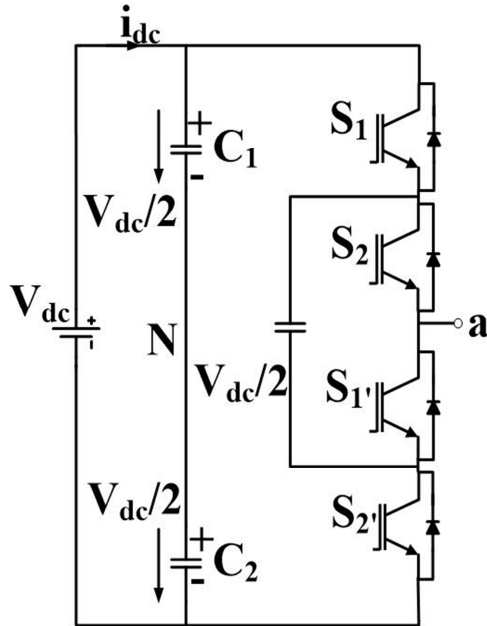
Fig. 2.5. Three-level single phase flying capacitor converter

Table.2.4 Switching states of a three level single phase FCC

Voltage, V_{aN}	Switching states	
	S_1	S_2
$V_{dc}/2$	1	1
0	1	0
0	0	1
$-V_{dc}/2$	0	0

Disadvantages of flying capacitor inverters:
- Control is complicated to regulate the voltage levels for all of the capacitors. Also, precharging all of the capacitors to the same voltage level and startup are complex.
- Inverter control will be very complicated and the switching frequency and switching losses will be high for real power transmission.
- The large numbers of capacitors are both more expensive and bulky than clamping diodes in multilevel diode-clamped converters. Packaging is also more difficult in inverters with a high number of levels.

Apart from the above topologies, there are Modular Multilevel Converter (MMC) [31], Cascaded Matrix Converter (CMC) [32], [33] and Neutral Point Piloted (NPP) converter [34]. There also exists symmetrical topologies like n-level Cascaded Cell Multilevel Converter (CCMC) [35], [36], which do not have a common dc link; instead they are made of stages, connected in series, which comprises two basic cells in parallel connection. These basic cells share a common DC source or capacitor. Asymmetric topologies also prevail, like Hybrid Multilevel Converter (HMC) [37] where different stages are connected in series, that has different values of DC voltages and Cascade Asymmetric Multilevel Converter (CAMC) [38], which is a combination of ANPC and FC.

In the project work, the NPP or T-type inverter is used & the emphasis lies on it, which is discussed in chapter 3 in detail.

2.2. MODULATION SCHEMES

The major modulation schemes are Pulse Width Modulation (PWM), Space Vector Modulation (SVM) & harmonic control. Focus on new and hybrid modulation schemes rely on encountering other issues like using less number of switches, optimizing output voltage control, solving the dc link capacitor voltage balancing problem, reducing or eliminating the harmonic contents, increasing robustness & fault tolerance capability, etc. Figure 2.6 shows the major modulation types in multilevel converters [39].
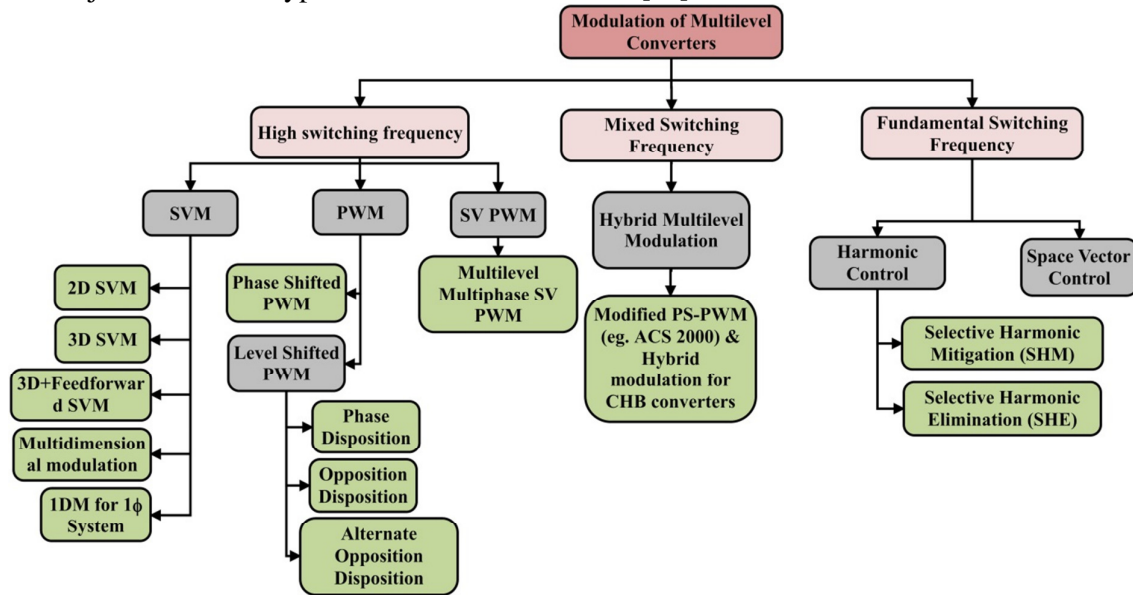
Fig. 2.6. Various modulation schemes for multilevel converters

Pulse Width Modulation (PWM): The basic idea in PWM is to compare a reference signal with a carrier signal in order to obtain a constant frequency PWM signal, which is used as firing pulses for the semiconductor switches. Numerous developments in optimizing the PWM technique have been done since its inception [10]. In Bipolar PWM (Two level voltage case), a simple triangular carrier signal is compared with a sine reference and those overlapping with the upper and lower carrier signals are given as switching pulses to the lower and upper switches respectively. In Unipolar PWM (used for single phase, three level voltage converter) a triangular carrier signal is compared with two reference sine waves of 180^0 shifted from each other. The switching pulses obtained from the positive sine wave overlapping are applied to one leg and the switching pulses obtained from the negative sine wave overlapping are applied to the other leg. In Phase shifted PWM (used for FCC or CHB converter) n-1 triangular carrier signals are used with optimal displacement 180⁰/m (where 'n' is the number of voltage levels and 'm' is the number of cells) are overlapped using a reference sine wave and the switching pulses are given to the converters. The number of carrier signals depends on the number of cells used. For example: In a three level FCC two carrier signals are used whereas in a four level FCC three carrier signals are used. In Level shift PWM the carrier signals are arranged in a vertical shift. For a m-level inverter, (m-1) carrier signals are needed. The below control logics are used in the level shifted PWM used for a three level converter:

➢ If the reference is above the carriers the upper switches are turn on.
➢ If the reference is between both carriers the output is connected to the neutral point.
➢ If the reference is under both carriers the lower switches are turned on.

In phase disposition, the carrier signals are aligned in a similar fashion, whereas in opposition disposition, the lower carrier signals are 180⁰ phase shifted from the upper signals, whereas

in alternate opposition disposition, the carrier signals are 180° phase shifted from each other.

Space Vector Modulation (SVM): The basic idea of SVM is to switch the semiconductor switches, by locating a reference signal on the Space Vector (SV) of appropriate level and finding the nearest switching vectors and their corresponding switching times. In a 2D SVM [11], the three phase reference is transformed to g-h coordinate system and the closest three vector are found and switched, whereas in a 3D SVM [12], a normalized phase voltage references are located in a three-dimensional space and the closed four vectors are switched. The feedforward 3D SVM [13] takes into account the actual dc-link capacitor voltage imbalance and uses a modulation scheme similar to 3D with slight changes. The 1DM for single phase multilevel converters uses the 1-D control region to identify the possible switching states and their duty cycles [40]. The multidimensional modulation technique is a generalized modulation scheme for cascaded multilevel converters, which determines the switching states on a multidimensional control region [41]. Here, the DC voltage control strategy is used on a 2D control region. One can consider the real values of dc-link capacitor voltages and extend the feedforward mD-PWM scheme for cascaded converters. (where m is the number of cells). In SVPWM technique, the reference voltage vector is resolved by time-averaging with the nearest active switching vectors. In Multilevel multiphase SVPWM [42], the concept of permutation matrix is introduced, which determines the switching time of the switches.

Hybrid multilevel modulation: Modified carrier-based PWM are used in Active NPCs, where n-1 triangular carriers are used which are phase-shifted by 90°(where n is the number of voltage level). Such modulation schemes are advantageous to balance the dc link capacitor voltages inherently in medium voltage power inverters. In 5L-ANPC a fundamental switching is used for ANPC cell and a phase-shifted PWM is used for the flying-capacitor cell [43].

Space vector control for multilevel converters: The basic idea of space vector control is when using multilevel inverters with high number of levels (which results in high space vector density) there is no need of modulation. Space vector control approximates the reference vector by the closest space vector generated by the inverter. The approximation is compensated by outer loop controllers and the inverter works with low switching frequency.

Harmonic control: In Selective Harmonic Elimination (SHE) [44] the 'n' lower-order odd, nontriplen (non-multiple of 3) harmonics are eliminated by solving a set of m= n+1 equations for fundamental amplitude and 'm' angles. The Selective Harmonic Mitigation (SHM) [45] is based on SHMPWM, that generates switching three-level PWM patterns to meet grid codes with high quality from harmonic perspective, thereby avoiding the elimination of some specific harmonics. Later an optimized SHM [46] is identified by, which are applied to high power converters with low switching frequency. In both the cases the objective functions are optimized by algorithms like Genetic Algorithm (GA), simulated annealing, etc.

The modulation schemes used in the project are 2D SVM, 3D SVM and 3D FFSVM, which are explained in detail in the chapter 4.

2.3. CONTROL STRATEGIES
The control strategies comprise concepts like direct power control [47], [48], [49], Model Predictive Control (MPC) [50], [51], hysteresis/non-hysteresis control of current [52], using conventional controllers like PI [53], fuzzy PID [54], neural network & fuzzy logic methods

[55] etc. and other advanced control techniques. Most new works rely and emphasize on strategies like harmonics reduction, dc link capacitor voltage balancing, less computation effort, new efficient control methods, that can solve one or more other issues and increased system performance. For this, one has to undergo a modeling approach to the converter system which is discussed in detail in chapter 4. All these modeling strategies need a prior knowledge of fundamental Clarke [56] & Park [57] transformation. Both the transformations are basically used to simplify the analysis of three phase circuits. The Clarke's transformation is used in the project, which facilitates the inclusion of the third control component i.e. the gamma (γ) or zero (0) component. This γ component is used to solve the dc link capacitor issue in the deterministic approach, which is discussed in detail in chapter 4.

CHAPTER 3

NEUTRAL POINT PILOTED (NPP) POWER INVERTER

The Neutral Point Piloted converter [58], [59] or the T-type converter is an extension of the conventional two-level Voltage Source Converter (VSC) with an active bidirectional switch to the dc-link midpoint, which blocks only half of the dc link voltage. Figure 3.1 (a) shows the leg schematic of a three-level T-type power converter, whose bidirectional switches are conventional IGBTs. Hence, it can be implemented with devices having a lower voltage rating. Due to this feature, the converter shows very low switching losses, acceptable conduction losses and lower number of semiconductor devices, when compared to conventional topologies like NPC and FCC. Although the T-type converters were introduced during 1985 [60], owing to demand in rise of compact and efficient low power converters, various developments are made in these T-type converters to be more reliable and fault tolerant [61], [62].

Later these conventional AC switches were replaced by Reverse blocking IGBT (RB-IGBT) [63] which has low switching losses and better reverse blocking capability. When seen from fabrication perspective, the module with RB-IGBT has only one pn-junction and this reduces the reverse recovery. Figure 3.1(b) shows the leg schematic of a three-level T-type power converter, whose bidirectional switches are RB-IGBT.
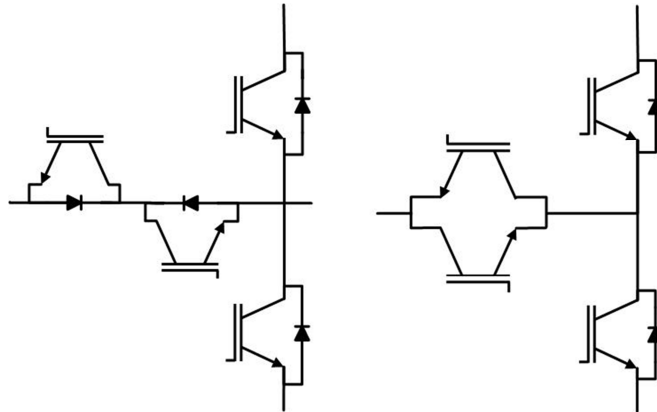
Fig. 3.1. Leg schematic of a three-level T-type power inverter : (a) bidirectional switch with conventional IGBT, (b) bidirectional switch with RB-IGBT

Table 3.1. Switching states of a single phase T-type converter

Voltage, V_{aN}	Switching states			
	T_1	T_2	T_3	T_4
$V_{dc}/2$	1	0	0	0
0	0	0	1	1
$-V_{dc}/2$	0	1	0	0
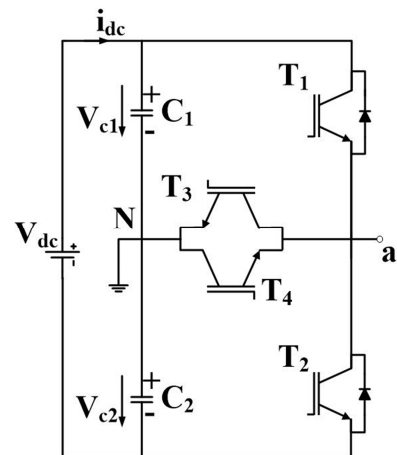
Fig. 3.2. Leg schematic of a single phase three level T-type converter

11

Figure 3.2 shows the circuit of a single phase T-type inverter. Table 3.1 shows the switching states of the T-type converter. Additionally, these T-type inverters are promising power conversion topologies for medium switching frequencies from 6-20 kHz. There T-type inverters are used in applications of low or medium power like small PV-systems and standalone applications [58], [59].

CHAPTER 4

SYSTEM DESCRIPTION, MODELING & CONTROL DESIGN

This chapter is the core work of thesis, that discusses on various aspects of how the output voltage is controlled and the capacitor voltage balance is achieved. The chapter is divided into three sub-chapters, which discusses initially about the Generalized Predictive Control (GPC) of output voltage control. Then, the topic on application of the GPC on the T-type inverter with individual voltage sources is discussed. The next part of the chapter explains how the dc link capacitor voltage balancing problem is solved by two approaches i.e. redundancy and deterministic approach. At last a comparison on system performance is done on these two approaches.

4.1. GPC STRATEGY FOR OUTPUT VOLTAGE CONTROL

The output voltage control is the primary objective, which is implemented by the Model Predictive Control (MPC) approach [64]. The MPC calculates the control signals to track the desired output capacitor AC voltages. These control signals are the $\delta_{\alpha\beta}$ component, which are the effective multiple of the reference voltage for the modulators.

MPC is a family of control techniques that has been successfully applied to power converter applications [65], [66]. The MPC strategy is based on explicitly using a model of the power inverter system to predict the process output at future time instants (called horizons). A control sequence is calculated in order to minimize an objective function and receding strategy is used, so that at each sampling instant the prediction horizon is displaced towards the future [67].

The GPC strategy, proposed by Clarke *et al*. is a well know control strategy in MPC family [9]. GPC favors many advantages like robustness and reasonable number of design variables intrusion, when applied to power converters.

GPC is based on predicting the output by using a Controlled Auto-Regressive and Moving-Average (CARIMA) model:

$$A(z^{-1})y(t) = B(z^{-1})z^{-d}u(t-1) + C(z^{-1})\frac{e(t)}{\Delta} \tag{1}$$

where $y(t)$ is the output of the system, $u(t)$ is the control sequence, d is the dead time or delay of the system, $e(t)$ is the zero mean white noise and $\Delta = (1-z^{-1})$. A, B and C are the polynomials in backward shift operator z^{-1}, which are obtained from the system transfer function.

When applying the GPC strategy to the T-type inverter system, the dead time, d is equal to 0 and for simplicity, the noise polynomial $C(z^{-1})$ is considered to be equal to 1. The CARIMA model for the inverter system becomes,

$$A(z^{-1})y(t) = B(z^{-1})u(t-1) + C(z^{-1})\frac{v(t)}{\Delta} \tag{2}$$

where y(t) is the output voltage & v(t) is an additive white Gaussian noise.

The optimal prediction is done by solving the Diophantine equation, whose solution is obtained by recursive algorithm. This algorithm uses the transfer function model of the system. The Diophantine equation is given by,

$$C(z^{-1}) = E_j(z^{-1})\tilde{A}(z^{-1}) + z^{-j}F_j(z^{-1}) \tag{3}$$

where E_j and F_j are the polynomial obtained by dividing 1 by $\tilde{A}(z^{-1})$ until the remainer can be factorized as $z^{-j}F_j(z^{-1})$, j is the value of prediction horizon and $\tilde{A}(z^{-1}) = \Delta A(z^{-1})$.

Applying the Diophantine equation to the T-type inverter system, the noise polynomial, $C(z^{-1})$ is taken as 1 (as considered before),

$$1 = E_j(z^{-1})\tilde{A}(z^{-1}) + z^{-j}F_j(z^{-1}) \tag{4}$$

A control sequence is applied that minimizes a multistage cost function, which is of the form,

$$J(N_1, N_2, N_u) = \sum_{j=N_1}^{N_2} \delta(j)[\hat{y}(t+j|t) - w(t+j)]^2 + \sum_{j=1}^{N_u} \lambda(j)[\Delta u(t+j-1)]^2 \tag{5}$$

where N_1 is the minimum costing horizon, N_2 or N_h is the maximum costing horizon, N_u is the control horizon, $w(t+j)$ is the future reference trajectory, $\delta(j)$ and $\lambda(j)$ are the weighting sequences & $\hat{y}(t+j|t)$ is an optimum j step ahead prediction of the system output on data up to time t.

When the cost function is applied to the T-type inverter system, it get minimized to,

$$J = \sum_{j=1}^{N_h}[\hat{y}(t+j|t) - w(t+j)]^2 + \sum_{j=1}^{1} \lambda(j)[\Delta u(t+j-1)]^2 \tag{6}$$

where control horizon, N_u=1 and the initial cost horizon, N_1=1.

When (2) is multiplied by $\Delta E_j(z^{-1})z^j$,

$$\tilde{A}(z^{-1})E_j(z^{-1})y(t+j) = E_j(z^{-1})B(z^{-1})\Delta u(t+j-1) + E_j(z^{-1})v(t+j) \tag{7}$$

Substituting (4) in (7),

$$y(t+j) = F_j(z^{-1})y(t) + E_j(z^{-1})B(z^{-1})\Delta u(t+j-1) + E_j(z^{-1})v(t+j) \tag{8}$$

where the polynomial $E_j(z^{-1})$ is of degree (j-1), the noise components are all in the future, so the optimal prediction is given by,

$$y(t+j|t) = F_j(z^{-1})y(t) + G_j(z^{-1})\Delta u(t+j-1) \tag{9}$$

where j>1 and $G_j(z^{-1}) = E_j(z^{-1})B(z^{-1})$.

The aim of the GPC is to compute the future control sequence u(t), u(t+1),…. in such a way that the future voltage output, y(t+j) coincides with the reference trajectory w(t+j). Let us consider a definite prediction horizon (say for instance j = 1,2,….,N) during which, a sequence of future control signals is calculated at each sampling instant until the output is close to the reference.

When (9) is considered for a set of j ahead optimal predictions and expressed in terms that depend only on past values and others which are dependent on the future control signals as

$$y = Gu+f \tag{10}$$

The cost function J obtained by substituting (10) in (6),

$$J = (Gu + f - w)^T(Gu + f - w) + \lambda u^T u \tag{11}$$

where, G matrix describes the system dynamics, f is the free response of the system, w is the reference sequence or future set-point and u is the future control input with the following vectors,

$$G = \begin{pmatrix} g1 & 0 & 0 & ... & 0 \\ g2 & g1 & 0 & ... & 0 \\ g3 & g2 & g1 & ... & 0 \\ . & . & & & . \\ . & . & & & . \\ . & . & & & . \\ gN_u & gN_u-1 & & ... & g1 \\ . & . & & . & . \\ . & . & & . & . \\ . & . & & . & . \\ gN & gN-1 & & ... & gN-N_u+1 \end{pmatrix} ; u = \begin{pmatrix} \Delta u(t) \\ \Delta u(t+1) \\ . \\ . \\ . \\ \Delta u(t+N-1) \end{pmatrix} ; w = \begin{bmatrix} w(t+1) & w(t+2) & . & . & . & w(t+N) \end{bmatrix}^T$$

The minimal cost function, J can be obtained by making its gradient equal to zero.

$$\frac{\partial J}{\partial u} = 0 \tag{12}$$

where u is the increment of control signal applied at each sampling instant, which leads to,

$$u = (G^T G + \lambda I)^{-1} G^T (w - f) \tag{13}$$

The control signal that is actually sent as input to the system is the first element of vector u, which is given by

$$\Delta u(t) = K(w - f) \tag{14}$$

where K is the vector of first row of matrix $(G^T G + \lambda I)^{-1} G^T$

The steps are repeated at each sampling instant. There will be no change in the control signal, if there exists no future prediction errors, i.e., if (w-f) = 0. It is to be noted that, all these computational steps (up to finding the K vector) are done explicitly during initiation of simulation [68].
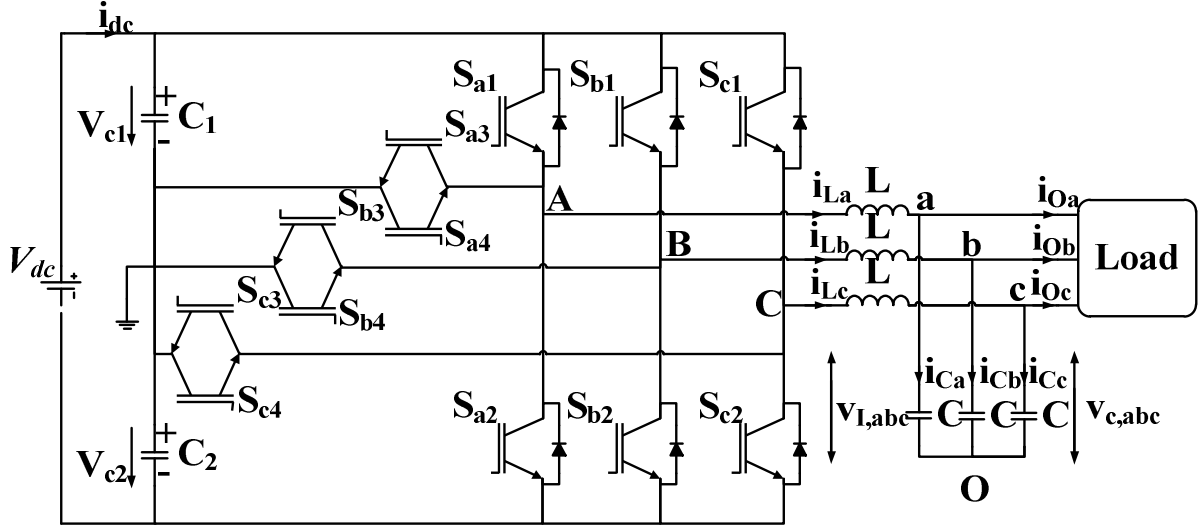
Fig. 4.1. Scheme of T-type converter connected to load via LC filter

The figure 4.1 shows the scheme of the T-type converter connected to a RL load via a LC filter [69], whose descriptions are given in table 4.1. Table 4.2 consists of the model and simulated parameters. It is to be noted that the load resistance, R_l used in actual simulation is 15 Ω, whereas the R_l used in model is 60 Ω. This is a model mismatch and the GPC is later notified for tackling this situation well, thereby predicting the output voltage across the filter capacitor.

The dynamic equations of the output filter inductor currents and the output filter capacitor voltages are as follows,

$$i_{L,abc} = C \frac{dv_{C,abc}}{dt} + i_{O,abc} \tag{15}$$

$$V_{I,abc} = L \frac{di_{L,abc}}{dt} + V_{C,abc} \tag{16}$$

15

Table 4.1 System Variables and Parameters

Variable	Description
$V_{C,abc} = \{v_{aO}\ v_{bO}\ v_{cO}\}^T$	Output filter capacitor voltage vector
$i_{L,abc} = \{i_{La}\ i_{Lb}\ i_{Lc}\}^T$	Output filter inductor current vector
$V_{I,abc} = \{v_{AO}\ v_{BO}\ v_{CO}\}^T$	T-type output voltage vector
$i_{O,abc} = \{i_{Oa}\ i_{Ob}\ i_{Oc}\}^T$	Output load current vector
$S_{abc} = \{S_a\ S_b\ S_c\}^T$	Switching vector
$S_{p\,|\,p=\{a,\,b,\,c\}} = \{-1,\,0,\,1\}$	Switching functions
L	Output filter inductance
C	Output filter capacitance
V_{dc}	dc-link voltage
i_{dc}	dc-link current
$C_1,\ C_2$	dc-link capacitance

Table 4.2 Model & Simulation Parameters for GPC

Parameter	Value
Output filter inductance, L	2mH
Output filter capacitance, C	50μF
Switching frequency, f_{sw}	10kHz
Output load resistance (model), R_l	60Ω
Output load resistance (actual), R_l	15Ω
V_{dc}	400V
Output voltage reference, V_{RMS}	120V
Weighting factor, λ	0.95 (say)
Control horizon, N_u	1
Prediction horizon, N	6 (say)

GPC formulation (for example)

Transfer function of the inverter system considering the output filter and load is given by,

$$H(s) = \frac{Y(s)}{U(s)} = \frac{1}{LCs^2 + \dfrac{L}{R_l}s + 1} = \frac{1}{(2\times10^{-3}\times50\times10^{-6})s^2 + (\dfrac{2\times10^{-3}}{60})s + 1} = \frac{1}{10^{-7}s^2 + 3.333\times10^{-5}s + 1}$$

Discretizing the system or taking Z-transform,

$$H(z\ ) = \frac{B(z)}{A(z)} = \frac{0.04904\,z + 0.0485}{z^2 - 1.8697\,z + 0.9672}$$

$$H(z^{-1}) = \frac{B(z^{-1})}{A(z^{-1})} = 1/z(\frac{0.04904 + 0.0485z^{-1}}{1\ -1.8697z^{-1} + 0.9672z^{-2}})$$

where, $A(z^{-1}) = 1 - 1.8697z^{-1} + 0.9672z^{-2}$

$B(z^{-1}) = 0.0490 + 0.0485\,z^{-1}$

$$C(z^{-1}) = 1 \quad \text{(noise polynomial)}$$

$$\tilde{A}(z^{-1}) = \Delta A(z^{-1}) = (1 - z^{-1})A(z^{-1}) = (1 - z^{-1})(1 - 1.8697z^{-1} + 0.9672z^{-2}) = 1 - 2.8697z^{-1} + 2.8369z^{-2} - 0.9672z^{-3}$$

The polynomials of the Diophantine equations are determined using the below recursive calculation steps.

Table 4.3 GPC recursive polynomial calculation across horizons

Prediction Horizon 1
$E_1 = 1$ $F_1 = z(1 - E_1\tilde{A}) = z[1 - (1 - 2.8697z^{-1} + 2.8369z^{-2} - 0.9672z^{-3})]$ $\quad = 2.8697 - 2.8369z^{-1} + 0.9672z^{-2}$ $G_1 = B(z^{-1})E_1 = (0.0490 + 0.0485z^{-1}) \times 1 = 0.0490 + 0.0485z^{-1}$
Prediction Horizon 2
$E_2 = E_1 + (F_1, 0)z^{-1} = 1 + 2.8697z^{-1}$ $F_2 = z^2(1 - E_2\tilde{A}) = z^2[1 - (1 + 2.8697z^{-1}) \times (1 - 2.8697z^{-1} + 2.8369z^{-2} - 0.9672z^{-3})]$ $\quad = 5.3982 - 7.1738z^{-1} + 2.7756z^{-2}$ $G_2 = B(z^{-1})E_2 = (0.0490 + 0.0485z^{-1}) \times (1 + 2.8697z^{-1}) = 0.0490 + 0.1892z^{-1} + 0.1392z^{-2}$
Prediction Horizon 3
$E_3 = E_2 + (F_2, 0)z^{-2} = 1 + 2.8697z^{-1} + 5.3982z^{-2}$ $F_3 = z^3(1 - E_3\tilde{A})$ $\quad = z^3[1 - (1 + 2.8697z^{-1} + 5.3982z^{-2}) \times (1 - 2.8697z^{-1} + 2.8369z^{-2} - 0.9672z^{-3})]$ $\quad = 8.3173 - 12.5385z^{-1} + 5.2212z^{-2}$ $G_3 = B(z^{-1})E_3 = (0.0490 + 0.0485z^{-1}) \times (1 + 2.8697z^{-1} + 5.3982z^{-2})$ $\quad = 0.0490 + 0.1892z^{-1} + 0.4039z^{-2} + 0.2618z^{-3}$
Prediction Horizon 4
$E_4 = E_3 + (F_3, 0)z^{-3} = 1 + 2.8697z^{-1} + 5.3982z^{-2} + 8.3173z^{-3}$ $F_4 = z^4(1 - E_4\tilde{A})$ $\quad = z^4[1 - (2.8697z^{-1} + 5.3982z^{-2} + 8.3173z^{-3}) \times (1 - 2.8697z^{-1} + 2.8369z^{-2} - 0.9672z^{-3})]$ $\quad = 11.3294 - 18.3740z^{-1} + 8.0446z^{-2}$ $G_4 = B(z^{-1})E_4 = (0.0490 + 0.0485z^{-1}) \times (2.8697z^{-1} + 5.3982z^{-2} + 8.3173z^{-3})$ $\quad = 0.0490 + 0.1892z^{-1} + 0.4039z^{-2} + 0.6697z^{-3} + 0.4034z^{-4}$
Prediction Horizon 5
$E_5 = E_4 + (F_4, 0)z^{-4} = 1 + 2.8697z^{-1} + 5.3982z^{-2} + 8.3173z^{-3} + 11.3294z^{-4}$ $F_5 = z^5(1 - E_5\tilde{A})$ $\quad = z^5[1 - (1 + 2.8697z^{-1} + 5.3982z^{-2} + 8.3173z^{-3} + 11.3294z^{-4}) \times (1 - 2.8697z^{-1} + 2.8369z^{-2} - 0.9672z^{-3})]$ $\quad = 14.1378 - 24.0958z^{-1} + 10.9580z^{-2}$ $G_5 = B(z^{-1})E_5 = (0.0490 + 0.0485z^{-1}) \times (1 + 2.8697z^{-1} + 5.3982z^{-2} + 8.3173z^{-3} + 11.3294z^{-4})$ $\quad = 0.0490 + 0.1892z^{-1} + 0.4039z^{-2} + 0.6697z^{-3} + 0.9589z^{-4} + 0.5494z^{-5}$
Prediction Horizon 6
$E_6 = E_5 + (F_5, 0)z^{-5} = 1 + 2.8697z^{-1} + 5.3982z^{-2} + 8.3173z^{-3} + 11.3294z^{-4} + 14.1378z^{-5}$ $F_6 = z^6(1 - E_6\tilde{A})$ $\quad = z^6[1 - (1 + 2.8697z^{-1} + 5.3982z^{-2} + 8.3173z^{-3} + 11.3294z^{-4} + 14.1378z^{-5}) \times (1 - 2.8697z^{-1} + 2.8369z^{-2} - 0.9672z^{-3})]$ $\quad = 16.4752 - 29.1496z^{-1} + 13.6743z^{-2}$ $G_6 = B(z^{-1})E_6$ $\quad = (0.0490 + 0.0485z^{-1}) \times (1 + 2.8697z^{-1} + 5.3982z^{-2} + 8.3173z^{-3} + 11.3294z^{-4} + 14.1378z^{-5})$ $\quad = 0.0490 + 0.1892z^{-1} + 0.4039z^{-2} + 0.6697z^{-3} + 0.9589z^{-4} + 1.2427z^{-5} + 0.6856z^{-6}$

The predicted output calculated for values from j=1 to j=6 and is given by,
$$y = Gu + F(z^{-1})y(t) + G'(z^{-1})\Delta u(t-1)$$

with $G = \begin{pmatrix} 0.0490 & 0 & 0 & 0 & 0 & 0 \\ 0.1892 & 0.0490 & 0 & 0 & 0 & 0 \\ 0.4039 & 0.1892 & 0.0490 & 0 & 0 & 0 \\ 0.6697 & 0.4039 & 0.1892 & 0.0490 & 0 & 0 \\ 0.9589 & 0.6697 & 0.4039 & 0.1892 & 0.0490 & 0 \\ 1.2427 & 0.9589 & 0.6697 & 0.4039 & 0.1892 & 0.0490 \end{pmatrix}$; $F = \begin{pmatrix} 2.8697 & -2.8369 & 0.9672 \\ 5.3982 & -7.1738 & 2.7756 \\ 8.3173 & -12.5385 & 5.2212 \\ 11.3294 & -18.3740 & 8.0446 \\ 14.1378 & -24.0958 & 10.9580 \\ 16.4752 & -29.1496 & 13.6743 \end{pmatrix}$;

$$G' = \begin{pmatrix} 0.0485 \\ 0.1392 \\ 0.2618 \\ 0.4034 \\ 0.5494 \\ 0.6856 \end{pmatrix}$$

where G' is the matrix of coefficients of the right-most backward shift operator of G_j, where j takes the value 1 to N_h or N_2 (prediction horizon).

K = first row of $(G^T G + \lambda I)^{-1} G^T$

= first row of

$$\left(\begin{pmatrix} 0.0490 & 0 & 0 & 0 & 0 & 0 \\ 0.1892 & 0.0490 & 0 & 0 & 0 & 0 \\ 0.4039 & 0.1892 & 0.0490 & 0 & 0 & 0 \\ 0.6697 & 0.4039 & 0.1892 & 0.0490 & 0 & 0 \\ 0.9589 & 0.6697 & 0.4039 & 0.1892 & 0.0490 & 0 \\ 1.2427 & 0.9589 & 0.6697 & 0.4039 & 0.1892 & 0.0490 \end{pmatrix}^T \begin{pmatrix} 0.0490 & 0 & 0 & 0 & 0 & 0 \\ 0.1892 & 0.0490 & 0 & 0 & 0 & 0 \\ 0.4039 & 0.1892 & 0.0490 & 0 & 0 & 0 \\ 0.6697 & 0.4039 & 0.1892 & 0.0490 & 0 & 0 \\ 0.9589 & 0.6697 & 0.4039 & 0.1892 & 0.0490 & 0 \\ 1.2427 & 0.9589 & 0.6697 & 0.4039 & 0.1892 & 0.0490 \end{pmatrix} + 0.95 \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \right)^{-1} \begin{pmatrix} 0.0490 & 0 & 0 & 0 & 0 & 0 \\ 0.1892 & 0.0490 & 0 & 0 & 0 & 0 \\ 0.4039 & 0.1892 & 0.0490 & 0 & 0 & 0 \\ 0.6697 & 0.4039 & 0.1892 & 0.0490 & 0 & 0 \\ 0.9589 & 0.6697 & 0.4039 & 0.1892 & 0.0490 & 0 \\ 1.2427 & 0.9589 & 0.6697 & 0.4039 & 0.1892 & 0.0490 \end{pmatrix}^T$$

= first row of $\begin{pmatrix} 0.0256 & 0.0817 & 0.1349 & 0.1654 & 0.1646 & 0.1317 \\ -0.0172 & -0.0274 & 0.0001 & 0.0485 & 0.1061 & 0.1646 \\ -0.0099 & -0.0467 & -0.0688 & -0.0334 & 0.0485 & 0.1654 \\ -0.0048 & -0.0230 & -0.0609 & -0.0688 & 0.0001 & 0.1349 \\ -0.0017 & -0.0084 & -0.0230 & -0.0467 & -0.0274 & 0.0817 \\ -0.0003 & -0.0017 & -0.0048 & -0.0099 & -0.0172 & 0.0256 \end{pmatrix}$

$K = (0.0256 \quad 0.0817 \quad 0.1349 \quad 0.1654 \quad 0.1646 \quad 0.1317)$

Expression for control law is given by,
$$\Delta u(t) = K(w - f)$$
=

$$(0.0256 \quad 0.0817 \quad 0.1349 \quad 0.1654 \quad 0.1646 \quad 0.1317) \left(\begin{pmatrix} w(t+1) \\ w(t+2) \\ w(t+3) \\ w(t+4) \\ w(t+5) \\ w(t+6) \end{pmatrix} - \begin{pmatrix} 0.0485\Delta u(t-1) + 2.855 y(t) - 2.8369 y(t-1) + 0.9672 y(t-2) \\ 0.1392\Delta u(t-1) + 5.3982 y(t) - 7.1738 y(t-1) + 2.7756 y(t-2) \\ 0.2618\Delta u(t-1) + 8.3173 y(t) - 12.5385 y(t-1) + 5.2212 y(t-2) \\ 0.4034\Delta u(t-1) + 11.3294 y(t) - 18.3740 y(t-1) + 8.0446 y(t-2) \\ 0.5494\Delta u(t-1) + 14.1378 y(t) - 24.0958 y(t-1) + 10.9580 y(t-2) \\ 0.6856\Delta u(t-1) + 16.4752 y(t) - 29.1496 y(t-1) + 13.6743 y(t-2) \end{pmatrix} \right)$$

$$=$$

$$(0.0256 \quad 0.0817 \quad 0.1349 \quad 0.1654 \quad 0.1646 \quad 0.1317) \begin{pmatrix} w(t+1) - 0.0485\,\Delta u(t-1) - 2.855\,y(t) + 2.8369\,y(t-1) - 0.9672\,y(t-2) \\ w(t+2) - 0.1392\,\Delta u(t-1) - 5.3982\,y(t) + 7.1738\,y(t-1) - 2.7756\,y(t-2) \\ w(t+3) - 0.2618\,\Delta u(t-1) - 8.3173\,y(t) + 12.5385\,y(t-1) - 5.2212\,y(t-2) \\ w(t+4) - 0.4034\,\Delta u(t-1) - 11.3294\,y(t) + 18.3740\,y(t-1) - 8.0446\,y(t-2) \\ w(t+5) - 0.5494\,\Delta u(t-1) - 14.1378\,y(t) + 24.0958\,y(t-1) - 10.9580\,y(t-2) \\ w(t+6) - 0.6856\,\Delta u(t-1) - 16.4752\,y(t) + 29.1496\,y(t-1) - 13.6743\,y(t-2) \end{pmatrix}$$

$$=$$

$$\begin{pmatrix} 0.0256\,w(t+1) - 0.0012416\,\Delta u(t-1) - 0.073088\,y(t) + 0.07262464\,y(t-1) - 0.02476032\,y(t-2) + \\ 0.0817\,w(t+2) - 0.01137264\,\Delta u(t-1) - 0.44103294\,y(t) + 0.58609946\,y(t-1) - 0.22676652\,y(t-2) + \\ 0.1349\,w(t+3) - 0.03531682\,\Delta u(t-1) - 1.12200377\,y(t) + 1.69144365\,y(t-1) - 0.70433988\,y(t-2) + \\ 0.1654\,w(t+4) - 0.06672236\,\Delta u(t-1) - 1.87388276\,y(t) + 3.0390596\,y(t-1) - 1.33057684\,y(t-2) + \\ 0.1646\,w(t+5) - 0.09043124\,\Delta u(t-1) - 2.32708188\,y(t) + 3.96616868\,y(t-1) - 1.8036868\,y(t-2) + \\ 0.1317\,w(t+6) - 0.09029352\,\Delta u(t-1) - 2.16978384\,y(t) + 3.83900232\,y(t-1) - 1.80090531\,y(t-2) \end{pmatrix}$$

$$\Delta u(t) =$$

$$\begin{pmatrix} -0.29537818 \quad \Delta u(t-1) - 8.00687319 \quad y(t) + 13.19439835 \quad y(t-1) - 5.89103567 \quad y(t-2) + \\ 0.0256\,w(t+1) + 0.0817\,w(t+2) + 0.1349\,w(t+3) + 0.1654\,w(t+4) + 0.1646\,w(t+5) + 0.1317\,w(t+6) \end{pmatrix}$$

Note: A similar calculation is carried out for prediction horizons 5, 7, 8 & 9 with a range of weighting factors λ and the comparison is made to extract the one with best pair of weighting factors and prediction horizon.

The output of GPC yields to the control component $\delta_{\alpha\beta}$, which is used as reference for modulation.

4.2. T-TYPE INVERTER SYSTEM WITH INDIVIDUAL VOLTAGE SOURCES

In this case separate dc voltage sources of each 200 V is used at the dc link instead of capacitors, so that there is no necessity of using a separate control strategy for balancing the dc link capacitor voltages. Figure 4.2 shows the block diagram of the T-type inverter system, when individual dc voltage sources are used. The control signal δ_{abc}, obtained from the GPC-strategy, discussed in the section 4.1 is first transformed to $\delta_{\alpha\beta}$, which is then transformed to δ_{gh} using the transformations (17) & (18) and normalized to $\frac{(n-1)}{v_{dc}}$, where n(=3) is the number of levels of the inverter & v_{dc} (=v_{dc1}+v_{dc2}=400 V) is the DC source voltage. It is to be noted that as δ_γ is not needed here in the case of T-type inverter system with individual voltage sources. Hence, it is neglected.

$$T_{abc}^{\alpha\beta\gamma} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{17}$$

$$T_{\alpha\beta}^{gh} = \begin{bmatrix} 1 & \frac{-2}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \tag{18}$$

(17) is the power variant form of Clarke's transformation, where the gain is $\sqrt{\frac{2}{3}}$. In ordinary Clarke's transformation the gain is 2/3. In order to make the transformation matrix unitary i.e.

19

the inverse matrix coincides with its transpose and to preserve the active and reactive power one has to consider power invariant form of Clarke's transformation.
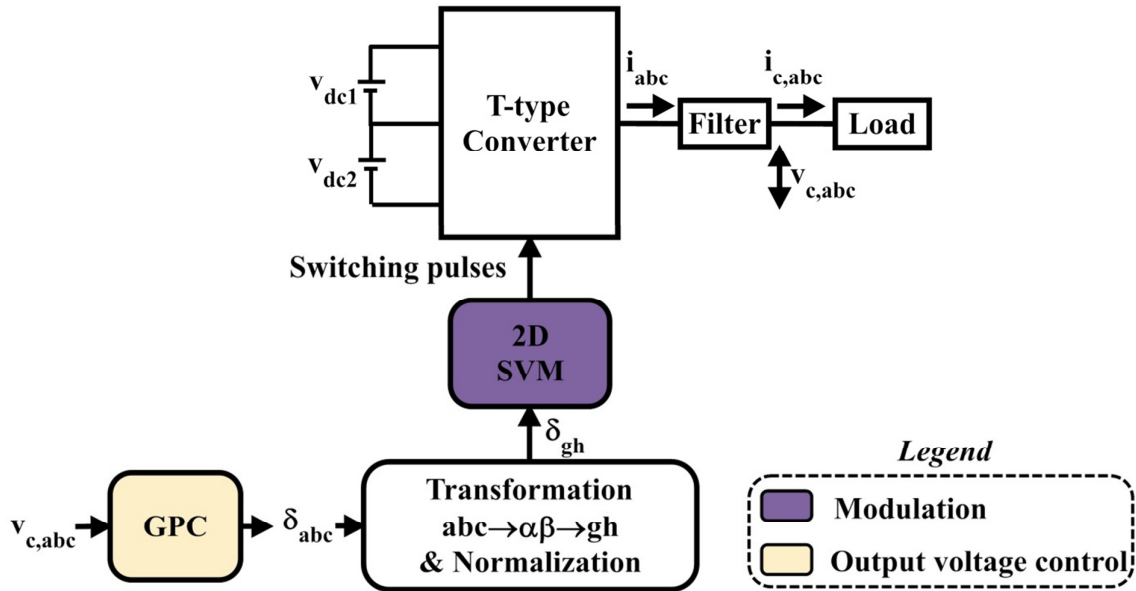
Fig. 4.2. Block diagram of the T-type inverter system with separate dc voltage sources

Once the control signal (or reference for modulator), δ_{gh} is obtained, it is sent to the modulator to get the firing pulses for the semiconductor switches. The modulation strategy used here is two-dimensional SVM [11]. This involves finding the nearest three coordinates in the two-dimensional space vector coordinate system and switching the corresponding vectors, with their respective duty cycles. It is done by rounding the values and doing a simple comparison in the two dimensional coordinate system. After finding the diagonal vectors of the parallelogram, another simple comparison is done to find if the reference, δ_{gh} is in the upper triangle or in the lower triangle, as shown in the figure 4.3. Once all the three coordinates in the g-h coordinate system are obtained, the duty cycles are computed and the switching pulses are generated for the IGBT switches. Figure 4.4 shows the 2D SVM algorithm.
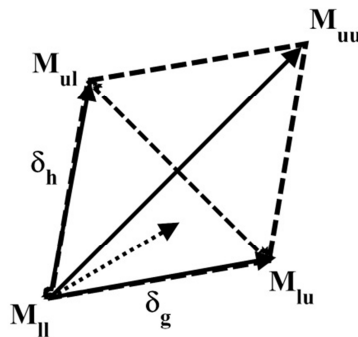
Fig. 4.3. Parallelogram comprising two equal triangles
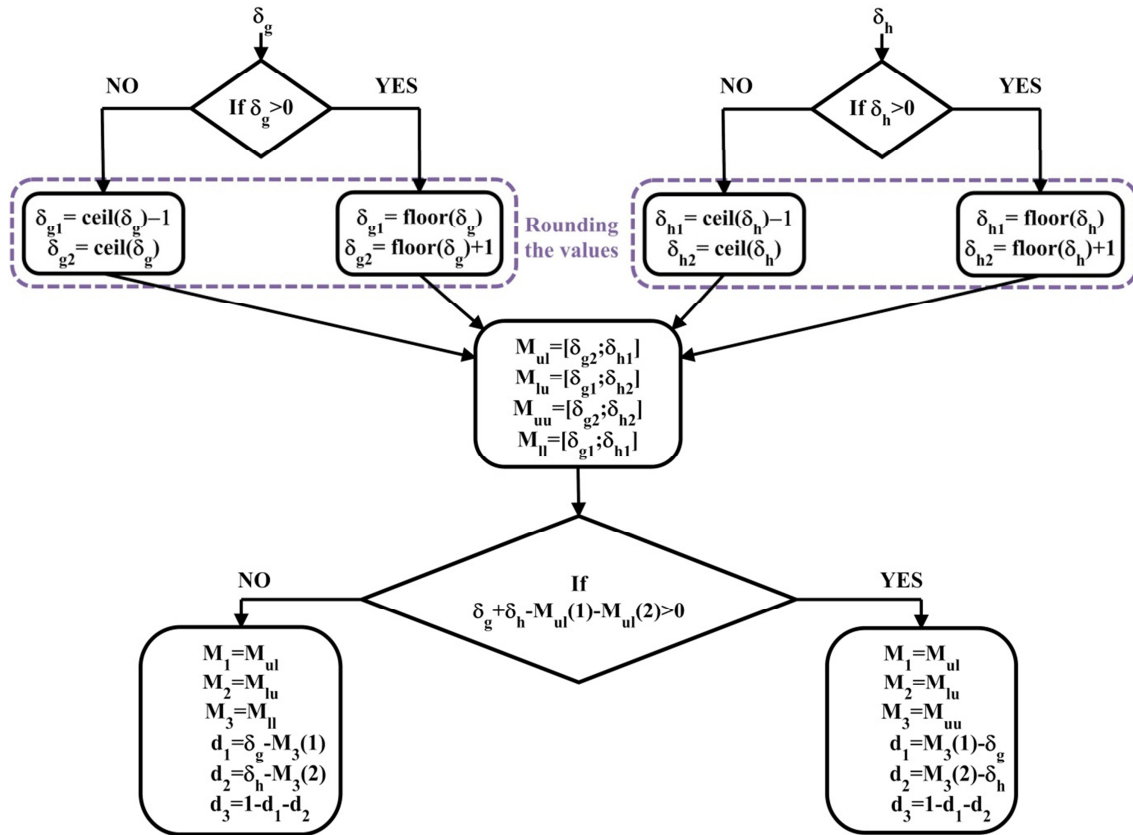
Fig. 4.4. Two dimensional Space Vector Modulation algorithm

It is to be noted that the two dimensional SVM is very fast and computationally efficient, which can be extended to n-level three phase converters. Figure 4.5 shows the reference and the actual output voltage of GPC control during simulation, which reveals the efficiency in tracking the reference and the performance of GPC to tackle the mismatch of model parameter.
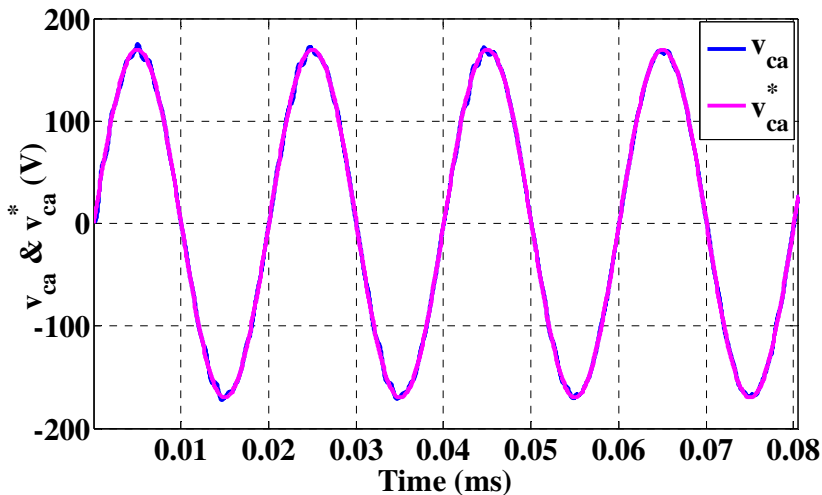
Fig. 4.5 Output voltage-reference and controlled waveforms for the T-type inverter system with individual dc voltage sources

21

4.3. T-TYPE INVERTER SYSTEM USING INDIVIDUAL DC LINK CAPACITORS

In this case the dc sources are replaced by separate dc link capacitors and this needs a separate control strategy for balancing the dc link capacitor voltages. The efficiency of the control strategy relies on system performance parameters like computational effort, harmonic reduction and good tracking of the output voltage. There are two dc link capacitor voltage balancing approaches i.e. the redundancy approach and the deterministic approach, whose performances are simulated and compared.

4.3.1. REDUNDANCY DC LINK CAPACITOR VOLTAGE BALANCING APPROACH

In this approach, an extra redundancy block is used, that facilitates a simple static comparison [70], [71], [72] of the dc link capacitor voltages and current as shown in the figure 4.6. According to this comparison result, the redundancy of the inner level switching vectors in a three level converter is used and appropriate switching is done as shown in the table 4.4. Figure 4.7 shows the possible switching states of a three level converter. The inverter has three states per phase and as there are three phases, 3^3=27 different switching states exists. It is to be noted that the redundancy exists in the inner level vectors- V_1, V_2, V_3, V_4, V_5 & V_6 in a three level space vector. For example- consider the vector V_7 (+, 0, -), which denotes that, phase a is connected to the positive terminal, phase b is connected to the dc link mid-point and phase c is connected to the negative terminal. In zero vector (V_0) the magnitude of voltage is 0V. In the internal vectors (V_1 to V_6) the magnitude of voltage is $\frac{v_{dc}}{3}$ V. The middle vectors (V_7 to V_{12}) have magnitude of $\frac{v_{dc}}{\sqrt{3}}$V, whereas the external vectors (V_{13} to V_{18}) have the magnitude of $\frac{2v_{dc}}{\sqrt{3}}$V.
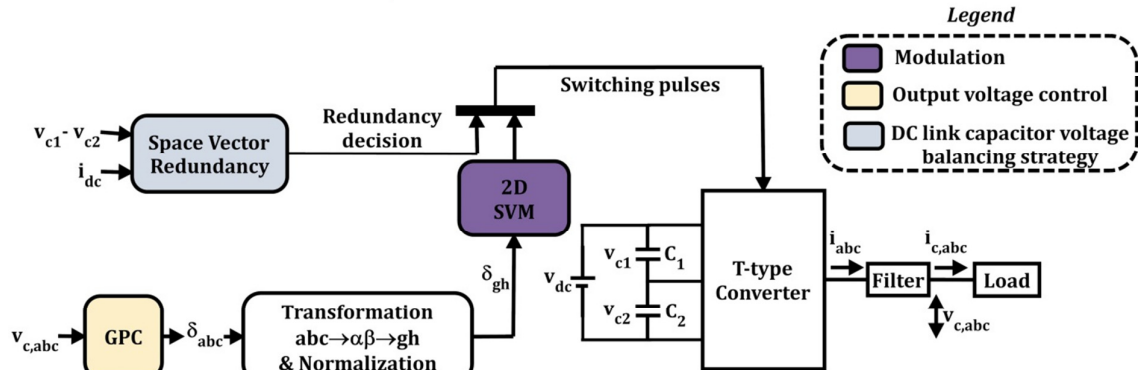
Fig. 4.6. Block diagram of the T-type inverter system with redundancy dc link capacitor voltage balancing approach

Table 4.4 Redundancy control strategy to balance the dc link capacitor voltages

Voltage imbalance	DC link current	Internal redundancy
$(v_{c1}-v_{c2}) < 0$	$i_{dc} < 0$	Positive redundancy (0)
	$i_{dc} > 0$	Negative redundancy (1)
$(v_{c1}-v_{c2}) > 0$	$i_{dc} < 0$	Negative redundancy (1)
	$i_{dc} < 0$	Positive redundancy (0)
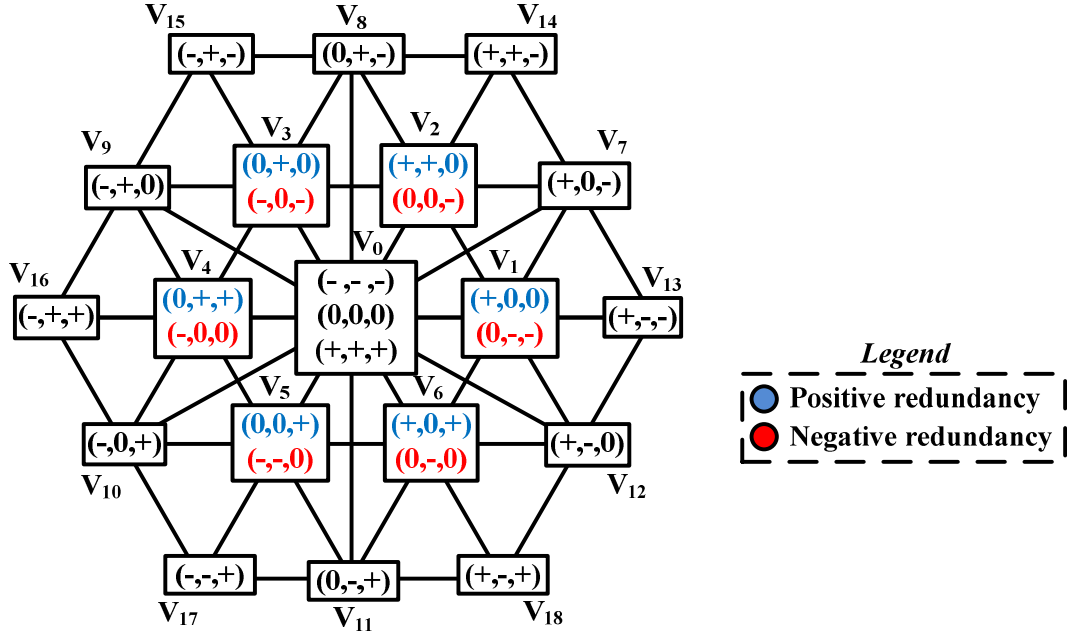
Fig. 4.7. Switching state vectors of a three level converter

It is to be noted that a two-dimensional SVM is used, as discussed in the section 4.2. The GPC strategy used is the same as the one discussed in section 4.1. On performing a series of simulation experiments, it is found that the GPC performs well when prediction horizon, N_h=6 and weighting factor, λ=0.242. This performance of the system is assessed by the Root Mean Square (RMS_{error}) and Total Harmonic Distortion (THD) values, which are discussed in section 4.4.

The RMS_{error} is given by,

$$RMS_{error}(\%) = \frac{RMS(v_{c,abc}-v_{c,abc}^*)}{v_{c,abc}^*|RMS} \times 100 \%$$

where $v_{c,abc}$ is the actual output voltage

$v_{c,abc}^*$ is the reference output voltage &

$v_{c,abc}^*|RMS$ is the RMS voltage reference =120 V, 50 Hz
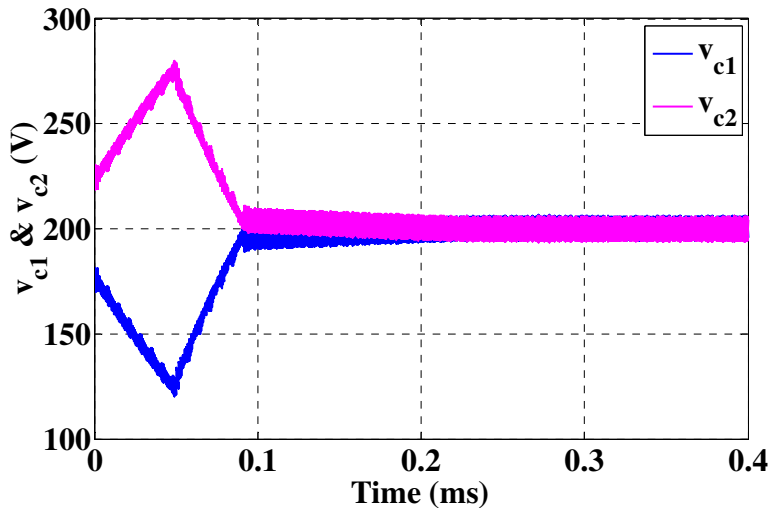
Fig. 4.8 DC link capacitor voltages v_{c1} & v_{c2} balanced by redundancy approach with initial imbalance condition
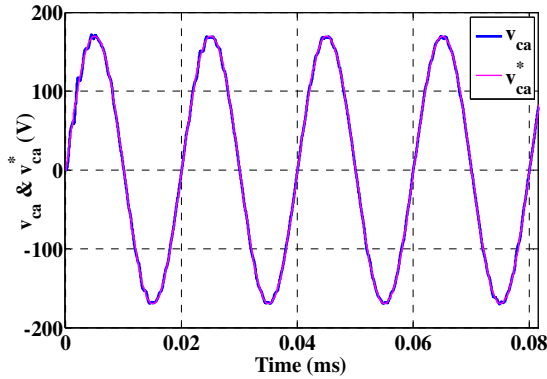
Fig. 4.9 Output voltage-reference and controlled waveforms for Redundancy approach
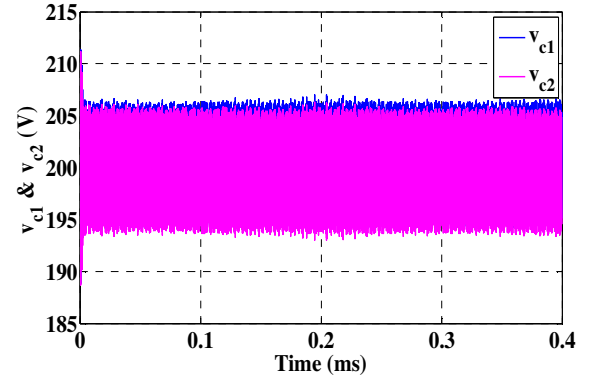
Fig. 4.10 DC link capacitor voltages v_{c1} & v_{c2} for redundancy approach

Figure 4.8 shows that an initial imbalance condition of dc link capacitor voltages is enforced and after some time instant the redundancy approach is activated. The capability of the approach to handle the imbalance situation and balance it later within the given stipulated time is observed. Figure 4.9 shows the GPC tracking the output reference voltage. Figure 4.10 depicts the balanced dc link capacitor voltages. Although this approach is simple with less computational efforts, it has its own drawbacks like high RMS$_{error}$ values and THD values of the output voltage & existence of lower order harmonics in the dc link capacitor voltage difference which are overcome by the deterministic dc link capacitor voltage balancing approach. The comparisons of these strategies are discussed in detail in section 4.4.

4.3.2. DETERMINISTIC DC LINK CAPACITOR VOLTAGE BALANCING APPROACH

Two serious problems in NPC and NPP converters are the capacitor voltage balancing issue and the sinusoidal disturbances in the dc link capacitors during switching. Such disturbances have pulled researcher's interest, which are encountered by basic control system design. Although many dc link capacitor voltage balancing approaches were found in literature [73], [74], still focus prevails on eradicating other issues along with balancing dc link capacitors.

The control component, δ_γ serves a freedom degree for solving the capacitor voltage imbalance and the reduction of the low-frequency oscillations. The deterministic approach of dc-link capacitor voltage balancing approach is based on using a state observer, called Luenberger observer [75], which estimates the sinusoidal oscillation at each sampling instant and minimizes certain level of lower order harmonics of dc link capacitor voltage difference, thereby regulating the dc link capacitor voltages [18].

The application of such control strategy couldn't be possible unless we model the converter and derive the phase current dynamics and the dc link capacitor voltage difference dynamics, which are effectively used in the deterministic approach [76]. Such parameter aids the controller and observer to keep the output voltage to go allied with the deterministic control approach.

The block diagram consists mainly of an output voltage control block (GPC), dc link capacitor voltage balancing block and the modulation block, which is depicted in the figures 4.11 & 4.12. The difference between these two figures is, in 3D FFSVM the real values of the dc link capacitor voltages are considered, which is discussed in detail in the modulation part of this section.

24
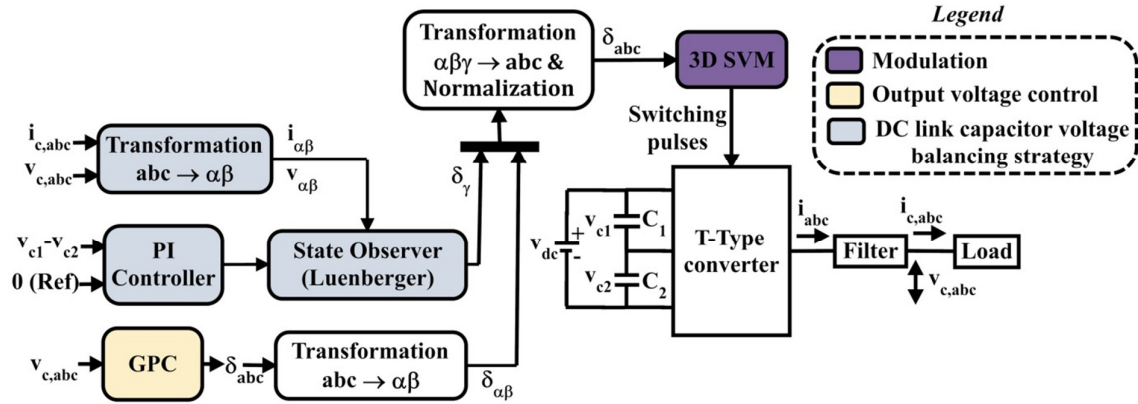
Fig. 4.11. Block diagram of deterministic dc link capacitor voltage balancing approach using 3D SVM
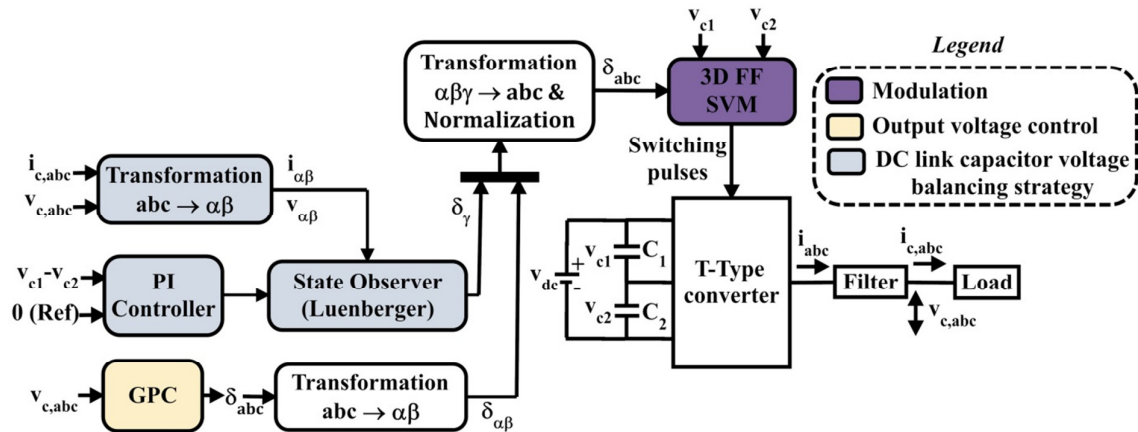
Fig. 4.12. Block diagram of deterministic dc link capacitor voltage balancing approach using 3D FFSVM

In order to model the converter, the three level equivalent circuit model of T-type power inverter is considered with the ideal switches [77], as shown in the figure 4.13.

Table 4.5 Model parameters used in the equivalent ideal switch

Variable	Description
v_{dc}	Source voltage
i_{dc}	dc-link current
C_1, C_2	dc-link capacitance
L	Filter inductance
C_f	Filter capacitance
i_{dc1}, i_{dc2}, i_{dc3}	Currents at top, middle and bottom connection points of capacitors
v_{abc}	Injected voltage referred to 'B'
i_{abc}	Inductor currents
δ_{abc}	Switching position
R_L	Load resistance
L_L	Load inductance
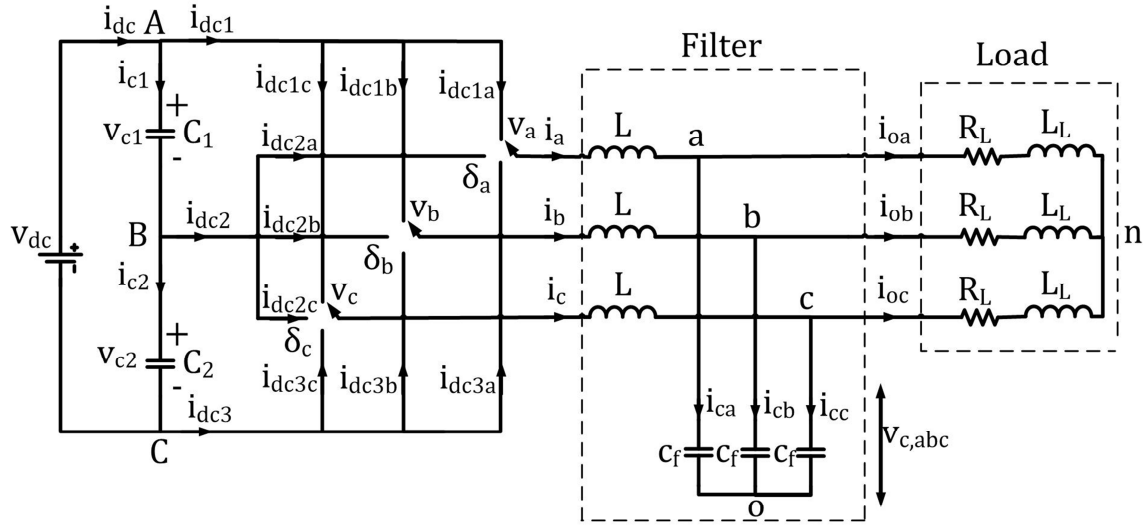
Fig. 4.13. Equivalent circuit of a 3L T-type converter with ideal switches

Table 4.5 shows the model parameters of the equivalent ideal switch.

By applying KCL,

$$i_{dc1} + i_{c1} = i_{dc} \rightarrow i_{dc1} = i_{dc} - i_{c1} \tag{19}$$

$$i_{dc2} + i_{c2} = i_{c1} \rightarrow i_{dc2} = i_{c1} - i_{c2} \tag{20}$$

$$i_{dc3} + i_{dc} = i_{c2} \rightarrow i_{dc3} = i_{c2} - i_{dc} \tag{21}$$

$$i_{dc1} + i_{dc2} + i_{dc3} = 0 \tag{22}$$

where

$$C_1 = C_2 = C$$

$$i_{C1} = C\frac{dv_{c1}}{dt}$$

$$i_{C2} = C\frac{dv_{c2}}{dt}$$

Subtracting equation (19) from (21),

$$i_{c1} + i_{c2} = i_{dc3} - i_{dc1} + 2i_{dc} \tag{23}$$
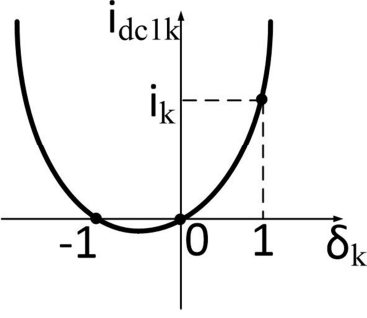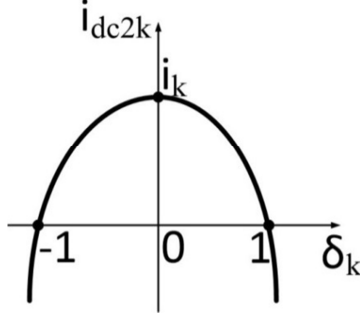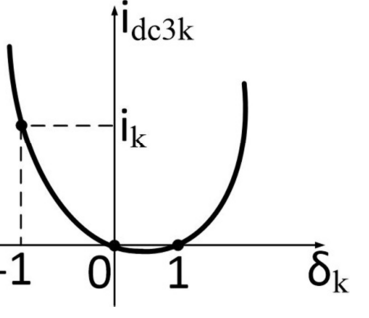
$$(20) \quad \rightarrow i_{c1} - i_{c2} = i_{dc2}$$

A relationship between the currents i_{dc1k}, i_{dc2k}, i_{dc3k} in terms of the three possible switch positions δ_k and for every $k \in \{a, b, c\}$ is established, where i_{dc1k}, i_{dc2k}, i_{dc3k} are the input current flowing towards the switches from the dc link capacitors connected to a DC voltage source as shown in the figure 4.13. Thus, for a given $k \in \{a, b, c\}$ three points are known, and a quadratic function relating i_{dc1k}, i_{dc2k}, i_{dc3k} and δ_k can be designed to fit all three points as shown in table 4.6.

Note: The above equivalent circuit is similar for a three level converter, in general.

Table 4.6 Resolving the input currents flowing towards the switches into quadratic function

$i_{dc1k} = (\delta_k + 1)\dfrac{\delta_k i_k}{2}$ for k ∈ {a, b, c}	$i_{dc2k} = (1 - \delta_k^2)i_k$ for k ∈ {a, b, c}	$i_{dc3k} = (\delta_k - 1)\dfrac{\delta_k i_k}{2}$ for k ∈ {a, b, c}
$i_{dc1} = (\delta_a + 1)\dfrac{\delta_a i_a}{2} +$ $(\delta_b + 1)\dfrac{\delta_b i_b}{2} +$ $(\delta_c + 1)\dfrac{\delta_c i_c}{2}$ (24)	$i_{dc2} = (1 - \delta_a^2)i_a +$ $(1 - \delta_b^2)i_b + (1 - \delta_c^2)i_c$ $= -\delta_a^2 i_a - \delta_b^2 i_b - \delta_c^2 i_c$ (25) Since $i_a + i_b + i_c = 0$	$i_{dc3} = (\delta_a - 1)\dfrac{\delta_a i_a}{2} +$ $(\delta_b - 1)\dfrac{\delta_b i_b}{2} +$ $(\delta_c - 1)\dfrac{\delta_c i_c}{2}$ (26)

Substituting (24), (25) & (26) in (20) & (23),

$$C\frac{dx_1}{dt} = C\frac{dv_{c1}}{dt} + C\frac{dv_{c2}}{dt} = -\delta_a i_a - \delta_b i_b - \delta_c i_c + 2i_{dc} \tag{27}$$

$$C\frac{dx_2}{dt} = C\frac{dv_{c1}}{dt} - C\frac{dv_{c2}}{dt} = -\delta_a^2 i_a - \delta_b^2 i_b - \delta_c^2 i_c \tag{28}$$

where $x_2 = v_{c1}-v_{c2}$ &

$\quad x_1 = v_{c1}+v_{c2}$

Applying power invariant form of Clarke's transformation (17) to (27) & (28),

(27)→
$$C\dot{x}_1 = -\delta_{abc}^T i_{abc} + 2i_{dc}$$
$$C\dot{x}_1 = -(T^{-1}\delta_{\alpha\beta\gamma})^T T^{-1}i_{\alpha\beta\gamma} + 2i_{dc}$$
$$C\dot{x}_1 = -\delta_{\alpha\beta}^T i_{\alpha\beta} + 2i_{dc}$$

As $i_a + i_b + i_c = 0 \rightarrow i_\gamma = 0$, the gamma component is removed.

As the value $\dot{x}_1$ becomes zero, since $v_{c1} + v_{c2}$ is always constant, the above equation can be written as,

$$\boldsymbol{i_{dc}} = \frac{\delta_{\alpha\beta}^T i_{\alpha\beta}}{2} \tag{29}$$

(28)→
$$C\dot{x}_2 = -[\delta_a^2 \ \delta_b^2 \ \delta_c^2]i_{abc}$$
$$C\dot{x}_2 = -[\delta_a^2 \ \delta_b^2 \ \delta_c^2]T^{-1}i_{\alpha\beta\gamma}$$
$$C\dot{x}_2 = -\sqrt{\frac{2}{3}}[\delta_a^2 - \frac{(\delta_b^2 + \delta_c^2)}{2} \quad \frac{\sqrt{3}}{2}(\delta_b^2 - \delta_c^2) \quad \frac{1}{\sqrt{2}}(\delta_a^2 + \delta_b^2 + \delta_c^2)]i_{\alpha\beta\gamma}$$
$$\boldsymbol{C\dot{x}_2 = -\frac{1}{\sqrt{6}}[\delta_\alpha^2 - \delta_\beta^2 \quad - 2\delta_\alpha\delta_\beta]i_{\alpha\beta} - \frac{2}{\sqrt{3}}\delta_{\delta\beta}^T i_{\alpha\beta}\delta_\gamma} \tag{30}$$

where

27

$$T = \sqrt{\frac{2}{3}}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}; \qquad T^{-1} = T^T; \qquad T.T^{-1} = I_3$$

$$\delta_a = \sqrt{\frac{2}{3}}(\delta_\alpha + \frac{\delta_\gamma}{\sqrt{2}}); \ \delta_b = \sqrt{\frac{2}{3}}(-\frac{\delta_\alpha}{2} + \frac{\sqrt{3}}{2}\delta_\beta + \frac{\delta_\gamma}{\sqrt{2}}) \ \& \ \delta_c = \sqrt{\frac{2}{3}}(-\frac{\delta_\alpha}{2} - \frac{\sqrt{3}}{2}\delta_\beta + \frac{\delta_\gamma}{\sqrt{2}})$$

It is to be noted that the values δ_a, δ_b & δ_c are obtained by simply taking the inverse matrix of the transformation (17).

Applying KVL in figure 4.13,

$$v_{aB} = L\frac{di_a}{dt} + v_{aO} + v_{OB} \tag{31}$$

$$v_{bB} = L\frac{di_b}{dt} + v_{bO} + v_{OB} \tag{32}$$

$$v_{cB} = L\frac{di_c}{dt} + v_{cO} + v_{OB} \tag{33}$$

Since, the voltages v_{aO}, v_{bO} & v_{cO} are equilibrated and no 4th wire is considered in the system, we have

$$v_{aO} + v_{bO} + v_{cO} = 0 \tag{34}$$

$$i_a + i_b + i_c = 0 \tag{35}$$

Substituting (34) & (35) in (31), (32) & (33) and adding, we get

$$v_{OB} = \frac{1}{3}(v_{aB} + v_{bB} + v_{cB}) \tag{36}$$

It is to be noted that voltage v_{abcB} represents the voltage between the switches and the terminal B, when the corresponding switches are closed. Both the voltages v_{abcO} & $v_{c,abc}$ represents the output voltage across the filter capacitor.

Substituting (36) in (31), (32) & (33) and combining them, we get

$$\begin{bmatrix} v_{aO} \\ v_{bO} \\ v_{cO} \end{bmatrix} = -L\begin{bmatrix} \frac{di_a}{dt} \\ \frac{di_b}{dt} \\ \frac{di_c}{dt} \end{bmatrix} + \frac{1}{3}\begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}\begin{bmatrix} v_{aB} \\ v_{bB} \\ v_{cB} \end{bmatrix} \tag{37}$$

The above equation can be written as,

$$L\frac{di_{abc}}{dt} = Rv_{abcB} - v_{abcO} \tag{38}$$

Applying Clarke's transformation to the above equation, we get

$$L\frac{di_{\alpha\beta}}{dt} = -v_{\alpha\beta O} + v_{\alpha\beta B} \tag{39}$$

where, $R = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}$ & $TRT^{-1} = diag\{1,1,0\}$;

As $v_{aO} + v_{bO} + v_{cO} = 0 \rightarrow v_{\gamma O} = 0$, the gamma component is removed.

Applying power invariant form of Clarke's transformation to the term v_{abcB} in (38),

$$v_{\alpha\beta B} = T\, v_{abcB}$$

$$= \sqrt{\frac{2}{3}}\begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix}\begin{pmatrix} v_{aB} \\ v_{bB} \\ v_{cB} \end{pmatrix}$$

$$v_{\alpha\beta B} = \sqrt{\frac{2}{3}}\begin{pmatrix} v_{aB} - (\frac{v_{bB}+v_{cB}}{2}) \\ \frac{\sqrt{3}}{2}(v_{aB} - v_{cB}) \end{pmatrix} \tag{40}$$

It is to be noted that, as there is no γ-term in $v_{\alpha\beta B}$, the last row in the above transformation matrix is removed.

The switching voltages are represented by the below quadratic function, that fits all the three states,

$$\begin{bmatrix} v_{aB} \\ v_{bB} \\ v_{cB} \end{bmatrix} = \frac{v_{c1}-v_{c2}}{2} \begin{bmatrix} \delta_a^2 \\ \delta_b^2 \\ \delta_c^2 \end{bmatrix} + \frac{v_{c1}+v_{c2}}{2} \begin{bmatrix} \delta_a \\ \delta_b \\ \delta_c \end{bmatrix} \tag{41}$$

Substituting (41) in (40),

$$v_{\alpha\beta B} = \sqrt{\frac{2}{3}} \begin{pmatrix} \delta_a^2 - (\frac{\delta_b^2+\delta_c^2}{2}) & \delta_a - (\frac{\delta_b+\delta_c}{2}) \\ \frac{\sqrt{3}}{2}(\delta_b^2 - \delta_c^2) & \frac{\sqrt{3}}{2}(\delta_b - \delta_c) \end{pmatrix} \begin{pmatrix} \frac{x_2}{2} \\ \frac{x_1}{2} \end{pmatrix}$$

Substituting $\delta_a = \sqrt{\frac{2}{3}}(\delta_\alpha + \frac{\delta_\gamma}{\sqrt{2}})$; $\delta_b = \sqrt{\frac{2}{3}}(-\frac{\delta_\alpha}{2} + \frac{\sqrt{3}}{2}\delta_\beta + \frac{\delta_\gamma}{\sqrt{2}})$ & $\delta_c = \sqrt{\frac{2}{3}}(-\frac{\delta_\alpha}{2} - \frac{\sqrt{3}}{2}\delta_\beta + \frac{\delta_\gamma}{\sqrt{2}})$ in the above equation, we get

$$v_{\alpha\beta B} = \sqrt{\frac{2}{3}} \begin{pmatrix} \sqrt{2}\delta_\alpha\delta_\gamma + \frac{(\delta_\alpha^2-\delta_\beta^2)}{2} & \sqrt{\frac{3}{2}}\delta_\alpha \\ \sqrt{2}\delta_\beta\delta_\gamma - \delta_\alpha\delta_\beta & \sqrt{\frac{3}{2}}\delta_\beta \end{pmatrix} \begin{pmatrix} \frac{x_2}{2} \\ \frac{x_1}{2} \end{pmatrix}$$

$$v_{\alpha\beta B} = \begin{pmatrix} \frac{\delta_\alpha\delta_\gamma}{\sqrt{3}} + \frac{(\delta_\alpha^2-\delta_\beta^2)}{2\sqrt{6}} & \frac{\delta_\alpha}{2} \\ \frac{\delta_\beta\delta_\gamma}{\sqrt{3}} - \frac{\delta_\alpha\delta_\beta}{\sqrt{6}} & \frac{\delta_\beta}{2} \end{pmatrix} \begin{pmatrix} x_2 \\ x_1 \end{pmatrix} \tag{42}$$

It is to be noted that the values δ_a, δ_b & δ_c are obtained by simply taking the inverse matrix of the transformation(17).

Substituting (42) in (39),

$$L\frac{di_{\alpha\beta}}{dt} = -v_{\alpha\beta O} + \begin{pmatrix} \frac{\delta_\alpha\delta_\gamma}{\sqrt{3}} + \frac{(\delta_\alpha^2-\delta_\beta^2)}{2\sqrt{6}} & \frac{\delta_\alpha}{2} \\ \frac{\delta_\beta\delta_\gamma}{\sqrt{3}} - \frac{\delta_\alpha\delta_\beta}{\sqrt{6}} & \frac{\delta_\beta}{2} \end{pmatrix} \begin{pmatrix} x_2 \\ x_1 \end{pmatrix}$$

$$L\frac{di_{\alpha\beta}}{dt} = -v_{\alpha\beta O} + \frac{1}{2}x_1\delta_{\alpha\beta} + \begin{pmatrix} \frac{\delta_\alpha\delta_\gamma}{\sqrt{3}} + \frac{(\delta_\alpha^2-\delta_\beta^2)}{2\sqrt{6}} \\ \frac{\delta_\beta\delta_\gamma}{\sqrt{3}} - \frac{\delta_\alpha\delta_\beta}{\sqrt{6}} \end{pmatrix} x_2 \tag{43}$$

From (29), (30) & (43),
The simplified dc link capacitor voltage dynamic equations are given by,

$$\boxed{\begin{aligned} C\dot{x}_2 &= -\frac{1}{\sqrt{6}}[\delta_\alpha^2 - \delta_\beta^2 \quad -2\delta_\alpha\delta_\beta]i_{\alpha\beta} - \frac{2}{\sqrt{3}}\delta_{\delta\beta}^T i_{\alpha\beta}\delta_\gamma \\ i_{dc} &= \frac{\delta_{\alpha\beta}^T i_{\alpha\beta}}{2} \end{aligned}}$$

The inductor current dynamics is given by,

$$\boxed{L\frac{di_{\alpha\beta}}{dt} = -v_{\alpha\beta O} + \frac{1}{2}x_1\delta_{\alpha\beta} + \begin{pmatrix} \frac{\delta_\alpha\delta_\gamma}{\sqrt{3}} + \frac{(\delta_\alpha^2-\delta_\beta^2)}{2\sqrt{6}} \\ \frac{\delta_\beta\delta_\gamma}{\sqrt{3}} - \frac{\delta_\alpha\delta_\beta}{\sqrt{6}} \end{pmatrix} x_2}$$

As the capacitor voltage difference voltage issue is solved by the design of a control system comprising a controller and a Luenberger observer, our interest lies in using only the dc link capacitor voltage difference voltage dynamic equation.

The dc link capacitor voltage is now analyzed by singular perturbation method as discussed in [18] and the dc link capacitor voltage difference dynamic equation is simplified.

Since, the objective of the deterministic approach is to balance the dc link capacitor voltages, the emphasize lies on the dc link capacitor voltage difference dynamic equation (30).

During the simplification process, it is assumed, that the instantaneous power dynamics, which are the instantaneous values of current and voltage waveforms including transients states, as defined by *Akagi et al.* [78] are very faster than the dc-link capacitor voltage difference dynamics. The simplified dc link capacitor voltage difference dynamics is given by

$$C\dot{x}_2 = -k_d\delta_\gamma + \phi(t) \tag{44}$$

$$\text{where } k_d = \frac{4p}{\sqrt{3}V_{dc}} \tag{45}$$

k_d depends on the dynamic active power. This value should be calculated online but p should be saturated to a minimum value, so that a controlled dynamic active power is used in the deterministic approach. $\phi(t) = \mu_1 \sin(3.2\pi ft + 3\theta + \tan^{-1}(\mu_2))$ is the sinusoidal disturbance as derived in [18].

The constant k_d is used in the deterministic approach, where the dynamic active power, p is given by,

$$p = v_{aB}i_a + v_{bB}i_b + v_{cB}i_c = v_\alpha i_\alpha + v_\beta i_\beta \tag{46}$$

Care should be taken that the δ_γ component should not become infinity, because of very less value of k_d. Figure 4.14 shows the schematic block of the Luenberger integrated to the converter for balancing the dc-link capacitor voltage.
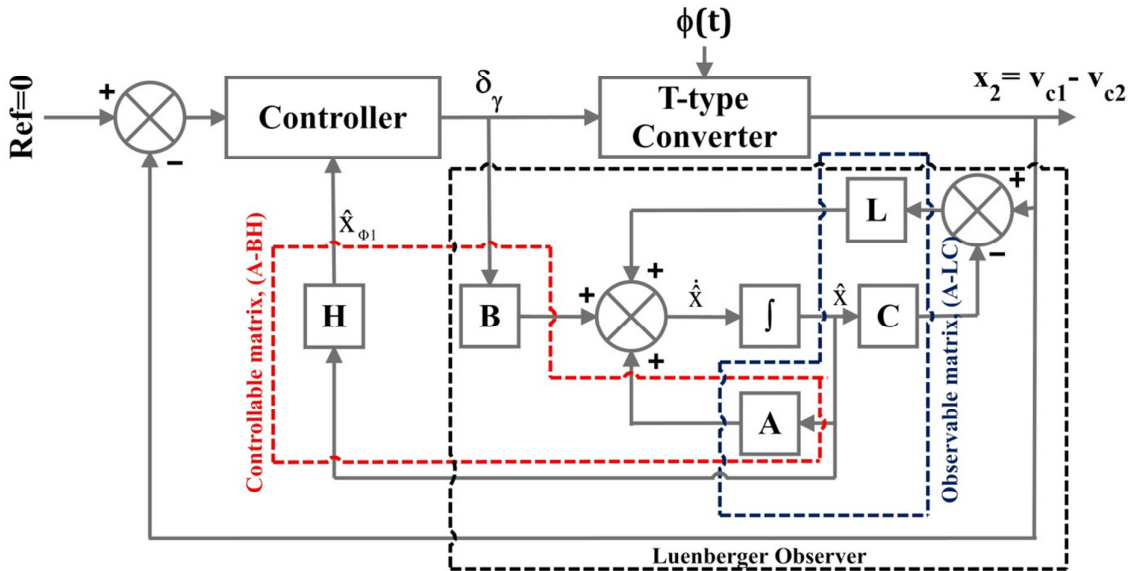
Fig. 4.14. Deterministic dc link capacitor voltage balancing approach

The Luenberger observer system, S_o is given by,

$$\dot{\hat{x}} = A\hat{x} + B\delta_\gamma + L(x_2 - \hat{y})$$
$$\hat{y} = C\hat{x} \tag{47}$$

where $A = \begin{pmatrix} 0 & \frac{1}{c} & 0 \\ 0 & 0 & 1 \\ 0 & -(3.2\pi.f)^2 & 0 \end{pmatrix}; B = \begin{pmatrix} -\frac{k_d}{c} \\ 0 \\ 0 \end{pmatrix}; C = \begin{pmatrix} 1 \\ 0 \\ 0 \end{pmatrix}^T$ & $H = (0 \quad 1 \quad 0)$ are the

matrices associated with the controller and observer.

$\hat{x} = (\hat{x}_2 \quad \hat{x}_{\phi 1} \quad \hat{x}_{\phi 2})^T$ is the sinusoidal disturbance estimated in the observer, f is the frequency of the system i.e. 50 Hz & c is the capacitance of the dc link capacitors.

The additional control component δ_γ is given by,

$$\delta_\gamma = -\frac{1}{k_d}\left[k_p(0-x_2) + k_i \int_0^t (0-x_2)\,d\tau + k_D\frac{d}{dt}(0-x_2) - \hat{x}_{\phi 1}\right] \qquad (48)$$

When δ_γ is written in Laplace transform,

$$\delta_\gamma(s) = -\frac{1}{k_d}\left[k_p + \frac{k_i}{s} + k_D s - \hat{x}_{\phi 1}(s)\right]$$

In order to make it less noisy and for practical implementation, it is quite common to modify the derivative term to an Low Pass Filter (LPF), as follows

$$\delta_\gamma(s) = -\frac{1}{k_d}\left[k_p + \frac{k_i}{s} + \frac{Nk_D}{1+\frac{N}{s}} - \hat{x}_{\phi 1}(s)\right] \qquad (49)$$

where k_p=1, k_i=1250 & k_D= 0 are the proportional, integral & derivative gain constants. N = 0 is the filter coefficient of the derivative term. These values are obtained by tuning of the PID controller. k_d as formulated in (45) depends on the dynamic active power p, which in turn depends on the load connected to the converter. Once the controller is established the Luenberger observer is integrated into the system. The observer gain matrix, L is a 3×1 matrix, whose values are obtained by pole-placement technique, such that the observer poles are faster than those of the system. So, the observer poles can be taken in multiples of 3 such that, -6ω, -9ω, -12ω, etc. depending on the disturbance and the system parameters. These pole values are tradeoff values obtained depending on the disturbance, application and system parameters. The observer poles or eigen values taken in our system is $S_{1,2,3}^O = -9*2*\pi*f$, where f is the frequency of the system, whose value is 50 Hz. The calculated observer gain matrix is $L = 10^7 \begin{pmatrix} 0.008 \\ 0.0051 \\ 3.3152 \end{pmatrix}$. The controller gain matrix is given by $B = \begin{pmatrix} -\frac{k_d}{c} \\ 0 \\ 0 \end{pmatrix}$ as explained in (47), whose value depends on the values of k_d and capacitance, c of the dc link capacitors. Once the sinusoidal disturbance, ϕ is estimated in the approximated model by the Luenberger observer, this estimate is then applied to asymptotically cancel the disturbance, thereby accomplishing the balancing of the dc-link capacitor voltages.

Once the $\delta_{\alpha\beta\gamma}$ values are obtained from the GPC and the deterministic control strategy, these values are normalized and transformed to abc-space and sent to the modulators. Two modulating techniques that contribute to this three-component controlled inverter approach are three dimensional and three dimensional feed-forward modulations.

In 3D-SVM the reference control component $\delta_{\alpha\beta\gamma}$ is transformed first to abc-space and then scaled/normalized by the factor $\sqrt{\frac{2}{3}}\left(\frac{V_{dc}}{n-1}\right)$, where n is the level of the multilevel converter.

In three-dimensional State Vector Modulation (3D-SVM), the normalized reference is made to swing on a three-dimensional space, where the tetrahedron is identified and the appropriate state vectors are switched with the corresponding switching times (duty cycles). This is done by rounding the values of the normalized values, u_{abc}. These rounded new values are abc, which are then used along with the normalized values, u_{abc} (can be called u_a, u_b & u_c separately for the individual three phases) for performing simple comparisons, as shown in figure 4.15. On the basis of comparison results, the cases A to F are identified and the corresponding space vector sequence and the switching times are used to switch the IGBT switches as depicted in the table 4.7.

It is to be noted that the coordinate (a,b,c) represent the different voltage levels of the dc link and they take the values between zero and n-1, where n is the number of levels in a multilevel converter. The duty cycles are also, only the functions of the reference vectors and the integral part of the reference vector coordinates. For the second half cycle the space vectors should be taken in the reverse sequence. It is also noted that, the behavior of a

balanced system without triplen harmonics using the 3D SVM makes the switching time of one of the four active vectors as zero and this problem can be reduced to the well-known 2D SVM situation.
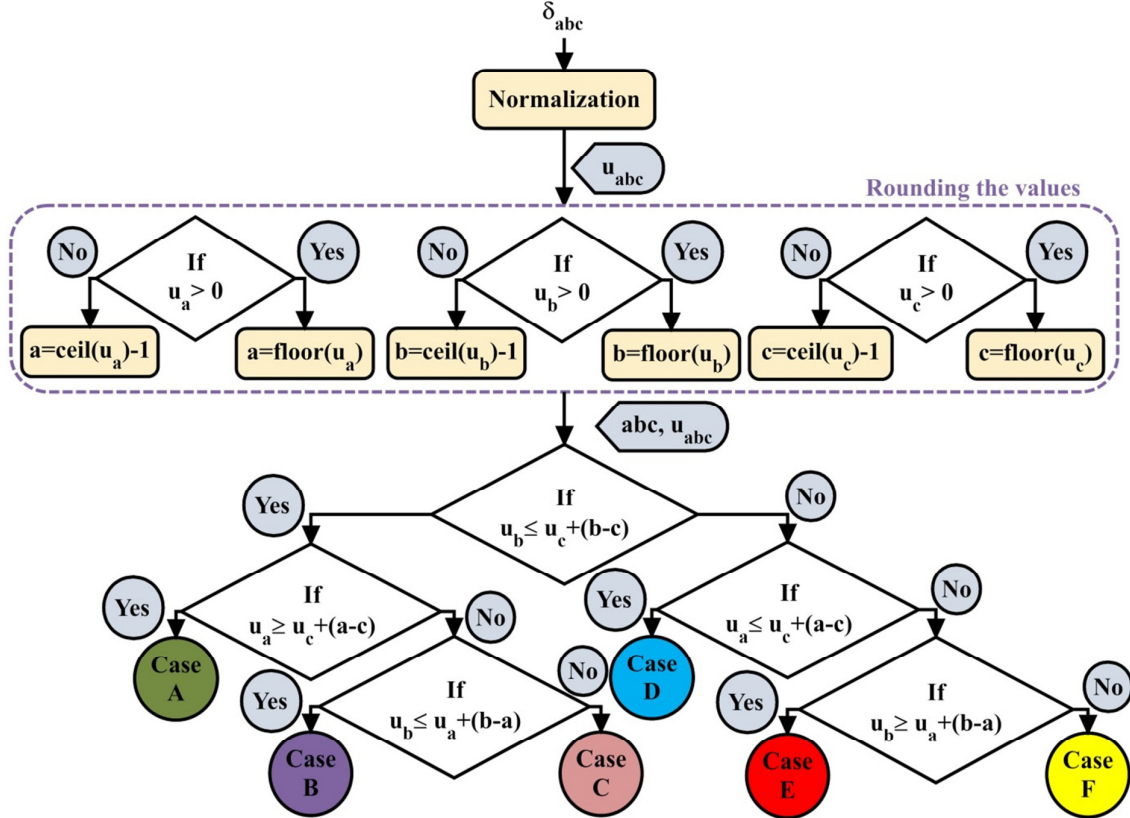
Fig. 4.15. 3D-SVM algorithm for selection of each tetrahedron for corresponding state vectors

Table 4.7 Space vector sequence & switching times for 3D-SVM

Cases	Space vector sequence												Switching times			
	S_a				S_b				S_c				D_1	D_2	D_3	D_4
	1	2	3	4	1	2	3	4	1	2	3	4	D_1	D_2	D_3	D_4
A	a	a+1	a+1	a+1	b	b	b	b+1	c	c	c+1	c+1	$1+a-u_a$	$-a+c+u_a-u_c$	$b-c-u_b+u_c$	$-b+u_b$
B	a	a	a+1	a+1	b	b	b	b+1	c	c+1	c+1	c+1	$1+c-u_c$	$a-c-u_a+u_c$	$-a+b+u_a-u_b$	$-b+u_b$
C	a	a	a	a+1	b	b	b+1	b+1	c	c+1	c+1	c+1	$1+c-u_c$	$b-c-u_b+u_c$	$a-b-u_a+u_b$	$-a+u_a$
D	a	a	a	a+1	b	b+1	b+1	b+1	c	c	c+1	c+1	$1+b-u_b$	$-b+c+u_b-u_c$	$a-c-u_a+u_c$	$-a+u_a$
E	a	a	a+1	a+1	b	b+1	b+1	b+1	c	c	c	c+1	$1+b-u_b$	$a-b-u_a+u_b$	$-a+c+u_a-u_c$	$-c+u_c$
F	a	a+1	a+1	a+1	b	b	b+1	b+1	c	c	c	c+1	$1+a-u_a$	$-a+b+u_a-u_b$	$-b+c+u_b-u_c$	$-c+u_c$

Simulation results reveal the performance of GPC to track the reference and tackle the model mismatch, resulting in minimized RMS_{error} and THD values, when compared to the redundancy approach, which are discussed in detail in section 4.4. Figure 4.16 shows the dc link capacitor voltages with an initial imbalance condition, which is then balanced using the deterministic-3D SVM method. Figure 4.17 shows the dc link capacitor voltages with an

initial imbalance condition by fine tuning. Here k_p=2.5, k_i=1500 & k_D=100 are the proportional, integral & derivative gain constants. The value of the filter coefficient of the derivative term, N is taken as 0.1, as explained in (43). A minimal derivative gain constant is taken in order to increase the stability and reduce the settling time. The dc link capacitor voltage balancing strategy is appreciated as it tackles the imbalance well and the balances the dc link capacitor voltages. Figure 4.18 depicts the output voltage tracked with the reference and figure 4.19 shows the dc link capacitor voltages.
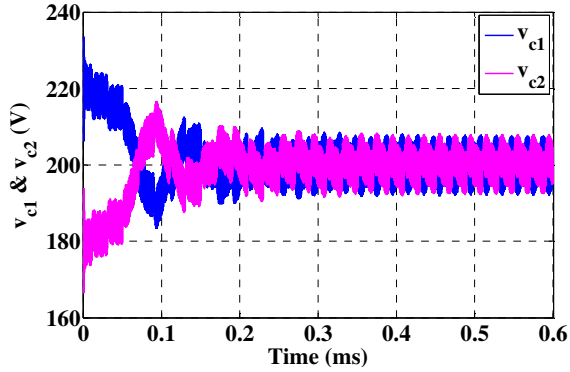

Fig. 4.16 DC link capacitor voltages v_{c1} & v_{c2} balanced by deterministic approach using 3D SVM with initial imbalance condition
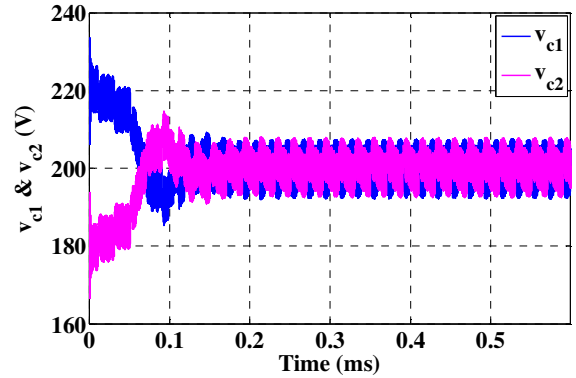

Fig. 4.17 DC link capacitor voltages v_{c1} & v_{c2} balanced by deterministic approach using 3D SVM with initial imbalance condition by fine tuning
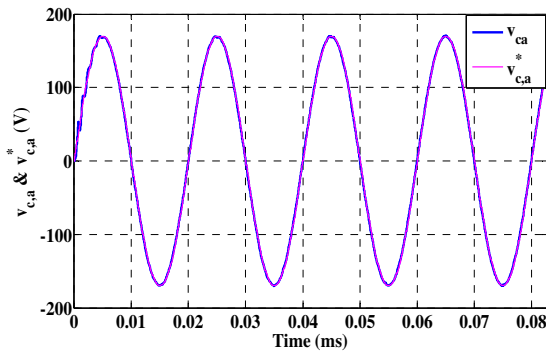
Fig. 4.18 Output voltage-reference and controlled waveforms for deterministic approach using 3D SVM
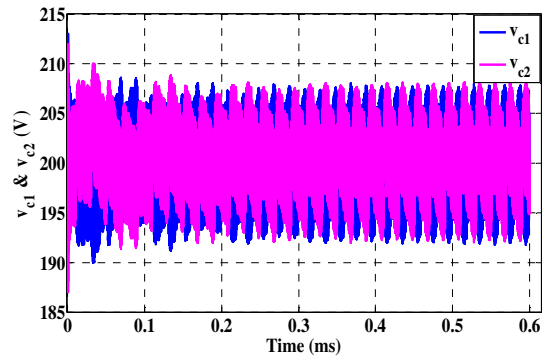
Fig. 4.19 DC link capacitor voltages v_{c1} & v_{c2} for deterministic capacitor voltage balancing approach using 3D SVM

In three-dimensional feedforward State Vector Modulation (3D FFSVM), a similar algorithm of 3D-SVM is used, in addition, the actual dc capacitor voltage unbalance is considered. Initially the 3D control region is determined in the scale of dc link generating vector, V_{on}= {0,δ_1,1} for a three-level converter and the reference control signal δ_{abc} is normalized by the factor $\frac{1}{V_{DCtotal}}$. The phase state vector is given by V_s= {0, 1, n-1}, where n is the number of voltage level of the converter. The size of the subprism is determined by the 3D control components, δ_1=v_{c1}/(v_{c1}+v_{c2}) & δ_2=v_{c2}/(v_{c1}+v_{c2}) by considering the real values of the dc link capacitor voltages. Using the above parameters, the sub-prism is found from the values of vectors Δ & ΔV, whose corresponding switching vector sequence and the switching times are computed as shown in the Table. 4.8. It is to be noted that O_{abc} & OS_{abc} are used to computed the switching times and O_{pabc} & OS_{pabc} are used to find the switching sequence.

This is done by comparing the position of elements in V_{on} and V_s vectors. For example, for phase a if $O_a=0$ and $O_{sa}=\delta_1$, as these values occupy the 1st and 2nd position in Von vector, the same positioned values of V_s vectors gives the corresponding switching state. So, in the above example the 1st and 2nd position in the V_s vectors are 0 and 1. So, $O_{pa}=0$ & $OS_{pa}=1$ are the switching state for phase a in the particular example discussed. Figure 4.20 shows the 3D-feedforward SVM algorithm for selection of sub-prism.

It is to be noted that, in 3D feed forward SVM, the second order harmonic distortion and the Total Harmonic Distortion (THD) are quickly and drastically reduced to lower values even when using a lesser voltage imbalance. It is also to be significantly noted that, in 3D feed forward SVM, the dynamic response achieves the same good operation compared to the steady state response. This paves a way to reduce the capacitance of the dc link capacitance, as possible oscillations and imbalance of the dc voltage values will not affect the output voltages and currents of the converter.
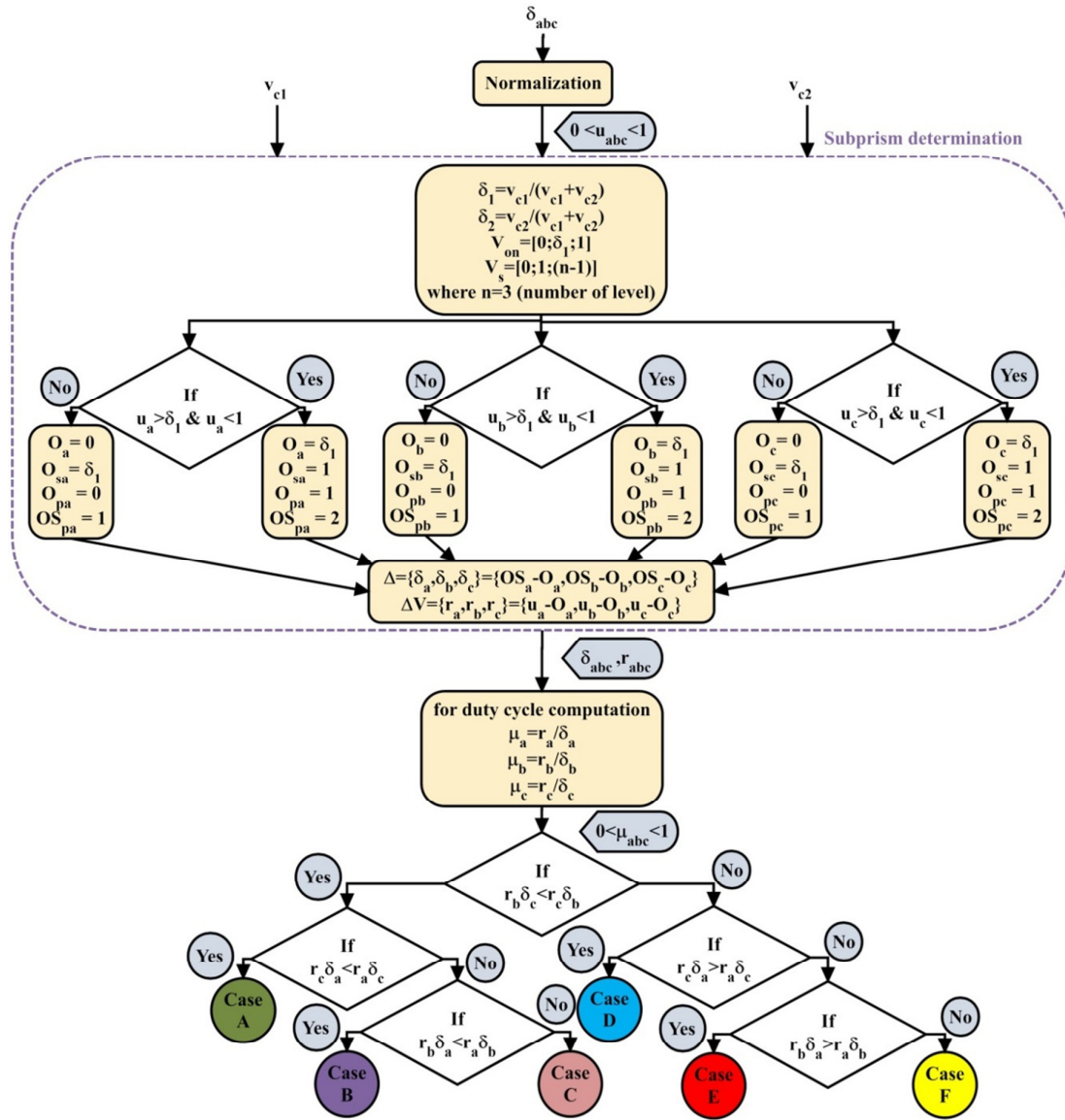
Fig. 4.20. 3D-feedforward SVM algorithm for selection of each subprism for corresponding state vectors

Table 4.8 State sequence & switching times for 3D-FFSVM

34

Cases	Space vector sequence												Switching times			
	S_a				S_b				S_c				D_1	D_2	D_3	D_4
	1	2	3	4	1	2	3	4	1	2	3	4				
A	O_a	OS_a	OS_a	OS_a	O_b	O_b	O_b	OS_b	O_c	O_c	OC_a	OC_a	$1-\mu_a$	$\mu_a-\mu_c$	$\mu_c-\mu_b$	μ_b
B	O_a	O_a	OS_a	OS_a	O_b	O_b	O_b	OS_b	O_c	OC_a	OC_a	OC_a	$1-\mu_c$	$\mu_c-\mu_a$	$\mu_a-\mu_b$	μ_b
C	O_a	O_a	a	OS_a	O_b	O_b	OS_b	OS_b	O_c	OC_a	OC_a	OC_a	$1-\mu_c$	$\mu_c-\mu_b$	$\mu_b-\mu_a$	μ_a
D	O_a	O_a	a	OS_a	O_b	OS_b	OS_b	OS_b	O_c	O_c	OC_a	OC_a	$1-\mu_b$	$\mu_b-\mu_c$	$\mu_c-\mu_a$	μ_a
E	O_a	O_a	OS_a	OS_a	O_b	OS_b	OS_b	OS_b	O_c	O_c	O_c	OC_a	$1-\mu_b$	$\mu_b-\mu_a$	$\mu_a-\mu_c$	μ_c
F	O_a	OS_a	OS_a	OS_a	O_b	O_b	OS_b	OS_b	O_c	O_c	O_c	OC_a	$1-\mu_a$	$\mu_a-\mu_b$	$\mu_b-\mu_c$	μ_c

Simulation results of deterministic dc link capacitor voltage balancing approach using 3D FFSVM also depicts improved GPC performance. Figure 4.21 shows the dc link capacitor voltages when an initial imbalance condition is enforced. Here k_p=0.5, k_i=525, k_D=25 & N=0.1. As there are few transients initially, a perfect tuning procedure can be done to obtain a less settling time. Figure 4.22 depicts the output voltage tracked with the reference and figure 4.23 shows the dc link capacitor voltages.
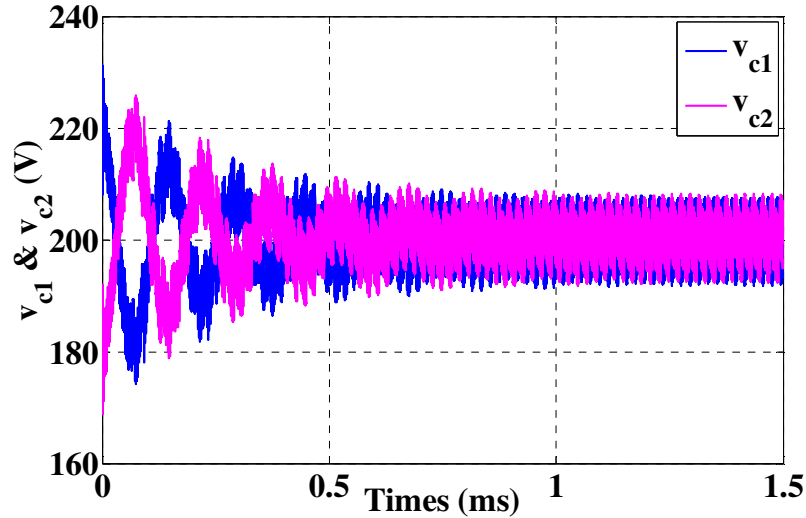

Fig. 4.21 DC link capacitor voltages v_{c1} & v_{c2} balanced by deterministic approach using 3D FFSVM with initial imbalance condition
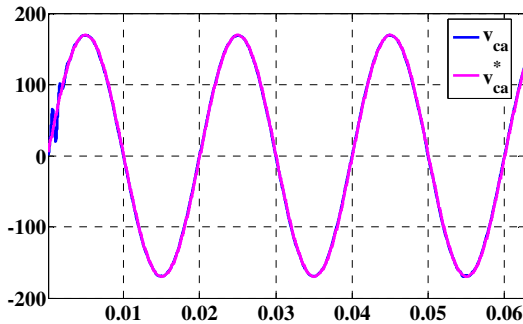

Fig. 4.22 Output voltage-reference and controlled waveforms for deterministic approach using 3D FFSVM
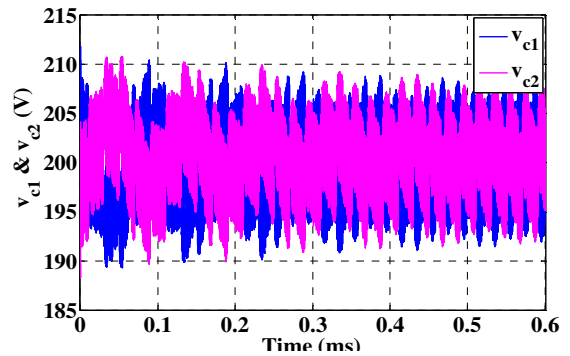
Fig. 4.23 DC link capacitor voltages v_{c1} & v_{c2} for deterministic capacitor voltage balancing approach using 3D FFSVM

4.4. COMPARISON OF THE DC LINK CAPACITOR VOLTAGE BALANCING APPROACHES

The simulation results for comparing various dc link capacitor voltage balancing strategies comprises both the single-sided amplitude frequency spectrum of the dc link capacitor voltage differences and the RMS_{error}-cum-THD values for deterministic and the redundancy approaches which are depicted below. The harmonics in the dc link capacitor voltage difference are observed for all the three approaches i.e. redundancy, deterministic-using 3D SVM and deterministic using 3D FFSVM. A set of simulations are performed for different values of weighting factor, λ and prediction horizon, N_h and the results of both RMS_{error} and THD are compared for the redundancy and the deterministic approaches.

RMS_{error} is given by,

$$RMS_{error}(\%) = \frac{RMS(v_{c,abc} - v_{c,abc}^*)}{v_{c,abc}^* | RMS} \times 100 \ \%$$

where $v_{c,abc}$ is the actual output voltage

$v_{c,abc}^*$ is the reference output voltage &

$v_{c,abc}^* | RMS$ is the RMS voltage reference =120 V, 50 Hz

Fig. 4.24 Single sided amplitude frequency spectrum of $x_2 = v_{c1} - v_{c2}$ for redundancy capacitor voltage balancing approach

Fig. 4.25 Single sided amplitude frequency spectrum of $x_2 = v_{c1} - v_{c2}$ for deterministic capacitor voltage balancing approach using 3D SVM
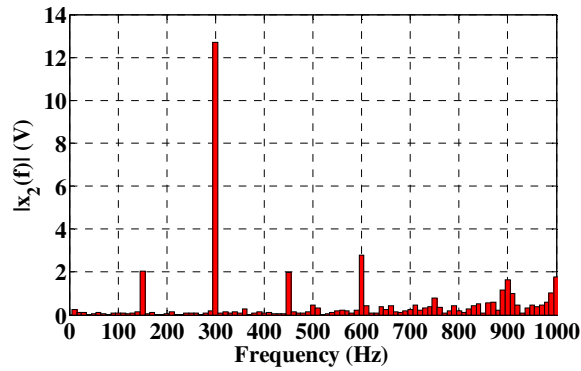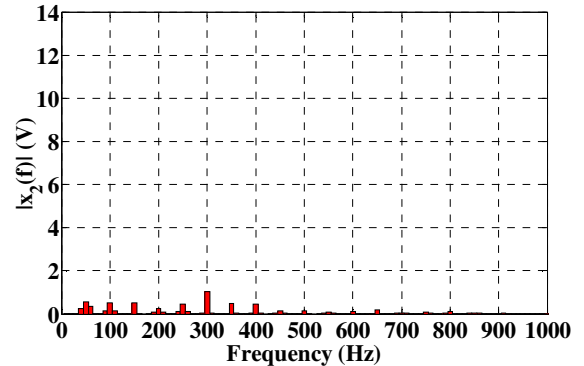

Fig. 4.26 Single sided amplitude frequency spectrum of $x_2 = v_{c1} - v_{c2}$ for deterministic capacitor voltage balancing approach using 3D FFSVM
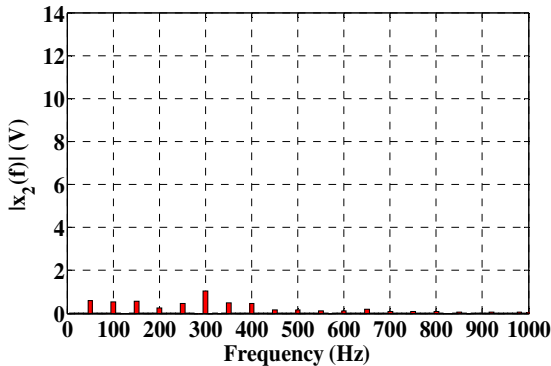
36
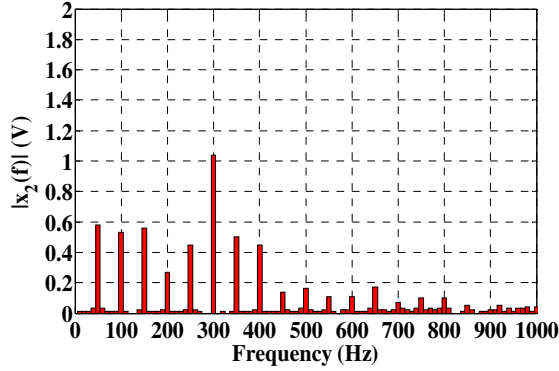
Fig. 4.27 A zoom preview of single sided amplitude frequency spectrum of $x_2 = v_{c1} - v_{c2}$ for deterministic capacitor voltage balancing approach using 3D SVM
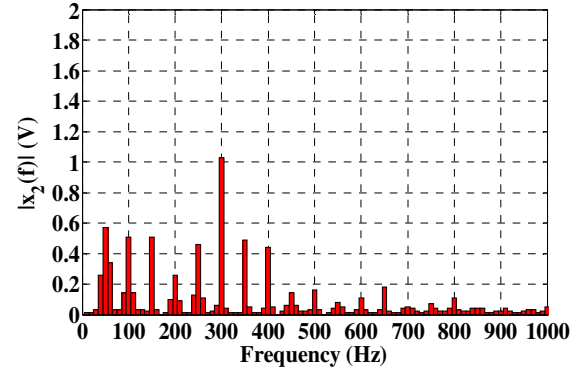
Fig. 4.28 A zoom preview of single sided amplitude frequency spectrum of $x_2 = v_{c1} - v_{c2}$ for deterministic capacitor voltage balancing approach using 3D FFSVM
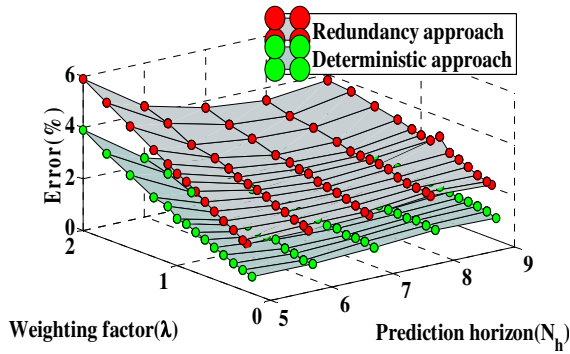
Fig.4.29 RMS_{error} values between the reference and the measured output voltages for different values of prediction horizons and weighting factors using redundancy and deterministic (3D SVM) approaches
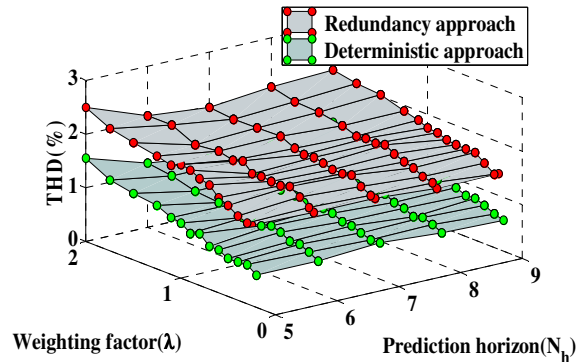
Fig.4.30 THD values of measured output voltages for different values of prediction horizons and weighting factors using redundancy and deterministic (3D SVM) approaches

Simulation results reveal that, in deterministic approach, there is fair reduction of low frequency ripples in the single-sided amplitude frequency spectrum of the dc link capacitor voltage difference, which are shown in the figure 4.24, 4.25 & 4.26. These low frequency ripples are caused by the switching of the dc link capacitors. In order to have a better comparative view, the figures 4.27 & 4.28 are depicted, which shows a zoom preview of the single-sided amplitude frequency spectrum of the dc link capacitor voltage difference of deterministic approach using 3D SVM and 3D FFSVM. The simulation results also reveal that the deterministic approach of capacitor voltage balancing has low RMS_{error} and THD values, than the redundancy approach, which are depicted in the figure 4.29 & 4.30. It is to be noted that in figures 4.29 and 4.30 the 3D SVM is used in the deterministic approach.

CHAPTER 5

DESIGN OF A NPP POWER INVERTER

The foremost step in designing the prototype of NPP power inverter is evaluating the IGBT module. The main components used in this process are the Digital Signal Processor (DSP) device (TMS320F28335), IGBT driver board & its I/O connectors, IGBT module, a resistive load (say 300 Ω), a Cathode Ray Oscilloscope (CRO), a computer/laptop with installed Code Composer Studio (CCS) , regulated DC power source for converter input, a 15 V DC power source for IGBT driver board and few connecting wires. Figure 5.1 shows the block diagram of the main components including Integrated Circuits (ICs) & connectors and their connections for the NPP module evaluation. The switching pulses across the gate-emitter terminal and the output voltage across the load resistor are observed by CRO during evaluation. Although the IGBT driver is used to drive two modules in parallel, only one module (single mode operation) is used for evaluation purpose. The main aim of the evaluation of the AT-NPC 3-level 4in1 IGBT module [79] is to ensure, that the PWM pulses (T_1, T_2, T_3 and T_4), which are generated by the DSP properly fires the semiconductor switches in the IGBT module, via the IGBT driver board and the output voltage is checked across the load resistor.
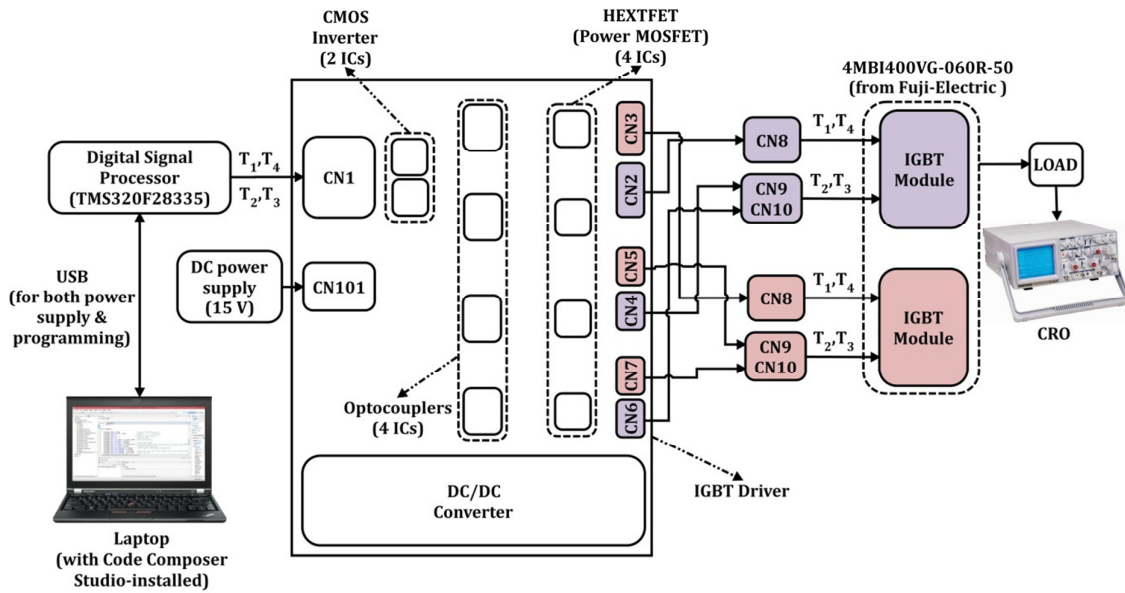
Fig. 5.1. Block diagram consisting of main components, ICs & connectors for the NPP module evaluation

Circuit arrangement, description & working

The DSP TMS320F28335 is programmed to produce the gate signals with switching frequency-2kHz, $V_{peak-to-peak}$=3.44 V (0-3.44 V switching pulse) and duty cycle-50 % based on the switching modes, shown in table 5.1, in which 'ON' represents a full pulse with 100 % duty cycle, 'OFF' represents the switching pulse with 0% duty cycle and 'SW' represents a switching pulse of user's choice of duty cycle (as the purpose is evaluation of the prototype). Enhanced Pulse Width Modulator (ePWM) 1-6 refers to six pins in the General Purpose Input/Output (GPIO) of the DSP device [80], specially designed for taking the PWM signals to the driver, once it is programmed in Code Composer Studio (CCS) [81], installed in a

computer or laptop. ePWM1A (at GPIO0) is used as T_1, ePWM1B (at GPIO1) is used as T_2, ePWM3A (at GPIO4) is used as T_3 and ePWM3B (at GPIO5) is used as T_4.
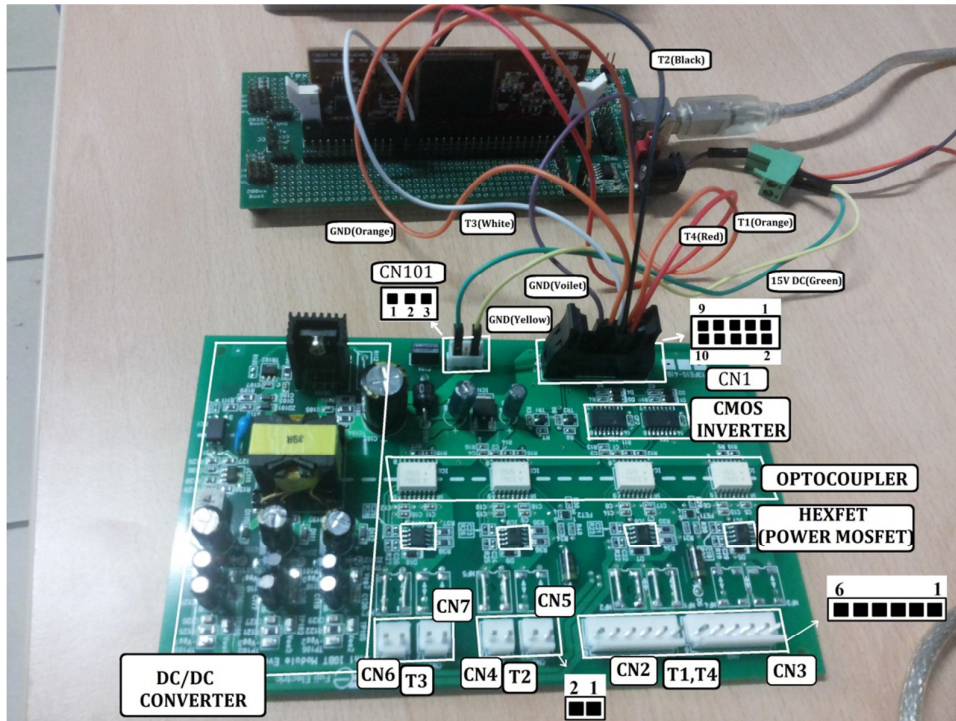
Fig. 5.2. Circuit arrangement showing DSP connected to the IGBT driver board

Table 5.1 Switching modes of AT-NPC 3-level IGBT module (a three level NPP converter leg)

SW mode	A_1	B_1	A_2	B_2
T_1	SW	OFF	OFF	OFF
T_2	OFF	OFF	SW	OFF
T_3	OFF	SW	ON	ON
T_4	ON	ON	OFF	SW

Table 5.2 Pin configuration of Input connectors- CN1 & CN101 for each IGBT driver board

Pin	Signal	Connector
1	PWM signal for high side IGBT(T_1)	CN1
2	PWM signal for RB-IGBT(T_4)	CN1
3	PWM signal for RB-IGBT(T_3)	CN1
4	PWM signal for low side IGBT(T_2)	CN1
5	GND	CN1
6	GND	CN1
7	GND	CN1
8	GND	CN1
9	GND	CN1
10	Fault detection output IGBT (T_1, T_2)	CN1
1	V_{DC} (15 V)	CN101
2	NC	CN101
3	GND (0 V)	CN101

39

The four switching pulses obtained from DSP are sent to the IGBT driver board via the connector CN1. The driver board is powered by a 15 V DC source via CN101. The pin configuration of these two connectors i.e. CN1 & CN101 are furnished in the table 5.2.

The foremost components where the PWM signals enter the IGBT driver board via CN1 connector are the Complementary MOSFET (CMOS) inverters (2 no.s) [82], which provides a buffered output with high noise immunity and stable output. These components are followed by optocouplers (4 no.s), which are used to drive, turn-on and off the power semiconductor switches. These dual outputs driven optocoupler (ACPL-339J) [83] contains a AlGaAs LED each, which is optically coupled to an integrated circuit with two power output stages with active timing control to prevent cross conduction at external MOSFET buffer. It is also integrated with features such as V_{CE} detection, under voltage lockout (UVLO), 'soft' IGBT turn-off and isolated open collector fault feedback to provide maximum circuit protection and integrity. It is also noted that the DESAT protection is the highlighting feature of these type of optocouplers, which makes turns off the IGBT shortly whenever a DESAT (or short circuit) fault is detected. These optocouplers are followed by the ultralow resistive dual N and P channel MOSFETs (4 no.s) [84], which deliver superior power density and lower switching losses to shrink the PCB size and improve the overall system efficiency. These MOSFETs are combined with excellent thermal performance and low on-state resistance. There is a common mode choke to ensure protection between the MOSFET and the output terminal connectors-CN2, CN3, CN4, CN5, CN6 & CN7 of the IGBT drivers. Table 5.3 shows the pin configuration of these connectors. Figure 5.3 shows the connections between the output terminal of the IGBT driver and the connectors- CN8, CN9 & CN10. These connectors have space for components like active clamp and resistors, which are used for protection during short circuit. These connectors are mounted on the IGBT module. It should be noted that the active clamp diode are not initially connected, as only few IGBT module needs it. There is a DC/DC converter in the left end of the board, which ensures appropriate power supplies to the ICs.

During single mode operation (connecting only one IGBT module) the common mode choke area is short circuited and the connector CN3 should not be used. Either of the connectors- i.e. CN5 or CN4 and CN6 or CN 7 can be used during single mode operation. Care should be taken that the IGBT is not operated without connecting T1C and T1 collector terminal.

Table 5.3 Pin configuration of Output connectors- CN2, CN3, CN4, CN5, CN6 & CN7 for each IGBT driver board

Pin	Connector	Remarks	Remarks
1	CN2/CN3	RB-IGBT Gate (T$_4$G)	connected to CN8-1
2	CN2/CN3	high side IGBT & RB-IGBT Emitter (T$_1$/T$_4$E)	connected to CN8-2
3	CN2/CN3	high side IGBT Gate (T$_1$G)	connected to CN8-3
4	CN2/CN3	No Connection	-
5	CN2/CN3	No Connection	-
6	CN2/CN3	high side IGBT Collector (T$_1$C)	connected to CN8-6
1	CN4/CN5	low side IGBT Emitter (T$_2$E)	CN1
2	CN4/CN5	low side IGBT Gate (T$_2$G)	CN1
1	CN6/CN7	RB-IGBT Emitter (T$_3$E)	CN1
2	CN6/CN7	RB-IGBT Gate (T$_3$G)	CN1
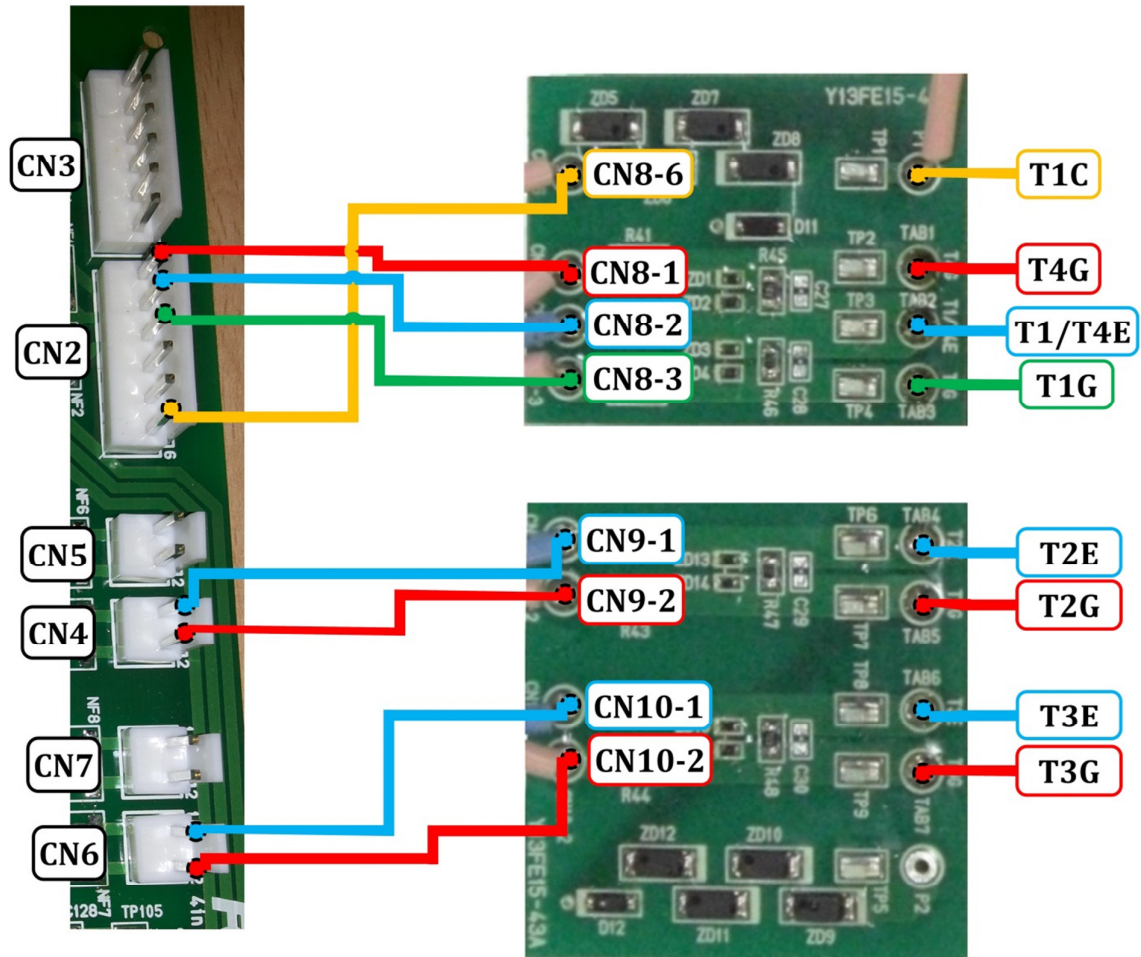
Figure 5.3 Connection between the output terminals of IGBT driver board and the connectors-CN8, CN9 & CN10

Drivers and First Fault Detection (FFD)

Initially, the components shown in table 5.4 are detected to be not working, since the components outputs are not the desired one, which varied from those of the working drivers.

Table 5.4 List of Faulty components during FFD

IGBT Drivers	Number of Optocouplers- not working	Number of MOSFET- not working
Driver 1	-	-
Driver 2	2 (for T4 and T1)	1 (for T2)
Driver 3	1 (for T2)	-
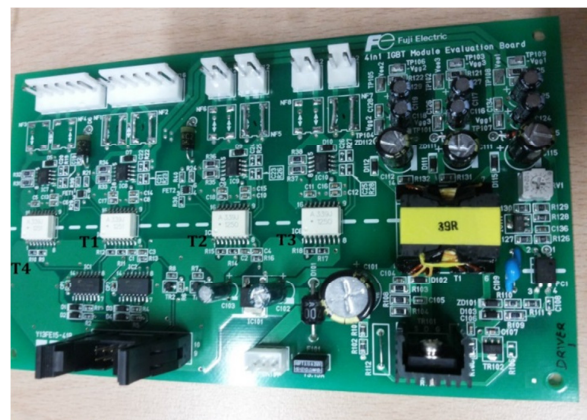
Fig. 5.4 IGBT Driver 1

41
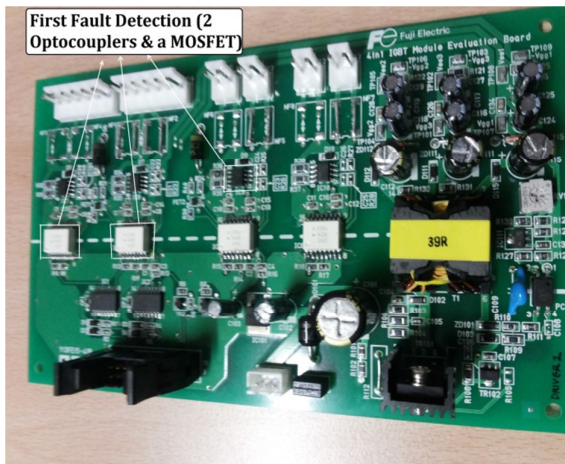
Fig. 5.5 IGBT Driver 2
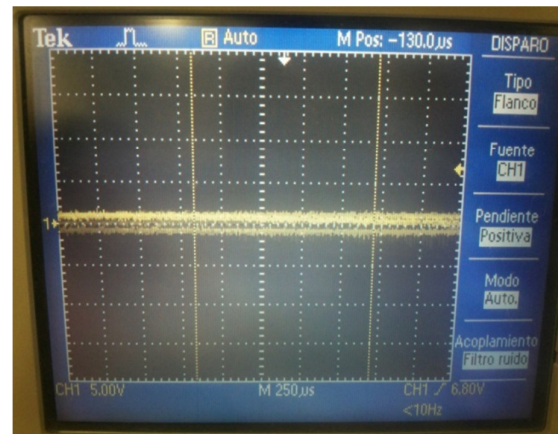
Fig.5.7 Faulty Optocoupler's High side voltage output
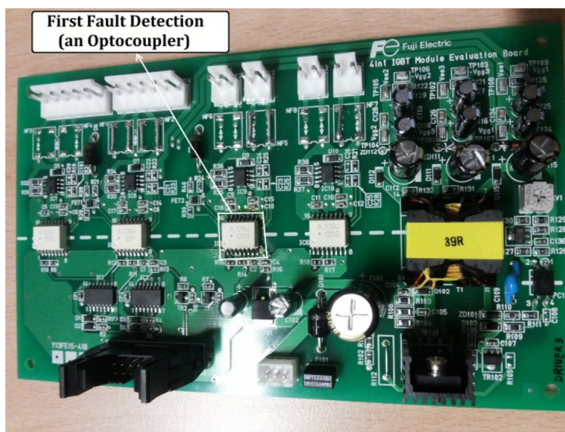
Fig. 5.6 IGBT Driver 3

Fig.5.8 Faulty Optocoupler's Low side voltage output

Progress of work in fixing the Drivers

i.   When the faulty optocoupler (T_2) in driver 3 is replaced with the one of the working optocouplers of driver 2, the same results were observed as shown in figure 5.7 & 5.8. During this process, the soldering station is used to unsolder the IC and the temperature of the soldering station ranges from 200-450 °C. So, the replaced optocouplers are suspected to have damaged LED during this replacement process.

ii.   After replacing a new MOSFET at T_2 in driver 2, still the same results were obtained. Now, when checking the resistor, R36 (10 Ω) at the output of the MOSFET, it has been observed that the resistance value is too high in kΩs (open-circuited). When the resistor R36=10 Ω is replaced, the T_2 of driver 2 works well. So, now the T_2 of driver 2 is fixed.

A= C_5, C_7, C_9, C_{11} (1 µF)
B= C_6, C_8, C_{10}, C_{12} (10 µF)
C= C_{13}, C_{14}, C_{15}, C_{16} (1 µF)
VE= Common (IGBT Emitter) output supply voltage
V_{CC2}= Positive output supply voltage
V_{EE}= Output supply voltage
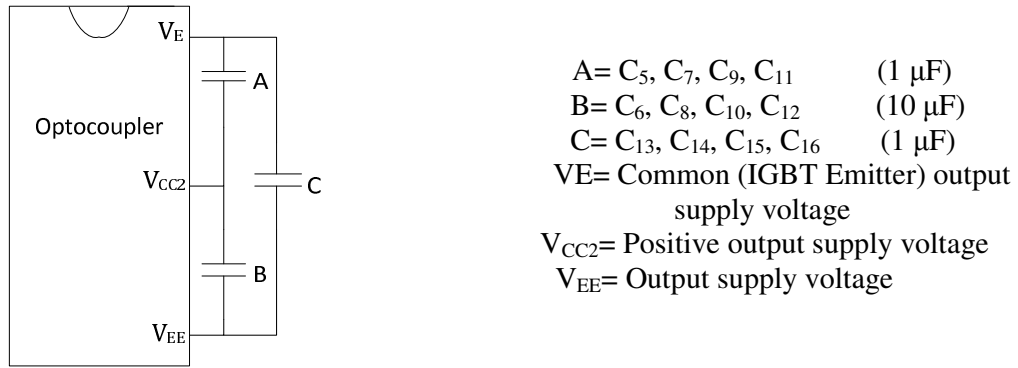
Fig.5.9 Optocoupler secondary side power supplies-outline

iii.   When the new optocouplers of T_1 and T_4 of driver 2 & T_2 of driver 3 are replaced, same results were obtained. Now, the voltage supplies of the optocoupler are examined and found that the voltage across V_{CC2}-V_E is not the desired value. Table 5.5 shows the rating of the output side power supply of the optocoupler and table 5.6 shows the observed values in the faulty optocouplers. The capacitor A (C_5, C_7 of driver 2 and C_9 of driver 3) is checked, because it can also fail to maintain the voltage across V_{CC2}-V_E. So, new capacitors were replaced in A for the faulty optocouplers. Figure 5.9 shows the outline of optocoupler's secondary side power supplies.

Table 5.5 Ratings of output side power supply of optocoupler

Absolute maximum ratings			
		Min (V)	Max (V)
Total output supply voltage	V_{CC2}-V_{EE}	0	35
Negative output supply voltage	V_E-V_{EE}	0	17
Positive output supply voltage	V_{CC2}-V_E	0	35- (V_E-V_{EE})
Recommended operating conditions			
Total output supply voltage	V_{CC2}-V_{EE}	21	30
Negative output supply voltage	V_E-V_{EE}	6	15
Positive output supply voltage	V_{CC2}-V_E	15	30- (V_E-V_{EE})

Table 5.6 Observed values in the faulty optocouplers

Parameters	Working condition	Faulty condition
V_{CC2}-V_{EE}	25 V	25 V
V_E-V_{EE}	10 V	25 V
V_{CC2}-V_E	-15 V	0 V
Voltage across B	25 V	25 V
Voltage across C	10 V	25 V
Voltage across A	-15 V	0 V

43

iv.   After replacing new capacitors across C_5, C_7 of driver 2, C_9 of driver 3 it is found that the fault was with the power supply V_{CC2}-V_E of the optocoupler and not the capacitors across it. When checking the components of their respective power supplies, the zener diodes of the faulty optocouplers were easily shorting with very less resistances. After replacing new zener diodes, the optocouplers are ensured proper power supply across V_{CC2}-V_E and thus the desired output is obtained. Finally, the remaining faults (T_1 and T_4 of driver 2 & T_2 of driver 3) were fixed. Figures 5.10, 5.11, 5.12 & 5.13 shows the output of optocoupler & gate-emitter terminal of IGBT driver for various working modes.

Table 5.7 Summary of faults in drivers & its correction

IGBT Driver	Number of Optocouplers-not working	Number of MOSFET-not working	Reason of fault	Faulty components (replaced to make the driver working)
Driver 1	-	-	In T_4 and T_1 there was no desired power supply across V_{CC2}-V_E for the faulty optocouplers	Zener diode PH C15
Driver 2	2 (for T_4 and T_1)	1 (for T_2)	In T_2 the resistor, R36 at the P-Drain output of MOSFET is open circuited	R_{36} (10 Ω) resistor
Driver 3	1 (for T_2)	-	In T_2 there was no desired power supply across V_{CC2}-V_E for the faulty optocoupler	Zener diode PH C15
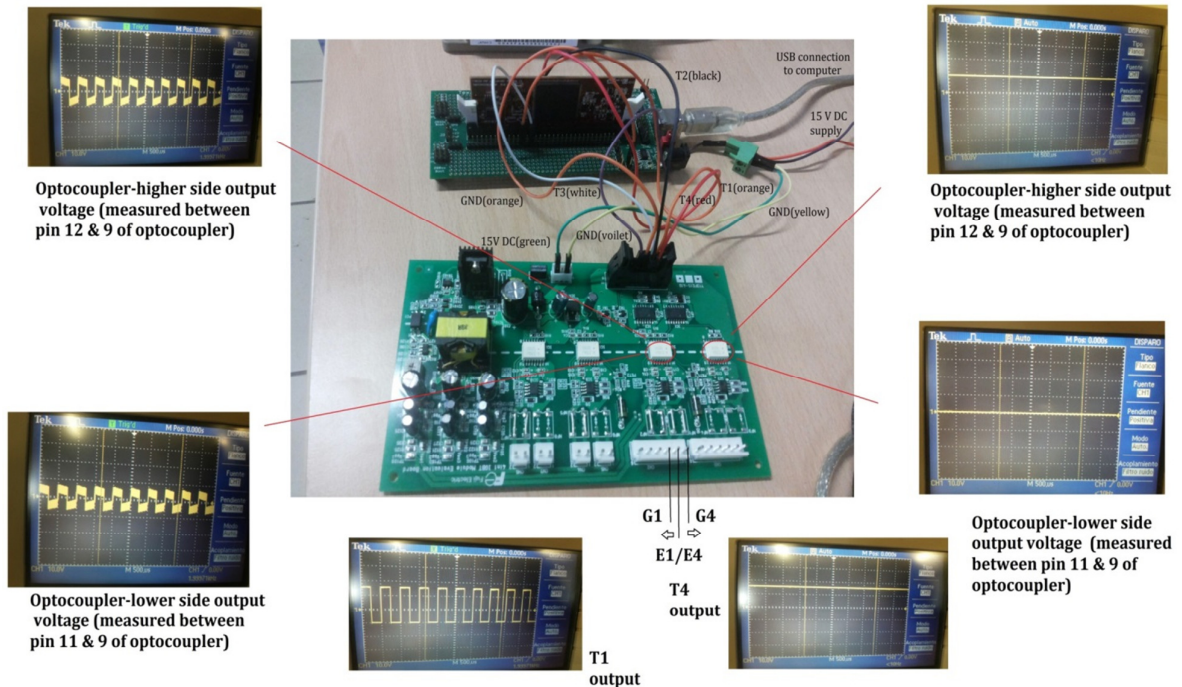
Fig. 5.10 Working mode of A_1
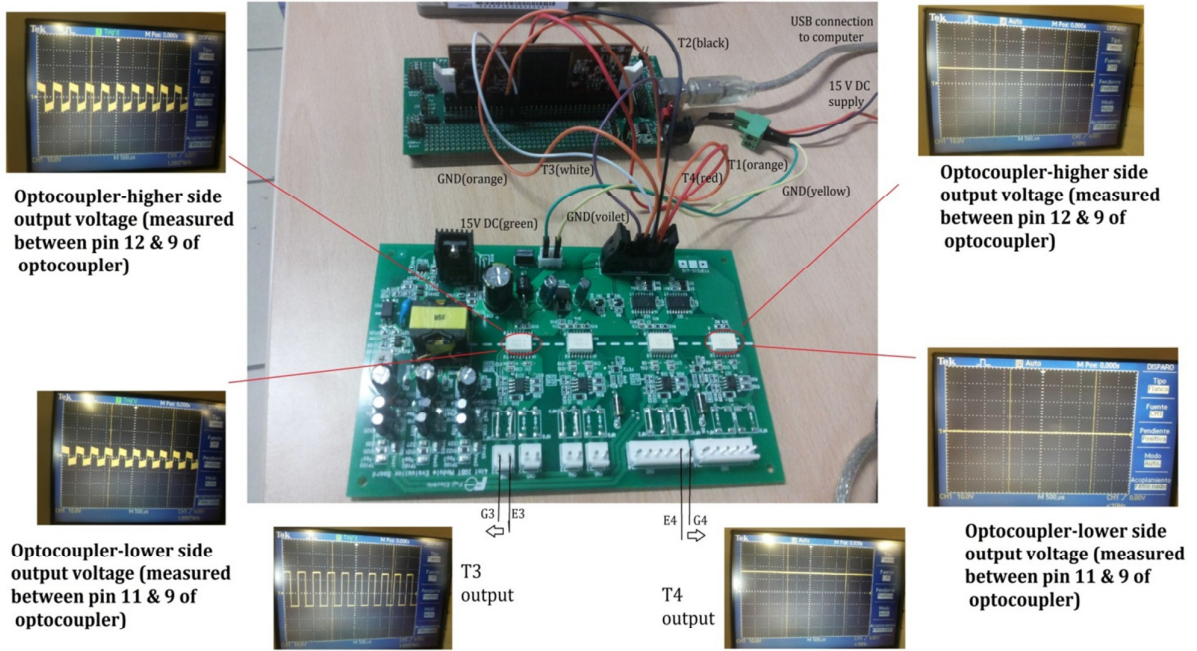
Fig. 5.11 Working mode of B₁
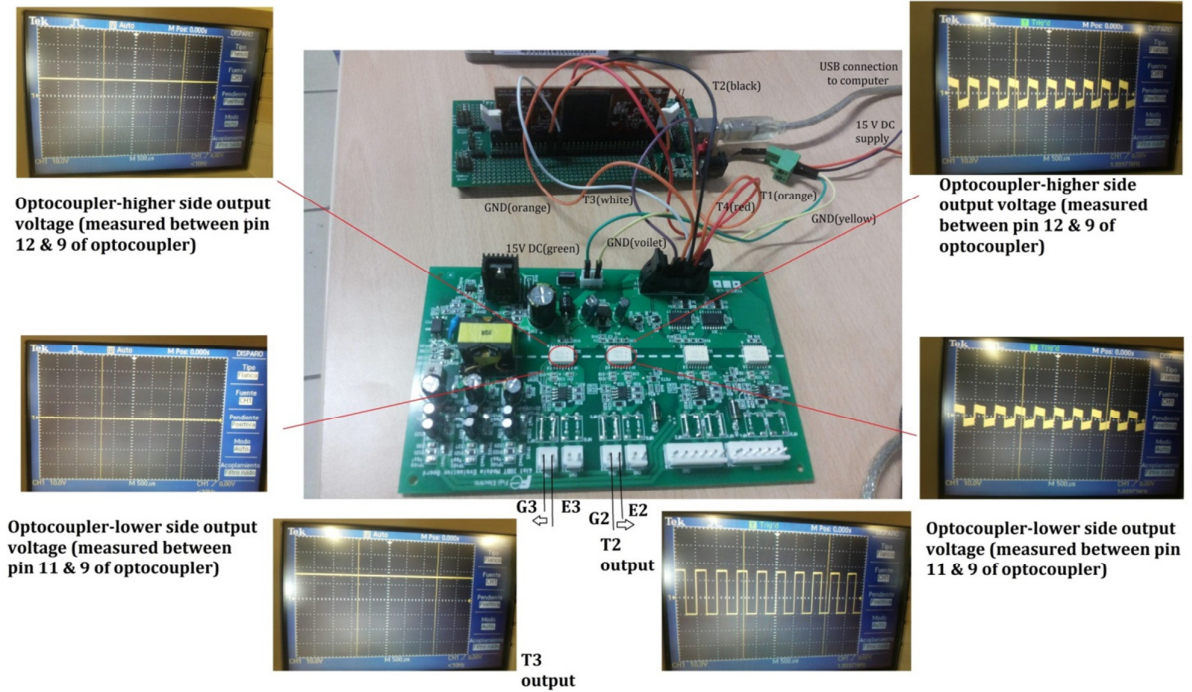
Fig. 5.12 Working mode of A₂
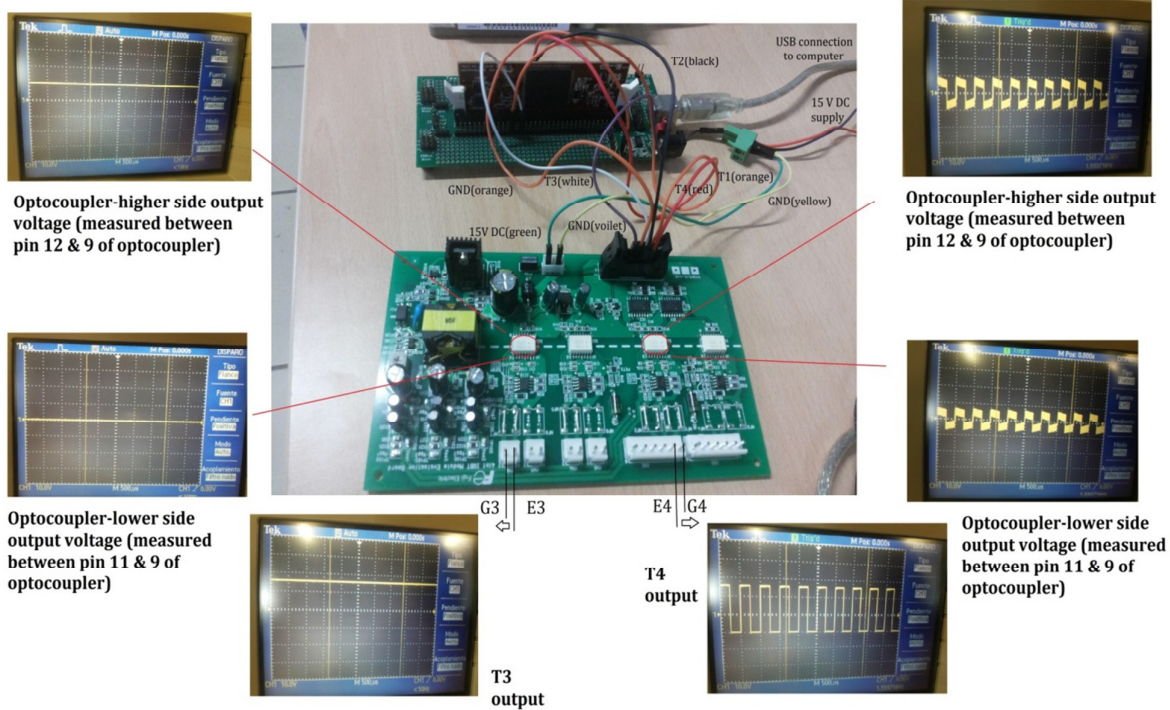
Fig. 5.13 Working mode of B$_2$

CHAPTER 6

ADVANTAGES & APPLICATIONS

Advantages- The foremost advantage of the NPP inverters is the good operating efficiency for medium switching frequencies from 6-20 kHz and this makes suitable for medium and low power PV applications. The GPC-control and its capability to track the reference even during a model mismatch of parameter, results in controlled output voltage with reduced RMS_{error} and THD values for deterministic approach, than the redundancy approach. The observer and controller used in the deterministic method not only paves a way to balance the dc link capacitor voltages, but also reduced the lower order harmonics in the dc link incurred during dc link capacitor's switching.

Applications- Applications of such controlled T-type multilevel inverters find its use in small & medium power PV & wind energy systems, UPS, standalone applications, small unmanned drones, etc., where high efficiency, compactness, less weight, easy operation, low conduction & switching losses are considered as the key elements of the system.

CHAPTER 7

CONCLUSION & FUTURE WORK

Thus, the generalized predictive controlled T-type converter using deterministic as well as the static redundancy approaches are simulated and the comparisons were made from the system performance perspective. Different modulation schemes like 2D-SVM, 3D-SVM and 3D FF-SVM are studied, applied and realized during the course of the project. Emphases on control theory and its application on power inverters are also studied. All the three control objectives i.e. control of output voltage across the filter capacitor, dc link capacitor voltage balancing and considerable low frequency ripple reduction are achieved. The work on the prototype of IGBT drivers and its evaluation have given hands-on laboratory exposure to PCBs, DSP, IGBT drivers, modules and its supplementary circuits.

Future work relies on implementing an optimized tuning methodology for the PI or PID controller. Incorporating other control strategies in place of PI controller, like predictive control or neural network control can be done, thereby comparing the strategies in terms of effectiveness, harmonics, computation cost and overall system integrity. As the first phase of building the prototype is accomplished, future work also relies on developing the complete NPP inverter system in order to check its performance with respect to the simulation results.

CHAPTER 8

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