

Electro-optical measurement system for the DC characterization of visible detectors for CMOS compatible vision chips

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Abstract

An electro-optical measurement system for the DC characterization of visible detectors for CMOS compatible vision chips is presented which can help designers to characterize these detectors. The measurement system has been designed to be versatile, fast and easily expandable and used. Two different set-up's for the measurement of the spectral response and the optical dynamic range of the detectors are described in detailed. Measurements of the spectral response are done with a fully computer controlled set-up, avoiding tedious and inaccurate measurements. A description of the different detectors available in a CMOS process is also given, together with the parameters affecting their response and a set of test structures which can be useful for the characterization of the detectors.

1. Introduction

In the last years there has been a growing interest in the development of CMOS compatible imagers which can substitute CCD cameras in imaging applications [1], overcoming the limitations of this technology when small sizes, low power consumption and random access are required [2]. CMOS imagers also allow on-chip processing of the image data which is very complicated and area expensive in a CCD camera [2]. This last property has been of great importance for the development of vision chips which not only detect the light intensity and transduce it into an electrical variable (voltage or current), but also process in real-time the signals from an array of photodetectors by including parallel analog signal processing on-chip. A good revision of vision chips including signal processing circuitry can be found in [3].

One major problem encountered when designing a vision chip in standard CMOS technologies is that foundries do not deliver characterization data for the available photosensors. Thus, designers are forced to use simplistic behavioral models based on the idealized CMOS-compatible photosensor descriptions found in literature. This may be enough for chips intended to process binary (black-and-white) images [4]. However, the characteristics of real devices largely differs from their idealized descriptions, being, on the other hand, strongly dependent on the fabrication process. Consequently, using these idealized models yields very inaccurate results whenever the analog content of the incoming light (regarding both intensity and wavelength) is significant for signal processing; i.e. chips whose behavior is anticipated on the basis of such simplified models will, most likely, not accomplish the specifications ¹.

In this scenario designers of vision chips are confronted to the necessity to fully characterize the CMOS-compatible photosensors by themselves. Unfortunately, this is not a simple task because it requires instrumentation apparatus and expertise which are not common to chip designers. This paper is intended to help designers to fill this gap. Based on a set of CMOS-photosensor test structures, we present a measurement system (including equipment and procedures) for their DC characterization. This system has been conceived to achieve two major targets: first, it should be used by people with a minimum optical background (i.e., by chip designers); second, it should be versatile (meaning that it should allow for different types of measurements set-up's), easily expandable, and fast. This is achieved by making the different optical and measurement parts to interact in such a way that the whole operation can

1. This risk cannot be undertaken because vision chips may be very large, up to 1cm^2 . The fabrication cost of a 1cm^2 chip as part of a MCP in a standard $0.7\mu\text{m}$ technology is about 27.500 \$.

be computer controlled, eliminating tedious and inaccurate measurements.

In section 3, the set of test structures useful for the characterization of visible detectors will be presented. Before a background on junction detectors available in a CMOS process will be given in section 2. This basic knowledge of the junction structures used for detection and the main parameters affecting their response will help to better understand the design of a dedicated chip for the characterization of the photodetectors and the measurement system used. A detailed description of the elements of this measurement system and the different set-up's mounted for their electro-optical characterization will be given in section 4. In this section the results obtained in the characterization of one of this detectors, which is a good candidate for the realization of vision chip, will be presented.

2. Theoretical background on CMOS junction photodetectors

2.1 Junction photodetectors

In a standard CMOS process, several junction structures can be used to convert light into an electrical signal. These structures are depicted in Figure 1 for an n-well process (the complementary structures are obtained in a p-well process). The first three structures are p/n diodes, whereas the last one is a vertical bipolar junction transistor (BJT). Diodes are formed by well/substrate (n^-/p^-) junctions, source-drain diffusion/substrate (n^+/p^-) junctions and source-drain diffusion/well (p^+/n^-) junctions. Vertical p/n/p BJT's are obtained by the structure formed by a p^+ source-drain diffusion, an n^- well and the p^- substrate.

When light is incident on a diode, photons absorbed in the depletion region of the p/n junction create electron-hole pairs which will be separated by the high internal electric field

formed across it. This charge can be detected as an increase in the reverse current of the device or as a change in the voltage across it. Carriers generated in the silicon bulk at a distance within a minority carrier diffusion length from the depletion region can also contribute to the detected signal, increasing the sensitive volume of the detector. The detected signal in a diode can be represented by a photogenerated current [5]:

$$I_{ph} = \frac{A \cdot P \cdot \lambda \cdot \eta}{1.24} \quad (1)$$

where A is the detector area, P the incident light power per unit area, λ the wavelength of the incident light in microns and η the quantum efficiency of the process.

For a phototransistor which is polarized in the active forward region with the base terminal (the well) left floating, the incident light generates electron-hole pairs in the reversed biased base-collector junction that induce a current which is equivalent to a base current. This base current is amplified by the gain of the transistor, resulting in an emitter current which is $(1+\beta_F)$ times the detected current. The emitter current is expected to be equivalent to the detected current in a well/substrate diode of the same well area, but amplified by $(1+\beta_F)$. The photogenerated current will be given by,

$$I_{ph} = \frac{A \cdot P \cdot \lambda \cdot \eta}{1.24} (1 + \beta_F) \quad (2)$$

where A is the area of the transistor base.

Comparing both types of detectors, photodiodes have the advantage of simpler structure and faster response, whereas phototransistors benefit from greater gain, although they also

require proportionally more power to operate.

The optical dynamic range of a photodiode or a phototransistor is normally defined as the range of incident light power over which the detected signal behaves as a linear function, according to equation (1) or (2), respectively. Usually its lower limit is determined by the dark current of the detector, which is the current flowing through the device without illumination, whereas the upper limit may be device or external circuit limited. For the detectors available in a standard CMOS process the optical dynamic range is about 7 decades of incident light intensity for photodiodes and 5 decades for phototransistors [6].

The difference in photoresponse between each type of sensor is determined by the fact that the absorption of light in silicon is strongly dependent on the wavelength. The absorption length, $L(\lambda)$, is shorter for shorter photon wavelengths [7]. This means that photodetectors formed with junctions which have different junction depths will have different spectral response. According to this, the three different types of diodes introduced in Figure 1 will present different spectral responses. From literature it is known that the n^-/p^- and n^+/p^- diodes behave in a similar manner [8], increasing their response with photon wavelength. The p^+/n^- diodes are more sensitive at shorter wavelengths as collection of carriers is limited by the volume bounded by the surface and the n^-/p^- junction, in contrast with the other diodes where the collection of carriers is limited by the diffusion length of minority carriers in the silicon bulk. Phototransistors response is very similar in shape to the spectral response of the n^-/p^- diodes but increased by the amplifying factor $(1+\beta_F)$ [8].

2.2 Technology and area scaling effects

The response of these detectors is also affected by other parameters, such as technology

scaling and detector size and shape. The effect of technology scaling is mainly caused by the wavelength dependence of the absorption length. When technology dimensions shrink, the spectral response of the devices shifts to shorter wavelengths, reducing their spectral detection range. This is due to the fact that for scaled processes the vertical dimensions get shorter, and photogenerated carriers contributing to the detected signal are those closer to the surface. Longer wavelength photons can contribute only if the junction is deep enough. This means that the detector response degrades for long wavelengths when the technology is scaled down. It is also known that in submicron technologies the doping level of the junctions is substantially higher than the corresponding value in a technology larger than $1\mu\text{m}$, therefore affecting the junction characteristics and hence the response of the detectors. Technology scaling also implies a voltage scaling which imposes important limitations in the dynamic range due to the decrease of the full signal charge capacity [2].

Technology scaling is certainly followed by a pixel scaling. The trends showed during the last years indicate that pixel size and fill-factor (ratio of sensor area to pixel size) scale linearly with the minimum feature size [2]. This reduction in sensor area implies a reduction in the photogenerated current, as can be seen from equation (1). Nevertheless, this linear relationship is no longer valid when the area of the detector is very small. At this point the volume of the lateral depletion region is comparable to the volume of depletion region determined by the detector area, therefore increasing the expected detected current. For this reason, it is important to characterize all possible detectors for different sizes independently of the circuitry to obtain the photogenerated current levels for each case.

These effects have to be considered when selecting a detector for an imaging application.

All possible detectors have to be characterized for each technology in order to select the optimum device to match the requirements of the signal processing circuitry. Therefore the need for an electro-optical set-up which allows the characterization of these detectors.

3. Photodetectors test structures

The characterization of the above described detectors needs in most cases of the realization of a dedicated chip with test structures which can be used to determine the actual response of the detectors processed in a given technology.

The response of these detectors can be affected by different parameters which can be either process or lay-out dependent. Process dependent parameters (i.e. junction depths, doping concentration ...) cannot be modified by the designer, opposite to lay-out dependent parameters (detectors size and shape). Therefore, when designing a test chip to characterize visible detectors both types of parameters have to be considered. On the one hand, all possible devices or structures available in the technology to detect visible light have to be included in the chip to obtain their actual behavior in the visible spectrum. On the other hand, these detectors should be tested for different sizes and shapes to account for the lay-out dependent parameters. Ideally, each detector should be tested for as many as possible sizes and, for each size, different perimeters (shapes) should be included. Furthermore, the chip should include as many as possible instances of each detector configuration to obtain statistical information on their response. However, the cost of fabrication of such a chip would be very high since detectors have to be connected to bonding pads to have direct access to the detected signal. A more realistic approach would consist on including a limited number of discrete detectors with different sizes and shapes, covering all the possible device structures, and several arrays of

detectors which can give statistical information. When considering the use of arrays of detectors, both digital decoders and multiplexers have to be included in the chip. However, the number of bonding pads needed is much smaller than the number of devices which can be measured.

Figure 2 shows the lay-out of a dedicated test chip that we have designed to characterize the photodetectors of a 0.8 μm CMOS process. In this chip we have included both discrete detectors, which are placed at the outer part of the chip, and arrays of 16x16 detectors, which are situated in the central area of the chip. To access the different elements of each array, three different decoders are used: one for the arrays, a second one for the columns and the last one for the rows. Each pixel includes an MOS switch which is activated by the output of the column decoder. Once a column is selected, the photogenerated signal of each row is transferred to its array multiplexer where the photogenerated signal of the selected row is output. This operation is done for all the arrays at the same type, therefore a global multiplexer is used to output the signal of the selected array to a pad. In this chip we have also included a pixel structure (labeled as test pixel in Figure 2) to be studied as a possible candidate for imaging camera.

The lay-out of the four different junction detectors, which were presented in section 2, can be seen in Figure 3. A ring of substrate contacts surrounds each detector to have a better collection efficiency, since the substrate is one of the electrodes of the detector (except for the diffusion/well diode). For the case of discrete diodes, the three different types of devices are included in the chip at least for one size, which is the largest size (100 μm x100 μm). One of them is studied in detail to obtain information on both area scaling and perimeter effects by

including 4 different sizes (ranging from $100\mu\text{m}\times 100\mu\text{m}$ to minimum size), and one of this sizes is studied for three different perimeters. The last diode is processed for two different sizes and two perimeters for one size. Thewell/substrate diode includes a n^+ contact ring for the largest detector areas to improve the collection of photogenerated carriers. Vertical bipolar transistors are also included in the chip with base areas ranging from the minimum size to 16 times the minimum size.

As can be seen in Figure 2, seven different arrays have been included in the chip (labeled A1, AA, A5, A6, A8, A9 and AD). Since the main idea is to obtain statistical information on the response of the detectors for their future application in imaging cameras, the areas of the detectors are minimum size or four times this minimum size, corresponding to usual areas in this type of applications. In some cases the efficiency of the substrate contact is studied by changing its size and position in the pixel. The size of the substrate contact is important for the design of imaging cameras since it affects the fill factor (ratio of sensing area to pixel area) of the pixel.

An important design consideration that has to be taken into account when making the lay-out of such a chip, is the need for a metal layer which can cover all the chip but the sensing areas (in Figure 2, the metal 2 layer, which covers most of the chip area, is not shown to allow a clear image of the lay-out). The silicon substrate is a potential detector where photons arriving to it can generate excited carriers with very long diffusion lengths in silicon. These excited carriers can be detected if a polarized junction is close enough (closer than their diffusion length in silicon). Therefore they can arrive to the detectors or to any other junction (i.e. a MOS switch) producing an increased in the actual currents. Although this effect can be

to a certain point positive for the design of cameras where the sensor area, and therefore the photogenerated current, is very small, in general, all the electrical circuitry can be strongly affected, changing its normal behavior. Special care must be taken to avoid the interaction of NMOS transistors with carriers generated in the surrounding substrate. For PMOS transistors, the problem is reduced since the interaction will be limited to the well area, although it will still remain and all the area should to be covered by metal.

After describing the test structures useful to characterize the different detectors available in a standard CMOS process, in the next section the effort will concentrate in describing the measurement system and the different set-up's. To illustrate the measurements done with these set-up's, results for a diffusion/well (p^+/n^-) diode will be presented. This detector, although it does not show the best photoresponse in the visible spectrum, presents the possibility of implementing antiblooming structures in 2 dimensional arrays through the $p^+/n^-/p^-$ vertical bipolar junction transistor [9]. Excess charges generated by strong incident light are drained away by the vertical transistor, preventing these charges from leaking to neighboring pixels. Its behavior has been studied for a double poly, double metal 0.8 μm technology.

4. Electro-optical characterization

The characterization of the detectors is done by implementing different set-up's where both optical elements and electrical instruments are appropriately combined to determine the electrical response of the detectors to optical stimuli. All these elements are controlled through a GPIB (IEEE488) National Instruments card by the HP-VEE program which is run on a Personal Computer.

In this section there will be first given a description of the elements forming the measurement system. Afterwards two different set-up's implemented for the measurement of the spectral response and the optical dynamic range of the detectors will be presented.

4.1 Description of the measurement system

The different set-up's used for the characterization of the detectors are mounted on a Newport optical table, with a honeycomb core table top and a working surface showing an array of closely spaced mounting holes which provides a method for attaching the different elements of the set-up, preserving the alignment of the whole system.

A 250W halogen-quartz Jobin-Yvon lamp is used as a light source, since this type of light sources shows an approximately flat output power all over the visible spectrum. The lamp housing is coupled to an H-10 Jobin-Yvon monochromator which includes a visible grating, obtaining an output light with a minimum bandpass of 4 nm in the 350-800nm range. A stepper motor, which is connected to an IEEE-488 controller, is coupled to the grating holder, controlling the position of the grating and therefore the output wavelength.

A long band pass filter with a cut-off wavelength of 400nm is placed at the output of the monochromator to eliminate second order harmonics originated by the grating. A biconvex lens is situated after the filter to collimate the output light beam.

A long optical rail placed along the monochromator optical axis, as can be seen in Figure 4, is used to move the different elements at positions or distances from the monochromator output different than those allowed by the table top holes. The optical rail is attached to the table top to avoid any misalignment of the system.

The detector to be measured (or Device Under Test, D.U.T.) is mounted on a home-made vertical support and aligned to the output beam.

An 818-SL/CM Newport calibrated silicon detector coupled to an 1830-C Newport optical power meter is used to determine the optical power incident on our detectors. The optical power meter has an IEEE-488 interface to allow computer control.

To make automatic and simultaneous measurements of both the detected signal and the incident light power, an OPTICS for RESEARCH metallic beamsplitter is used to split the light beam in two separate beams: one transmitted through the beamsplitter and the other reflected 90°. The transmitted beam arrives to the D.U.T. and the reflected beam arrives to the calibrated detector, which is located on an optical rail perpendicular to the monochromator optical axis and at the same distance as the D.U.T. (see Figure 4). The beamsplitter, which is placed forming an angle of 45° with the optical axis, transmits 36% of the total light power, reflects 33% and absorbs 31% all over the visible spectrum. This element is not strictly necessary, although its use helps to automate the system and reduce the complexity of the measurement procedures.

An HP3245A power supply is used to polarize the detectors, and a 6512 Keithley electrometer measures the photogenerated current.

A set of Newport calibrated neutral density filters is used to decrease the light beam power. These filters present a uniform transmittance in the visible spectrum, and are mainly used to determine the dynamic range of the detectors.

A set of interference band pass filters with center wavelengths ranging from 400nm to

1200nm each 50nm are also available for measurements not requiring very monochromatic light. These filters could be considered as an alternative to the use of a monochromator, which is one of the most expensive elements of the system. However, the number of wavelengths that could be measured would be limited by the number of available filters. Furthermore, the bandwidth of the filters is wider than that of the monochromator, producing an error in the measurement of the incident light power. Narrower filters can be used but its price can also be higher. However the automation of the measurement could be done by using a filter wheeler with a stepper motor which could be controlled through a IEEE controller, although the final price of the system would also increase.

Another halogen-quartz lamp is placed in a parallel set-up to allow achromatic measurements, and to be used with the interference band pass filters.

To avoid the influence of external light in the measurements, the optical table is covered with a black-painted home-made box, about one meter high, which has windows with blinds in three sides to access the different elements of the set-up. At the other side of the box, there is a set of coaxial connectors and small holes where electrical and GPIB cables can access the table top. The cables are surrounded by a black tissue, which is glued around the hole, to avoid light going through the hole.

When measuring 2 dimensional arrays of detectors, like those described in section 3, an HP-8175A digital signal generator is used to generate the 3 different words needed to select each detector. The HP-8175A has a IEEE-488 Interface which allow computer control.

Although only a limited number of measurement set-up's is presented here, the system can be easily adapted to other types of measurements. For instance, the dynamic response of

the detectors could be easily determined when using a LED (Light Emitting Diode) or a low power visible laser which can be modulated at different frequencies.

4.2 Electro-optical measurements

Two different types of measurements are done to characterize the detectors: measurements of the spectral response and measurements of the optical dynamic range. Both types of measurements will be described now.

4.2.1 Spectral response measurements

The spectral response of the detectors is obtained by mounting a very similar set-up to that depicted in Figure 4, although in this case the neutral density filters are not used. A 250W halogen-quartz lamp coupled to the monochromator is used as a monochromatic light source. Light going out of the monochromator is collimated before being splitted by the beamsplitter. The transmitted light impinges on the D.U.T. a current which is measured by the electrometer. The reflected light arrives to the calibrated detector, giving a measurement of the optical power incident on the D.U.T. (a small correction is done when calculating the quantum efficiency to take into account the ratio of transmitted to reflected light by the beamsplitter which is 36%/33%).

Diodes are reverse polarized by the HP3245A power supply, and the current flowing through them is measured by the 6512 Keithley electrometer. First the dark current is determined to eliminate this component of the measured current with illumination and obtain the actual photogenerated current. This subtraction of the dark current is done by software.

The wavelength of the incident light is controlled by the HP-VEE program through the

IEEE controller of the stepper motor, therefore eliminating the manual change of the output wavelength. For each wavelength the program reads the optical power and the photocurrent from the optical powermeter and the electrometer, respectively. The program directly operates these figures to depict in real-time the quantum efficiency of the detector on a graph, taking into account both the dark current and the ratio of transmitted to reflected light by the beamsplitter. The use of the beamsplitter helps to reduce the inaccuracy in this type of measurements since the optical power can be measured almost simultaneously to the photogenerated current in the detector. If the beamsplitter is not used, the spectral output power of the lamp has to be measured before or after the spectral response of the detector, introducing an error in the measurements since the output power of the lamp could have slightly changed.

The spectral response of the arrays of detectors can also be measured by using the HP-8175A digital signal generator. Then, once the wavelength is selected, the photocurrent is measured for all the different detectors of one or more arrays. The HP-VEE program is slightly modified for this measurement by introducing the selection of the different detectors with the digital word generator.

As an example of this type of measurement, the spectral response of a $100\mu\text{m}\times 100\mu\text{m}$ p^+/n^- diode can be seen in Figure 5. The ripple observed is due to multiple light interferences in the dielectric layers deposited on top of the detector, that depend on the dielectric layer materials and thicknesses. As expected, the quantum efficiency shows a maximum at short wavelengths (around 480nm) and then decreases with photon wavelength.

4.2.2 Optical dynamic range

Measurements of the optical dynamic range are done using the set-up shown in Figure 6.

A 250W halogen-quartz lamp is used together with an interference band-pass filter to select the light wavelength. One or more neutral density filters are also used to reduce the light power arriving to the detector. Once the power supply of the lamp is set, the optical power is measured with the calibrated detector in the exact position where the D.U.T. will be placed. Then the photogenerated current is measured with the electrometer without the neutral density filter to obtain the first data point. Afterwards this current is measured placing different calibrated neutral density filters in between the light beam and the D.U.T. to reduce the light power arriving to the detector. In this case the filters are placed manually since in some cases a combination of two or more filters is used. The optical dynamic range for a p^+/n^- diode is shown in Figure 6 for different wavelength. As it can be observed, the optical dynamic range measured is 4 decades of incident light. Higher light power could not be reached due to the limitations of our lamp; however, it is expected that the dynamic range will improve in about 3 decades of light intensity, corresponding to the values known from literature.

5. Conclusions

An electro-optical measurement system for the DC characterization of visible detectors is presented which can be used by vision chip designers to characterize these detectors. This measurement system is versatile, fast and easily expandable and used. Two different type of measurement are done: spectral response and optical dynamic range measurements. For the first type of measurements, the set-up is computer controlled, avoiding tedious and inaccurate measurements. A set of detector test structures for the characterization of a technology process is also given which can help designers in the selection of the detector better suited to their application. Results are presented for both types of measurements for diffusion/well diodes

processed in a double poly, double metal 0.8 μm technology.

Acknowledgments

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References

- [1] E. R. Fossum, "CMOS image sensors: Electronic camera on a chip," *Int. Electron Device Meetings*, p. 17, 1995.
- [2] H.-S. Wong, "Technology and device scaling considerations for CMOS imagers," *IEEE Transactions on Electron Devices*, Vol. 43, No. 12, pp. 2131-2142, 1996.
- [3] A. Moini, *Vision Chips or Seeing Silicon*, Technical Report, Centre for High Performance Integrated Technologies and Systems, The University of Adelaide, March 1997.
- [4] R. Domínguez-Castro, S. Espejo, A. Rodríguez-Vázquez, R. Carmona, Péter Földesy, Ákos Zarándy, Péter Szolgay, Tamás Szirányi and Tamás Roska: "A 0.8 μm CMOS 2-D Programmable Mixed-Signal Focal-Plane Array Processor with On-Chip Binary Imaging and Instructions Storage". *IEEE J. Solid-State Circuits*, Vol. 32, No. 7, pp. 1013-1026, July 1997.
- [5] S.M. Sze, *Physics of Semiconductor Devices*, 2nd edition, John Wiley & Sons, 1981.
- [6] J. Mann, "Implementing early visual processing in analog VLSI: light adaptation", *Proc. of SPIE, Visual Information Processing: from neurons to chips*, Vol. 1473, pp. 128-132, 1991.

- [7] W.C Dash and R. Newman, "Intrinsic optical absorption in single-crystal germanium and silicon at 77K and 300K," *Physical Review*, Vol. 99, pp. 1151-1155, 1955.
- [8] T. Delbrück, *Investigations of Visual Transduction and Motion Processing*, Ph. D. Thesis, Computational and Neural Systems Program, California Institute of Technology, 1993.
- [9] C.H. Aw and B.A. Wooley, "A 128x128-pixel standard-CMOS image sensor with electronic shutter", *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 12, pp. 1922-1930, December 1996.

Figure captions

Figure 1. Junction devices available in a standard n-well CMOS process for visible light detection. The complementary structures are obtained in a p-well process. The active junction is shaded for each device. (a) Well/substrate (n^-/p^-) diode. (b) Diffusion/substrate (n^+/p^-) diode. (c) Diffusion/well (p^+/n^-) diode. (d) Vertical bipolar transistor ($p^+/n^-/p^-$).

Figure 2. Lay-out of a dedicated test chip for the characterization of junction photodetectors. The metal2 layer, which covers most of the chip area, is not shown to allow a clear image of the lay-out

Figure 3. Lay-out of the junction devices available in a standard CMOS process for visible light detection. (a) Well/substrate diode. (b) Diffusion/substrate diode. (c) Diffusion/well diode. (d) Vertical bipolar transistor.

Figure 4. Schematic representation of the different elements of the electro-optical measurement system. The set-up indicated in the figure is used for spectral response measurements, although for these measurements the neutral density filter is not included.

Figure 5. Measurement of the spectral response of a p^+/n^- diode. The ripple observed is due to

multiple light interferences in the dielectric layers deposited on top of the detector.

Figure 6. Schematic representation of the set-up used for the measurements of the optical dynamic range.

Figure 7. Optical dynamic range for a diffusion/well diode at different light wavelengths.

Figure 1

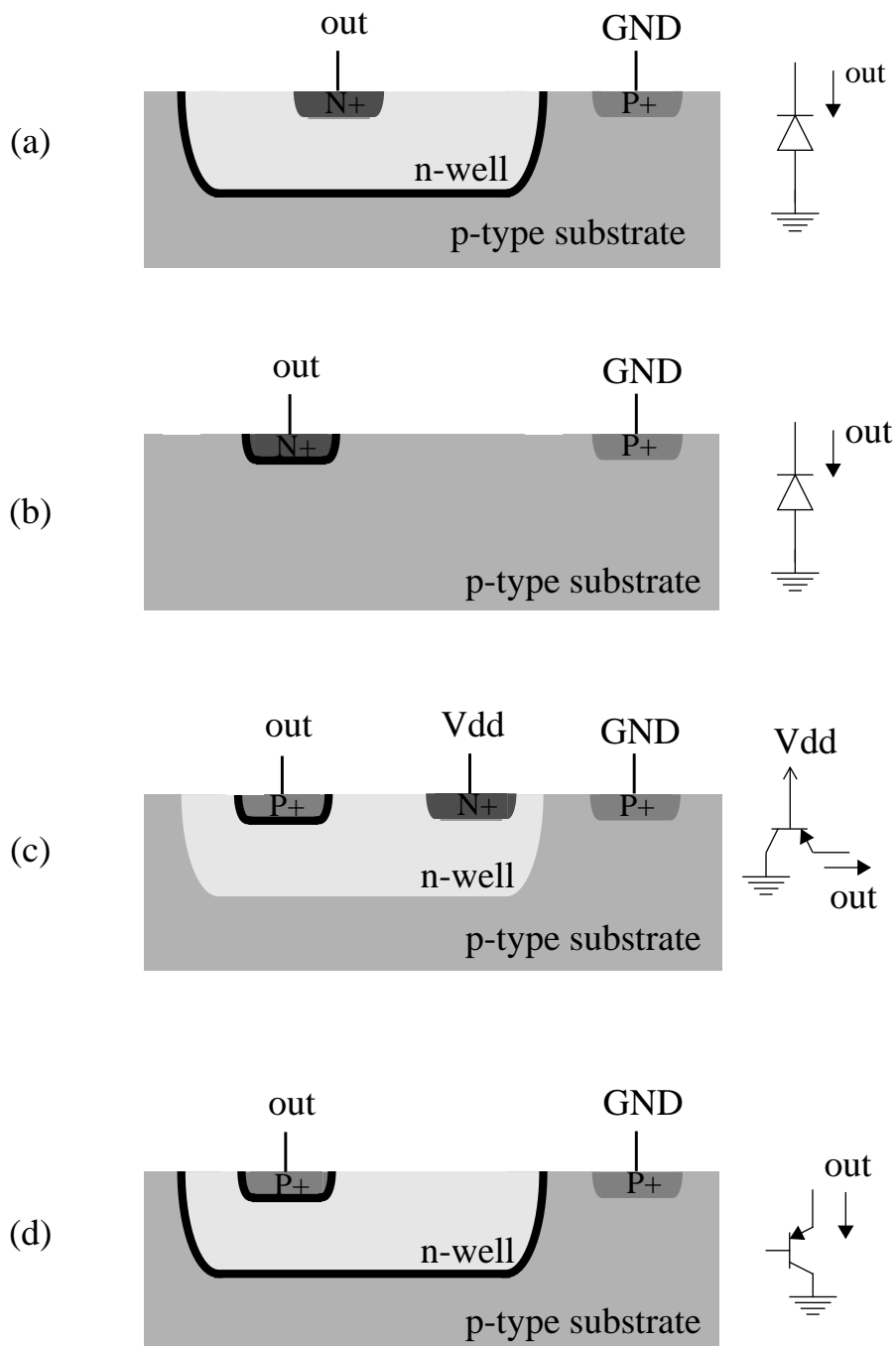


Figure 2

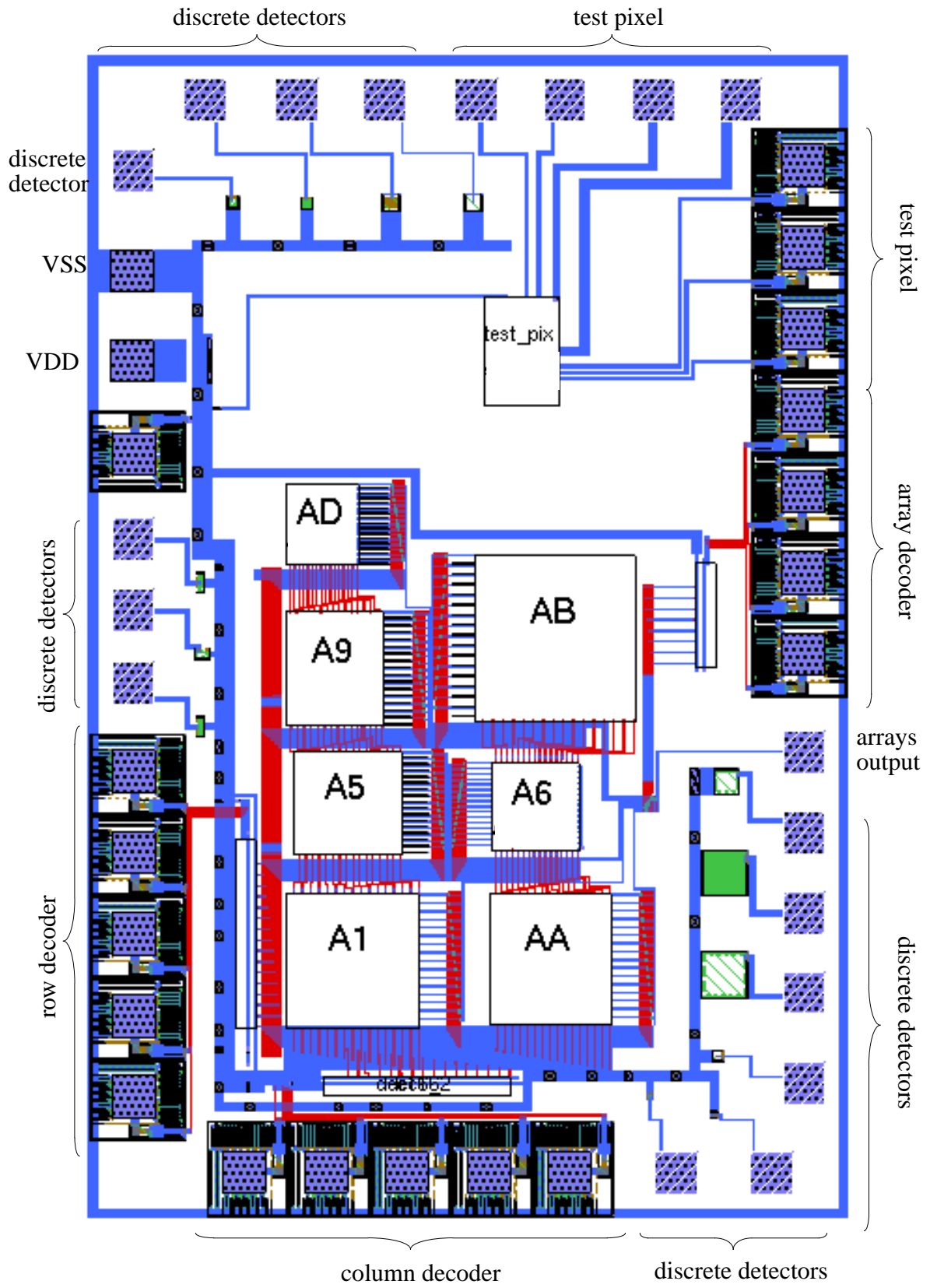


Figure 3

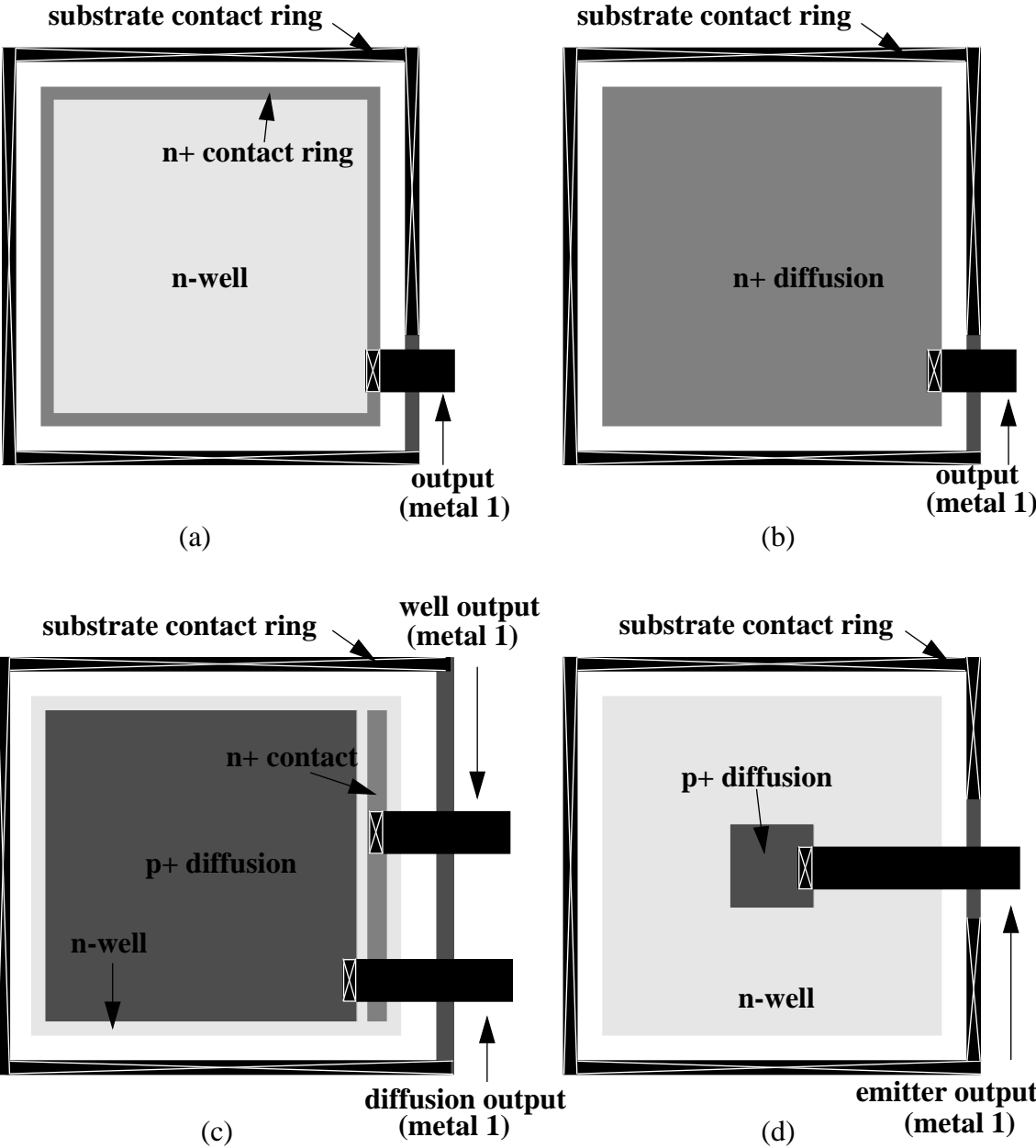


Figure 4

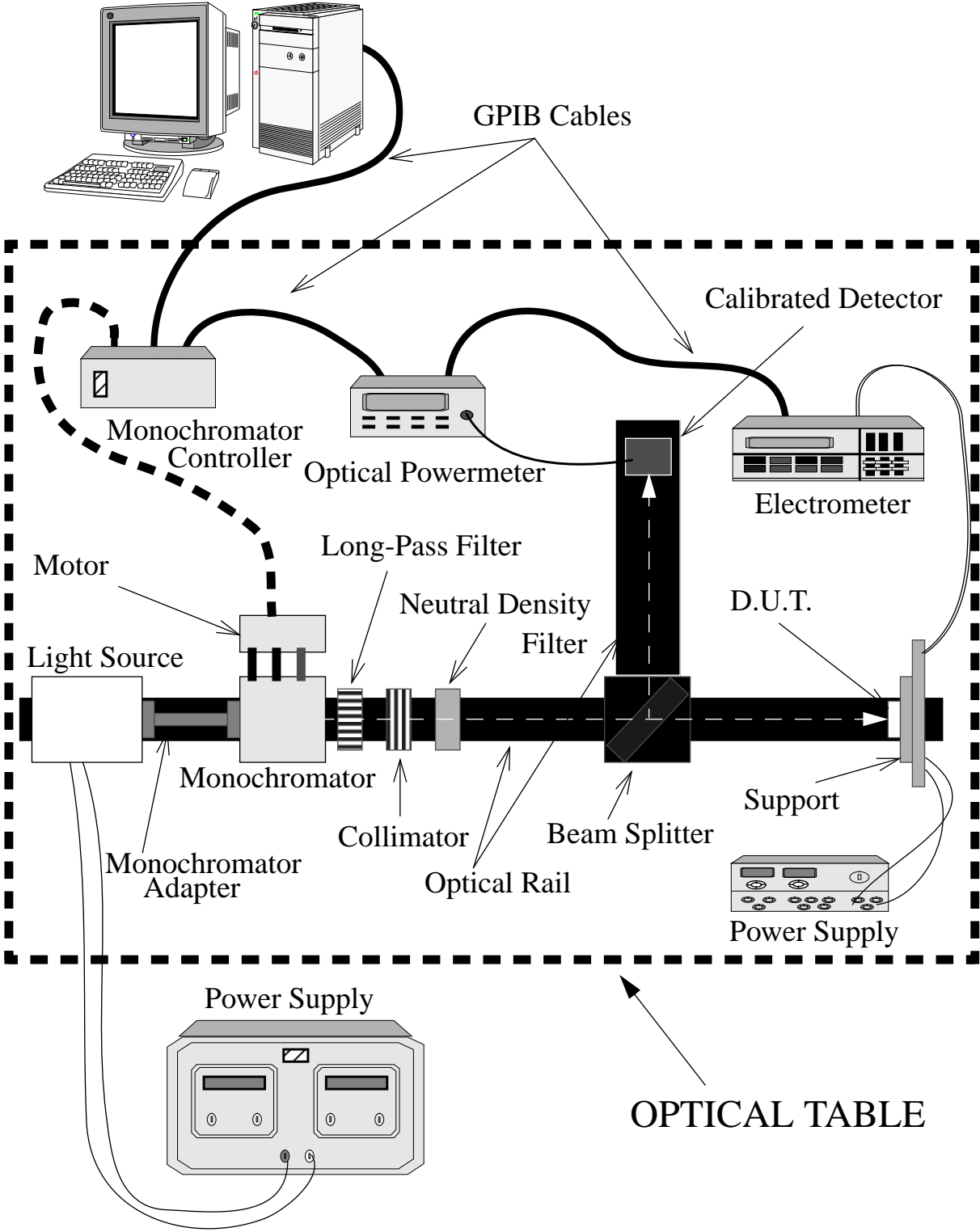


Figure 5

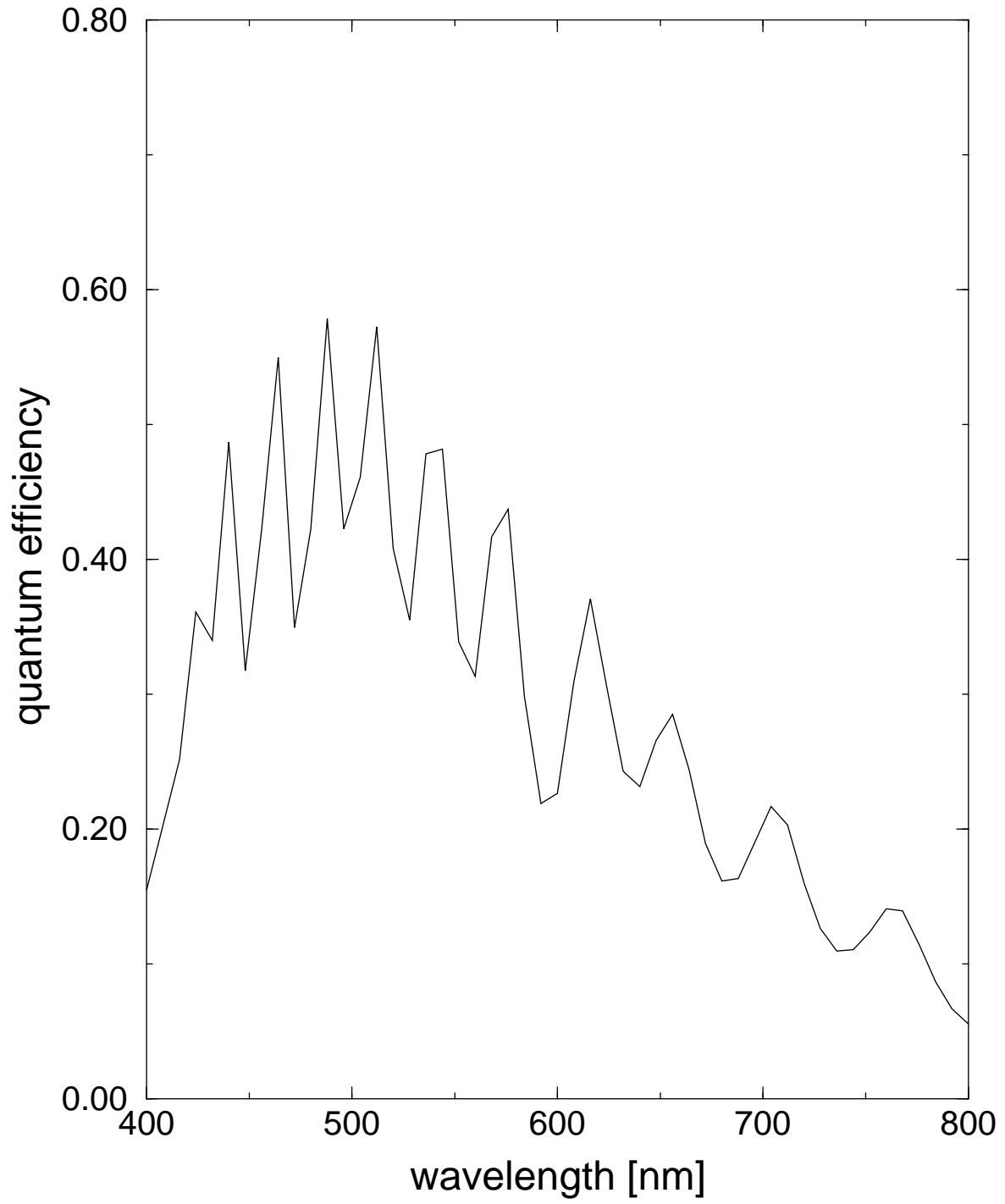
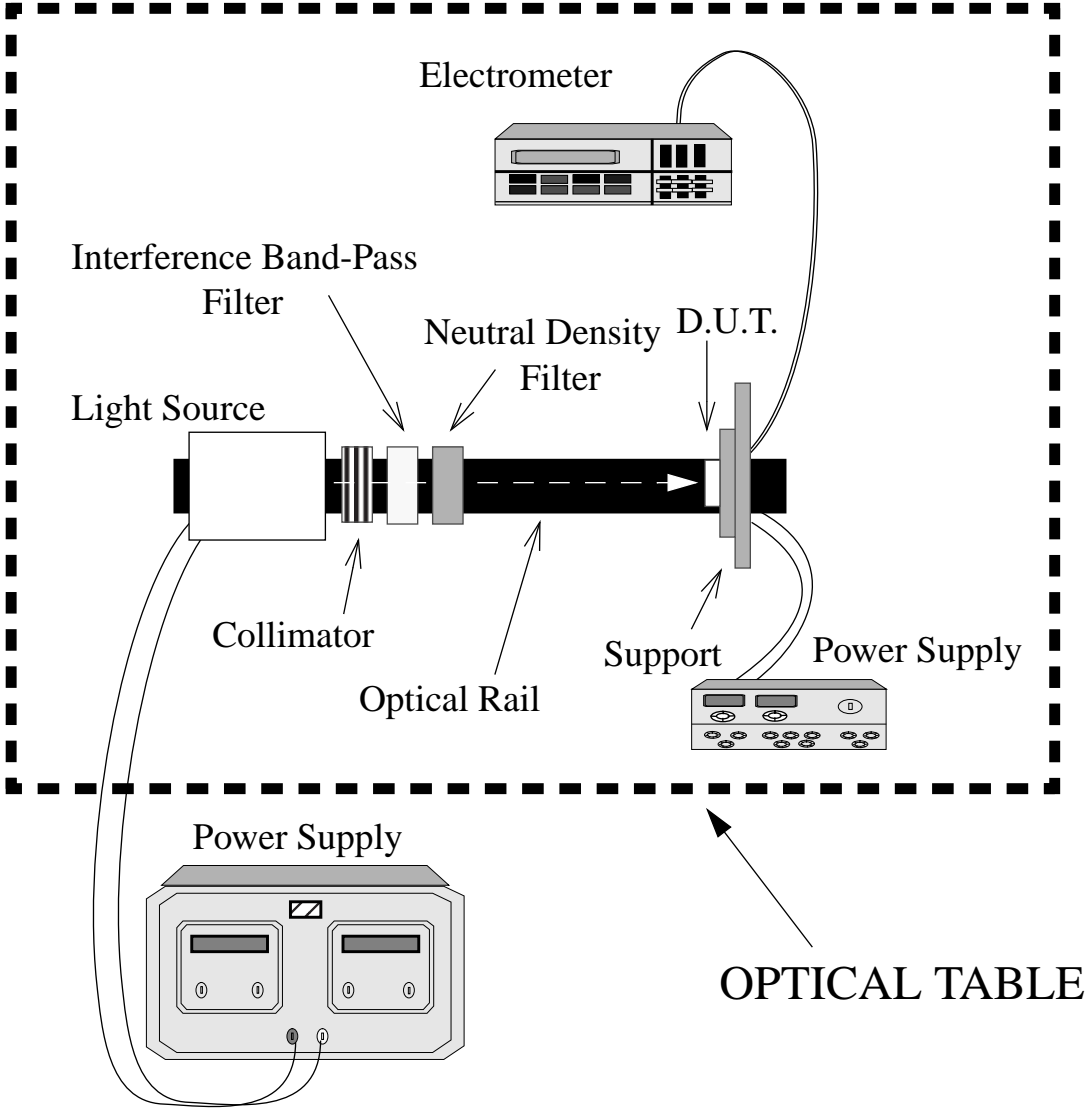


Figure 6



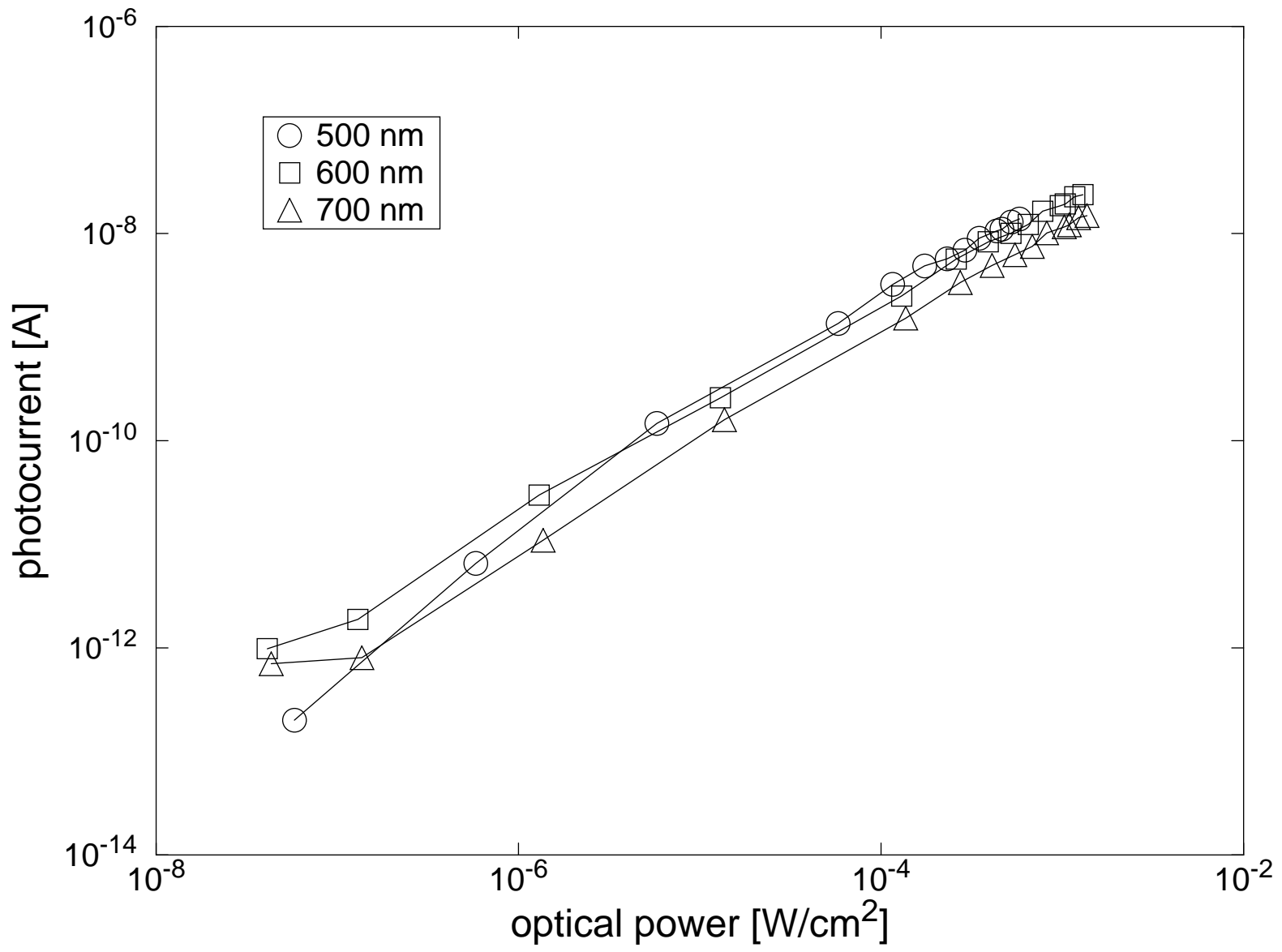


Figure 7