Selective Harmonic Mitigation Technique for multilevel Cascaded H-bridge Converters

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Abstract—The increasing demand of energy and proliferation of non-linear loads have leaded to the appearance of new grid codes which limit the maximum acceptable harmonic levels. In this context, multilevel topologies are very attractive because can generate output waveforms with a low harmonic content using a low switching frequency. In this paper, the recently presented selective harmonic mitigation technique (SHMPWM) is adapted to a nine-level converter. Its flexibility is exploited to meet the EN 50160 and CIGRE WG 36-05 grid codes without any additional filtering system using 10 switching angles per quarter of period in a wide range of amplitudes of the fundamental harmonic from 0.70 to 1.22. Some results validating this technique applied to this topology are presented. A comparison with the well known selective harmonic elimination method is included showing the advantages of the SHMPWM technique.

I. INTRODUCTION

The power losses when solid state devices are used limit the maximum switching frequency that can be used in a power electronic converter. Reducing the number of switchings per cycle generates higher harmonic content. In order to reduce the harmonic distortion content, an appropriate modulation technique has to be chosen. Another strategy to reduce the harmonic content keeping the number of switchings is increasing the number of levels of the converter using a more complex topology. This fact leads to a higher number of devices but it could save energy and the extra cost of filtering systems.

Several studies related with pulse width modulation (PWM) techniques have been published presenting different strategies to generate the most interesting harmonic content. The well known selective harmonic elimination (SHEPWM) technique [1] can set the amplitude of the fundamental harmonic and make it zero the amplitude of \( k - 1 \) desired harmonics (if \( k \) switching angles are used per quarter of period). The recently presented selective harmonic mitigation technique (SHMPWM) [2], [3] generates output waveforms that completely fulfil specific grid codes (for instance, the EN 50160 [4] and CIGRE WG 36-05 [5]) with a lower switching frequency than SHEPWM.

The SHMPWM technique has been previously presented using a three-level converter but, as happens with the SHEPWM technique, it can be extended to converters with a higher number of levels independently of the specific converter topology. Several papers dealing with the SHEPWM technique applied to these type of converters have been previously published [6], [7]. This paper presents the results obtained using the SHMPWM technique in a nine-level converter. In this case, the study is focused on the application of the SHMPWM to a two-cell cascaded H-bridge converter (2-cell CHB) with a dc voltage ratio equal to 1:3. However, it has to be noticed that other nine-level converter topologies as the diode-clamped or flying capacitor [8]–[10] could use exactly the same switching angles achieving the same results.

This paper is organized as follows; in section II the characteristics of the topology under study are summarized. Next section describes the SHMPWM principle and how it is extended to a nine-level topology. In section IV, the results obtained using the SHMPWM method are presented. Finally, the conclusions of the paper are detailed.

II. NINE-LEVEL CASCADED H-BRIDGE TOPOLOGY

Several three-level power cells formed by full H-bridges can be associated to build a converter with a higher number of levels as can be observed from Fig. 1. In fact, connecting several three-level cells it can be obtained a converter with many levels as desired [9]. In general, if \( n \) power cells are connected in series to build the converter and all the cells have the same dc voltage, the number of levels that can be achieved is \( 2n+1 \). This topology is named \( n \)-cell CHB converter and it presents great properties as a high modularity and reduced number of switches.

A very interesting multilevel converter topology based on the cascaded H-bridge concept can be obtained connecting two three-level cells (called in this work 2-cell CHB) with different dc voltages. This topology is represented in Fig. 1 where the dc voltages are denoted by \( V_A \) for the upper cell and \( V_B \) for the lower cell respectively. The number of levels depends on the ratio of the dc voltages (\( V_A/V_B \)) as can be observed in Table I. A very interesting case is obtained when the dc voltage ratio is 1:3, i.e. \( V_B=3V_A \), because nine symmetrical levels are obtained using a low number of switches.

The disadvantage of this topology is that, as two different dc sources are needed, the converter is not symmetrical. The modularity property, present on the symmetrical CHB topology is lost when the dc voltages are different. Usually, different power semiconductors are needed in order to build the converter, i.e. IGBTs and IGCTs are used for the lowest and highest voltage cells respectively. The switching frequency
of the highest voltage cell has to be very low to reduce the power losses as possible. In this way, a very suitable modulation method for asymmetrical CHB converters is the hybrid modulation where the highest voltage cell provides the main portion of the output voltage (with very low switching frequency) and the lowest voltage cell provides the high frequency components of the output voltage [11]. However, although the asymmetrical CHB topology is more complex due to the different nature of the power semiconductors, as the number of levels is increased, high quality output waveforms are achieved improving the harmonic response. As the power losses can be below acceptable limits obtaining a high performance, this converter topology is very interesting in high power applications.

III. SHMPWM PRINCIPLE

A. Three-level converters

The typical three-level waveform with \( k \) switching angles \( \alpha_i \) \((i=0,...,k-1)\) (Fig. 2) generates a harmonic content which can be studied using the Fourier analysis [12]. The amplitude of each harmonic can be obtained using the following expression where \( H_j \) is the amplitude of the \( j^{th} \) harmonic:

\[
H_j = \frac{4V}{j\pi} \sum_{i=0}^{k-1} (-1)^i \sin(j\alpha_i) \tag{1}
\]

The well known SHEPWM technique try to reduce the harmonic content using this expression to set the amplitude of the \( 1^{st} \) order harmonic to a desired value (called modulation index \( M_a \)) and reducing to zero the amplitude of a limited number of harmonics. Using a \( k \) switching angles waveform a maximum of \( k-1 \) harmonics can be zeroed. Normally, the lowest odd non-triplen harmonics (5, 7, 11,...) are the most interesting orders to be eliminated. This is because, due the symmetry of the waveform, even harmonics have zero amplitude and in topologies without neutral connection, triplen harmonics can not appear.

Summarizing, the SHEPWM technique for three-level converters [13] is based on solving the following system of equations where \( q \) is the highest harmonic order zeroed:

\[
H_1 = \frac{4V}{\pi} \sum_{i=0}^{k-1} (-1)^i \sin(\alpha_i) \\
0 = \frac{4V}{j\pi} \sum_{i=0}^{k-1} (-1)^i \sin(j\alpha_i),
\]

where \( j = 5, 7, 11,..., q \). \( \tag{2} \)

The SHMPWM technique is based on the idea that it is not necessary reducing to zero the amplitude of the harmonics. They just have to be decreased under convenient levels where they can be acceptable. The appropriate harmonic content levels can be obtained from the limits specified in the actual grid codes.

The SHMPWM technique can be formulated with the following system of inequalities where \( M_a \) is the modulation index and \( L_j \) is the maximum limit of harmonic \( j^{th} \):

\[
E_1 = |M_a - H_1| \leq L_1 \\
E_j = \frac{1}{|H_1|} \frac{4V}{j\pi} \sum_{i=0}^{k-1} (-1)^i \sin(j\alpha_i) \leq L_j,
\]

where \( j = 5, 7, 11,..., 49 \). \( \tag{3} \)
The system (3) can be arranged into an objective function in order to use an optimization method to minimize it. This function could be as follows:

\[
OF(\alpha_0, \ldots, \alpha_{k-1}) = \sum_{i=1}^{49} c_i E_i^2 + c_{THD} THD. \tag{4}
\]

The \(c_i\) coefficients are modeled as non-linear functions. For each harmonic, if the amplitude is higher than 80% of the limit \(L_j\) in (3)) then \(c_i = 1000\) else \(c_i = 1\). The same criterion is used with the total harmonic distortion (THD) and the fundamental harmonic amplitude \(M_k\). In this way, the algorithm searches the most appropriate switching angles to minimize the \(OF\). In this case, up to harmonic 49\(^{th}\) are considered.

### B. Nine-level converters

Considering for instance a waveform as shown in Fig. 3 with \(N\) levels, output voltage levels \(V_i\) \((i=1, \ldots, (N-1)/2\) with \(N\) odd) and \(k\) switching angles \(\alpha_i\) \((i=0, \ldots, k-1)\) the Fourier analysis gives:

\[
H_j = \frac{4}{j\pi} \left[ V_1 \sin(\alpha_0) + \sum_{i=1}^{k-1} \left[ V_i \sin(j\alpha_i) - \sin(j\alpha_{i-1}) \right] \right]. \tag{5}
\]

The SHEPWM can also be applied to this kind of converters [14]. Again, solving the equations, the fundamental harmonic can be set to the desired value and \(k-1\) harmonics can be reduced to zero. The new system of equations would be:

\[
H_1 = \frac{4}{\pi} \left( V_1 \sin(\alpha_0) + \sum_{i=1}^{k-1} \left[ V_i \sin(\alpha_i) - \sin(\alpha_{i-1}) \right] \right)
\]

\[
0 = \frac{4}{j\pi} \left( V_1 \sin(\alpha_0) + \sum_{i=1}^{k-1} \left[ V_i \sin(j\alpha_i) - \sin(j\alpha_{i-1}) \right] \right),
\]

where \(j = 5, 7, 11, \ldots, q\). \tag{6}

The SHMPWM can also be applied to converters with more than three levels. Applying again the SHMPWM principle, based on reducing the harmonic amplitudes to a safe value but higher than zero, the system of equations changes to the following system of inequalities:

\[
E_1 = |M_a - H_1| \leq L_1
\]

\[
E_j = \frac{1}{|H_1| j\pi} \left( V_1 \sin(\alpha_0) + \sum_{i=1}^{k-1} \left[ V_i \sin(j\alpha_i) - \sin(j\alpha_{i-1}) \right] \right) \leq L_j, \quad \text{where } j = 5, 7, 11, \ldots, 49. \tag{7}
\]

Again, the whole system can be grouped in the same objective function (4) where the \(c_i\) coefficients are modeled as the non-linear functions defined in section III-A.

Several optimization methods as Tabu Search, Ant Colony or Particle Swarm [15]–[17] can be used to solve the system. As in previous works, in this paper, the well known simulation annealing optimization method [18], [19] has been chosen because using it is very simple to adapt the system from three to nine levels. Anyway, it has to be noticed that the optimization method itself is not very important because it has to be executed once as all the calculations are done off-line.

It must be noticed that using the SHEPWM or the SHMPWM techniques, the waveform shape is completely fixed because they are pre-programmed PWM techniques. In multilevel converters with more than three levels, different waveforms using the same number of switching angles can be used. The optimization method used to minimize the objective function does not change the waveform shape but it only determines the switching angles.

It can be noticed that any waveform with nine output voltage levels can be generated with any nine-level converter: 9-level diode-clamped converter, nine-level flying capacitor or a four-cell symmetrical CHB (four series connected full H-bridges with the same dc voltage). However, this paper is especially focused on the asymmetrical 2-cell CHB with dc voltage ratio 1:3. As the cells are not symmetrical in this topology, the shape of the different waveforms to be generated by this topology have been chosen in order to reduce as maximum as possible.
the number of switchings of the cell with maximum voltage. In Fig. 4 is detailed how the waveform is generated combining the outputs of both cells. All the waveforms considered for the SHM PWM technique applied to this asymmetrical converter only switch the highest voltage cell once per quarter of a cycle as can be observed from 4. This concept was also used in the hybrid modulation technique in order to reduce the power losses of this asymmetrical converter [11].

In addition, in order to improve the results of the SHM PWM technique, using the same switching frequency, the shape of the waveform is previously adapted to the $M_a$ considered in each case. In this work, it has been used three different waveforms for three ranges of $M_a$ (Fig. 5). In all the proposed cases in Fig. 5, only one switching per quarter of a cycle is needed in the highest voltage cell.

IV. Obtained Results

This section presents the results obtained using the SHMPWM technique in a nine-level 2-cell CHB converter. In order to obtain solutions which could be easily implemented in a real converter, real power semiconductors have been considered. A minimum margin of 0.01 radians between two consecutive switching angles has been taken into account as in [20]. In the computing process the limits specified in the EN 50160 [4] and CIGRE WG 36-05 [5] grid codes have been considered but any other could have been chosen. They include specific limits for each harmonic up to $49^{th}$ and for the THD considering harmonics up to $40^{th}$. In Table II are detailed all the limits specified in these specific grid codes.

Fig. 6 shows the maximum harmonic amplitude in the whole range of $M_a$ (worst case) obtained using the SHMPWM technique and the maximum limit imposed by the applied grid code. It must be noticed that for all the harmonics of interest, the worst case is always under the limits specified in the grid code. This means that using the 10 switching angles $\alpha_i$ determined by the SHMPWM technique, the grid code is met and the output filtering component, usually present in the power converters, can be avoided. This fact leads to an important economical cost, weight and volume reduction of the power system.

In order to compare the results with other previous techniques, the SHEPWM method has been studied following the same waveforms presented in Fig. 5. Once the 10 switching angles are determined, they are applied to obtain the results for the nine-level 2-cell CHB converter. The results of the comparison between the SHEPWM and the SHMPWM are presented in Fig. 7 and Fig. 8 where a modulation index $M_a$ equal to 1.02 and 1.12 respectively is considered. It can be observed that all the harmonics from the SHPWM result are below the limits imposed by the grid code (as expected from Fig. 6). In front of this fact, using the SHEPWM technique, low order harmonics are zeroed but several harmonics from $31^{st}$ up to $49^{th}$ are above the maximum limits. This fact shows that using the SHEPWM technique needs a high cost filtering system in order to reduce the harmonic content of the output waveform. This filter, as commented above, is avoided when the proposed SHMPWM technique is used.

![Fig. 4. Generation of the waveforms from the outputs of both cells. Detail of one quarter of a period. From top to bottom: a) Total phase voltage b) Output voltage of the highest voltage cell c) Output voltage of the lowest voltage cell.](image)

![Fig. 5. Nine level waveforms used with the SHPWM technique. Each shape is more suitable for different ranges of the modulation index $M_a$. From top to bottom: a) $0.7 \leq M_a \leq 0.9$ b) $0.9 < M_a \leq 1.10$ c) $1.11 \leq M_a \leq 1.22$.](image)
TABLE II
GRID CODE EN 50160 REQUIREMENTS + QUALITY GRID CODE CIGRE WG 36-05

<table>
<thead>
<tr>
<th>Harmonic order (n)</th>
<th>Relative Voltage ($L_i$)</th>
<th>Harmonic order (n)</th>
<th>Relative Voltage ($L_i$)</th>
<th>Harmonic order (n)</th>
<th>Relative Voltage ($L_i$)</th>
</tr>
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<td>3</td>
<td>5%</td>
<td>2</td>
<td>2%</td>
</tr>
<tr>
<td>7</td>
<td>5%</td>
<td>9</td>
<td>1.5%</td>
<td>4</td>
<td>1%</td>
</tr>
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<td>15</td>
<td>0.5%</td>
<td>6...10</td>
<td>0.5%</td>
</tr>
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<tr>
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<td>&gt;25</td>
<td>0.2+32.5/n</td>
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</table>

SHMPWM results in the range $0.70 < M_a > 1.22$

Fig. 6. Maximum harmonic amplitudes obtained using the SHMPWM technique in the $M_a$ range from 0.70 to 1.22.

SHMPWM versus SHEPWM with $M_a = 1.02$

Fig. 7. Harmonic amplitudes obtained using the SHEPWM and the SHMPWM techniques for a modulation index $M_a$ equal to 1.02.

V. CONCLUSION

In this paper, the SHMPWM technique has been implemented with a nine-level cascaded H-bridge converter. Although the proposed modulation technique can be applied to any nine-level converter, the study is especially focused on a two non-symmetrical cells cascaded H-bridge topology because it can generate up to nine levels with a low number of power semiconductors. The shape of the waveforms of the pre-programmed SHMPWM technique have been chosen in order to reduce as maximum as possible the number of switchings in the cell with highest voltage. In all the cases only one switching in the highest voltage cell is needed per quarter of
period reducing therefore the overall switching losses of the power converter.

In the computing process, real power devices have been considered and a minimum margin of 0.01 radians between two consecutive switching angles has been taken into account in order to obtain solutions which can be implemented in the real converter.

In this paper, the SHMPWM technique can generate output waveforms with ten switching angles per quarter of cycle with very low harmonic content which can meet the EN 50160 and CIGRE WG 36-05 grid codes without any additional filtering system. Different waveforms have been used in order to adapt the shape to the desired modulation index $M_a$.

Some results validating the method are included showing the improvements obtained with this technique in comparison with the well known SHEPWM technique.

ACKNOWLEDGMENT

The authors would like to thank the Computing and Scientific center of Andalucia where its computing service has offered their facilities to obtain most of the results presented in this paper. Also, the authors gratefully acknowledge financial support provided by the Spanish Ministry of Science and Technology under project TEC2006-03863.

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