MODASC: ASIC for Mobile Data Acquisition Systems using Satellite Communications

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Abstract— **MODASC is an ASIC that performs wide area mobile data acquisition using satellite communication to provide global coverage. This circuit provides two operation modes: an *autonomous mode*, that periodically establishes connection with the control center, and a *slave mode*, working as a peripheral connected to a general purpose micro controller. This experiment has been realized under FUSE special action in collaboration with SAINSEL.**

I. Introduction

Most data acquisition systems make use of communication channels to send captured data to the control center. These communication channels are usually radio links, local computer networks or dedicated telephone lines. The selection of the most suitable communication channel is determined by taking into account application parameters, such as distance, installation and transmission costs, liability,... All previously mentioned communication channel alternatives are used for fixed installations or mobile stations in a local area. But when wide area data acquisition is required, satellite communication is the most valid alternative because it provides global coverage.

In this paper we present an ASIC designed to acquire data and send it to a control center via Inmarsat. This circuit provides two operation modes: an *autonomous mode*, that periodically establishes connection with the control center, and a *slave mode*, working as a peripheral connected to a general purpose microcontroller.

II. Functional Description

The functionality of this circuit can be summarized as remote data acquisition and communication using satellite links.

As it has been mentioned above, this circuit present two different operation modes: an *autonomous mode* and a *slave mode*.

In the first mode, the circuit uses the Data Communication Equipment (DTE) GALAXY-C/GPS from TRIMBLE [1]. This transceiver uses Inmarsat Standard-C satellite communication protocol and also receives signal according to GPS standard. The DTE/ASIC physical interface is over an RS-232 link.

In the second mode, this connection and its protocol are no longer needed, although they can be easily implemented using one of the 5 available serial channels implemented in MODASC.

The mode selection is determined by pin named CONFIG, where 0 and 1 indicates autonomous and slave modes respectively. As both modes are independent, bellow they are explained in different sections.

A. Autonomous Mode

In this mode MODASC captures environmental data and also determines its position using GPS. According to a predetermined schedule, MODASC waits until the control center establishes a connection, sending queries to determine ASIC present status.

In figure 1 a block diagram of autonomous mode is shown. In this mode, the most critical issue is to ensure power supply to guarantee proper operation and location of the system. Therefore, energy consumption minimization should be taken. MODASC internally stores sensor information and receives GPS position from the transceiver. All this data is periodically sent to the control center.

The functionality of the circuit is completed with

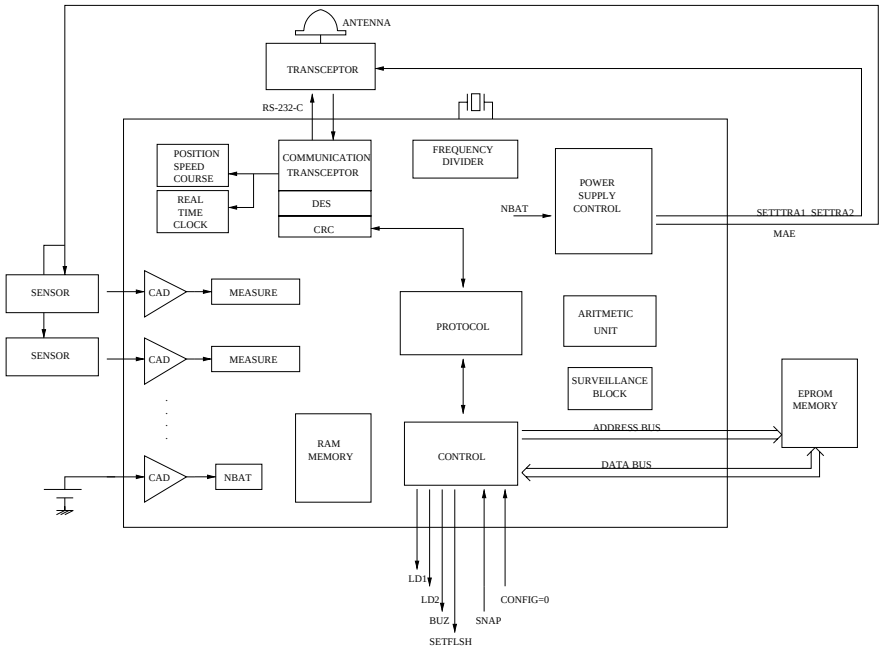

Figure 1: ASIC functional diagram in autonomous mode

violation sensors, optical and acoustical signals to indicate functional status, control block, arithmetic unit, frequency divider and internal configuration registers.

MODASC is connected to the GALAXY transceiver using RS-232-C. In order to achieve maximum compatibility with other transceivers, the communication between ASIC and GALAXY utilizes STANDARD-C Inmarsat Protocol when possible. The Communication Module is devoted to this communication protocol.

To achieve data privacy, standard encryption algorithm (DES)[2] is implemented in MODASC. To verify data integrity, CRC code is added at the end of every message.

The Power Supply Module deals with power consumption, activating peripherals only when it is needed. The activation schedule can be determined using programmable timers. This module also supervises battery voltage level. When this voltage level is bellow a predefined reference (50%), MODASC begins working in *energy saving mode*. When in this mode, its functionality is reduced to provide communication with the control center.

The Analog Signal Acquisition Module captures environmental analog data. Eight ten-bit analog to digital stochastic converters [3] are implemented. The main advantage of these converters is that use purely digital technology, thus decreasing manufacturing costs.

A real-time clock is included to determine communication periods. This clock is update whenever ASIC receives GPS time.

The Global Control Module determines the global functionality of the system, including access to system buses.

The kind of messages used in INMARSAT-C protocol is the 'Store & Forward' class, chosen because of its high reliability and acceptable transmission cost.

For debugging facilities, an auxiliary serial port is connected to the serial port devoted to transceiver communication, as it is shown in figure 2. This way, when CONFIG is equal to 0 (autonomous mode), the auxiliary serial port receives all messages that are transmitted between transceiver and ASIC, and it can directly send data to the transceiver to be configured. In slave mode (CONFIG=1) serial ports are working independently.

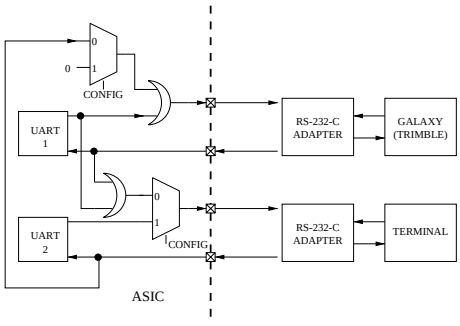

Figure 2: ASIC-Transceiver protocol monitoring in autonomous mode

B. Slave Mode

In this mode MODASC works as a peripheral to a standard microprocessor. In figure 3 a block diagram corresponding to the slave mode is shown. An 8-bit data bus, 6-bit address bus, $R/\bar{W}$ and $\bar{CS}$ are microcontroller's signals to access ASIC data. In this mode, MODASC provides 5 serial commu-

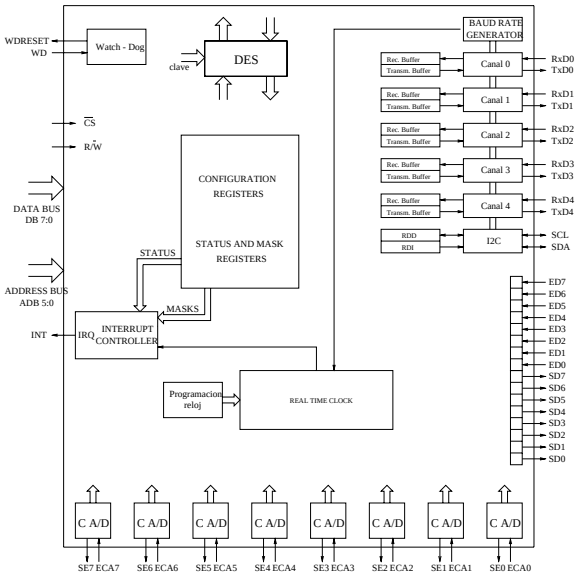

Figure 3: ASIC functional diagram in slave mode

nication ports. They manage 8 data, one start and one stop bits. Whenever an UART receives one data byte, it generates an external interruption. Similarly, when one data byte is written in the transmission register, it is automatically transmitted. When this buffer empties, the corresponding state flag is activated. There exist a mask register to deactivate interruptions, and an error register to indicate frame errors.

Another communication block implements a simplified version of an I^2C bus [4]. This is a synchronous serial communication channel, that utilizes only two lines: a bidirectional data line and a synchronization clock line. In our approach, this mode is considered to be master respect to peripheral circuits that work as slaves when they are connected to this port.

Communication frames are composed of 7-bit address, a R / W bit, one byte of data, and an reception acknowledge bit (see figure 4). The synchronization clock frequency is 100 K bits / s.

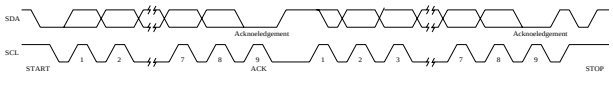

Figure 4: I^2C bus data transfer

Signal timing and electrical features comply specifications given in [4].

External control of I^2C bus is realized by writing and reading operations of corresponding output and input data registers. Available status register allows for control of this block. Both interrupt and polling management of this port is possible.

A Watch-Dog circuit has been included in ASIC functionality to prevent microcontroller from being blocked.

ASIC functionality is completed with 8 input and 8 output digital signals, 8 Analog to digital converters based on stochastic logic [3] as it is drawn in figure 5, a real time clock, and DES block

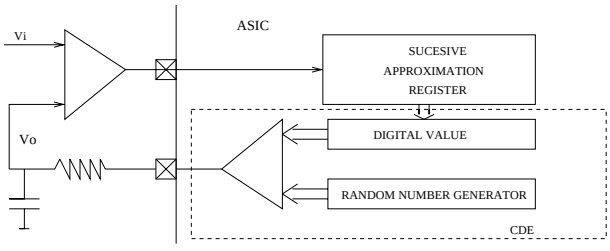

Figure 5: Block Diagram of an analog to digital converter based on stochastic logic

III. Implementation

Critical blocks, such as Inmarsat-C protocol, have been simulated in C language. Now, the hole system its being described in behavioral language (VERILOG [5]). The ASIC will be designed using CADENCE DESIGN FRAMEWORK II. The ASIC has a estimated area of $50mm^2$ using ES2 ECPD07 Standar Cell technology and PLCC-84 package has been selected.

References

[1] *GALAXY-C / GPS Users Manual. TRIMBLE. 1995*

[2] A.S. Tannenbaum *Computer Networks.* Prentice-Hall International. 1989.

[3] J.G. Ortega, C.L. Janer, J.M. Quero and L.G. Franquelo. *"Analog to Digital and Digital to Analog Conversion Based on Stochastic Logic"*. Proceedings IECON'95.

[4] *Philips Semiconductors 80C51-Based 8-Bit Microcontrollers*

[5] *Verilog-XL. Reference Manual, vol 1,2,3.* Cadence Design Systems, Inc.