Automatic Synthesis of Analog Fuzzy Controllers

R. G. Carvajal, A. Torralba, F. Colodro and L. G. Franquelo
Dpto. de Ingeniería Electrónica
Escuela Superior de Ingenieros,
Avda. Reina Mercedes s / n, Sevilla–41012 (SPAIN)
e–mail: carvajal@gte.esi.us.es

Abstract— **In this paper, a silicon compiler for analog fuzzy controllers is presented. The layout is automatically generated automatically, starting from a set of user specifications such as number of rules, number of inputs and maximum current (power consumption). This tool relies on a library of parametrizable basic cells designed in a CMOS 0.7 μm technology.The structure of the defuzzification part of the controller is based on the modular definiton made in [1]. This structure allows multi–input, multi–output fuzzy logic based controllers. It also a allows an easy extension of the controller (Serial or parallel conection of them to obtain controllers with more inputs or rules).**

I. Introduction

In the last few years, fuzzy controllers have found a large number of applications in fields such as automotive industry, robotics, power drives and home appliances [2]. Therefore, it is no longer strange to find fuzzy systems embedded in industrial ASICs. Hence, the architecture of these controllers is so frequently repeated, that automation is possible. Automation significatively shortens the design time, reducing the design cost. Different tools have recently been proposed to automate the hardware design of fuzzy controllers using a digital approach [3], [4], [5] or an analog approach [6]. Analog circuits are known to be inherently faster than digital circuits with significantly less power consumption and silicon area. On the other hand, digital circuits are superior in accuracy, extendability and ease of design. But in the both cases the design effort is high, so the developmet of tools to automate the design cycle is very convenient.
In this paper a silicon compiler for the automatic synthesis of analog fuzzy controllers is described. It is based on the modular structure proposed in [1]. This structure allows to split into modules, that uses a current mode approach. These modules form a library of parametrizable basic cells which are instantiated to build the controller that meets a set of user requeriments. Once the netlist is generated, the final layout can be obtained using Cadence Software.
This paper is organized as follows. Section II describes the design flow. The architecture of the controller is detailed in Section III. Section IV presents some results and advances future research.

II. Design Flow

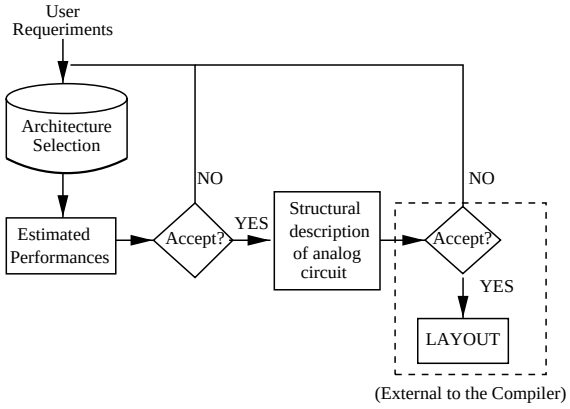

Figure 1: Design Flow

The design flow is depicted in figure 1. In a typical design, user specifications are related to number of inputs, number of outputs, number of rules, maximum bias current (power consumtion) and desired throughput.
The silicon compiler takes advantage of the fact that hardware fuzzy controllers are, in practice, composed of a set of basic building blocks, such as membership generators, max–min blocks and defuzzifiers.

III. Architecture of the Fuzzy Cotroller

The floor-plan of the fuzzy controller is shown in figure 2. As mentioned before it uses the modular structure proposed in [1]. This structure is based on the fuzzy singleton algorithm with the Mandani–type inference process and the center of gravity defuzzifier method.
As can be seen in the figure, this structure allows a variable number of inputs, outputs and rules. The automatic synthesizerconects these basic modules (library cells) to form the complete controller. The following building blocks can be identified in the fuzzy controller[7]–[8]:

1. The (MBF) Membership Function Generator. It uses the circuit proposed in [9] which is based on a linear tunable OTA proposed in [10]. It produces a fully programmable MBF's

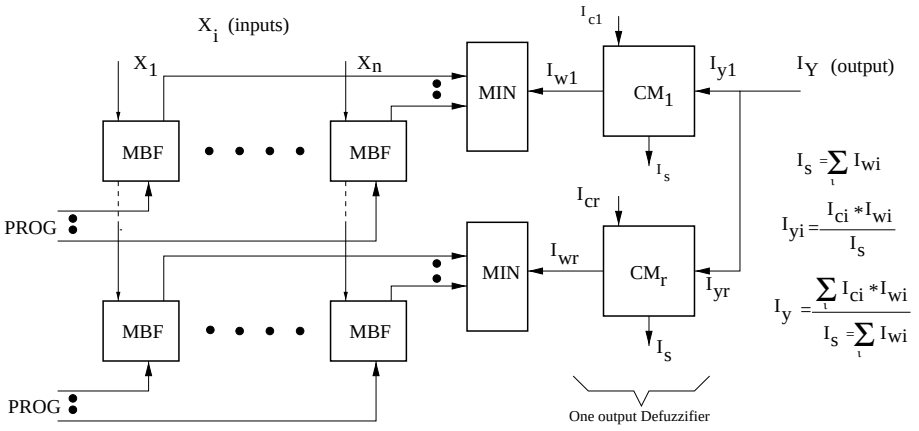

Figure 2: Architecture of the Fuzzy Controller

with a Triangular / Trapezoidal shape, as can be seen in figure 3. As the circuit os based in a linear transconductor, it performs the triangular and trapezoidal shapes better than the commonly used OTA based on the differential pair.

2. The Inference Machine (IM). The IM blocks performs the Mamdani–type of inference process (figure 4) using the *AND* operators, which are implemented with a *MIN* circuit. Figure

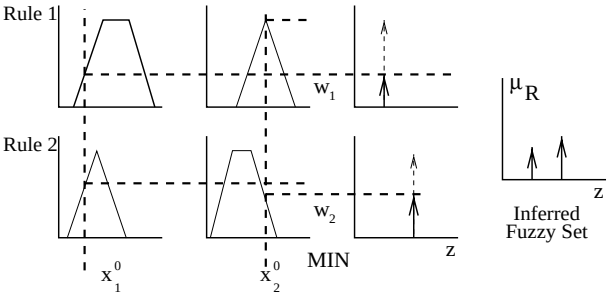

Figure 4: Mamdani–type inference process, using singleton as membership functions for the output variable

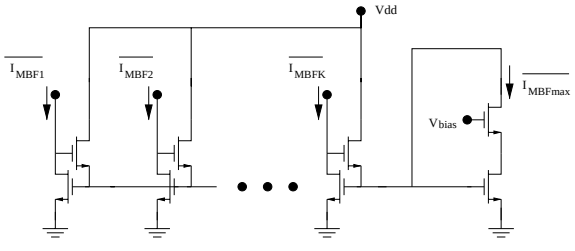

Figure 5: Max Circuitry

5 shows the *MAX* circuit, which is based on the Winner–Take–All circuit proposed in [11] and later improved in ([12]); the only modification included here is a cascode output to improve the response of the output current mirrors. This circuit also builts the *MIN* operator, using the De Morgan's Law and the complement operator [13]. (Figure 6)

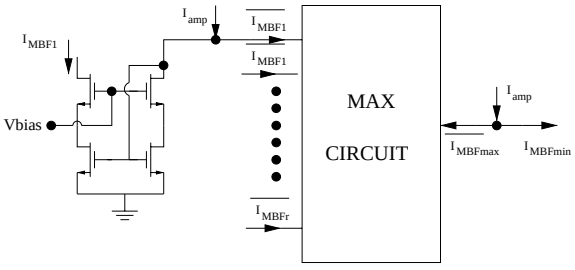

Figure 6: Min Circuitry

3. The Defuzzifier Block (DF). The defuzzifier block implementes the center of the gravity method with singletons as the rule consequents. Equation (1) resumes the computations to be performed.

$$output = \frac{\sum_{i=1}^{i=r} w_i c_i}{\sum_{i=1}^{i=r} w_i} \qquad (1)$$

where r is the number of rules, w_i is the inferred output for rule i, and c_i is the singleton for the consequent of rule i. These computations can be performed better in current-mode (in a circuit node the output current is the sum of the input currents), using the current multiplier / divider proposed in [14] and depicted in figure 7. It makes the Defuzzifier Block faster and simple.

IV. Results and Future Research

HSPICE simulations using a standard 0.7 μm CMOS technology were performed. In figure 10, 9 and 8 can be seen the tunability of the positions ,

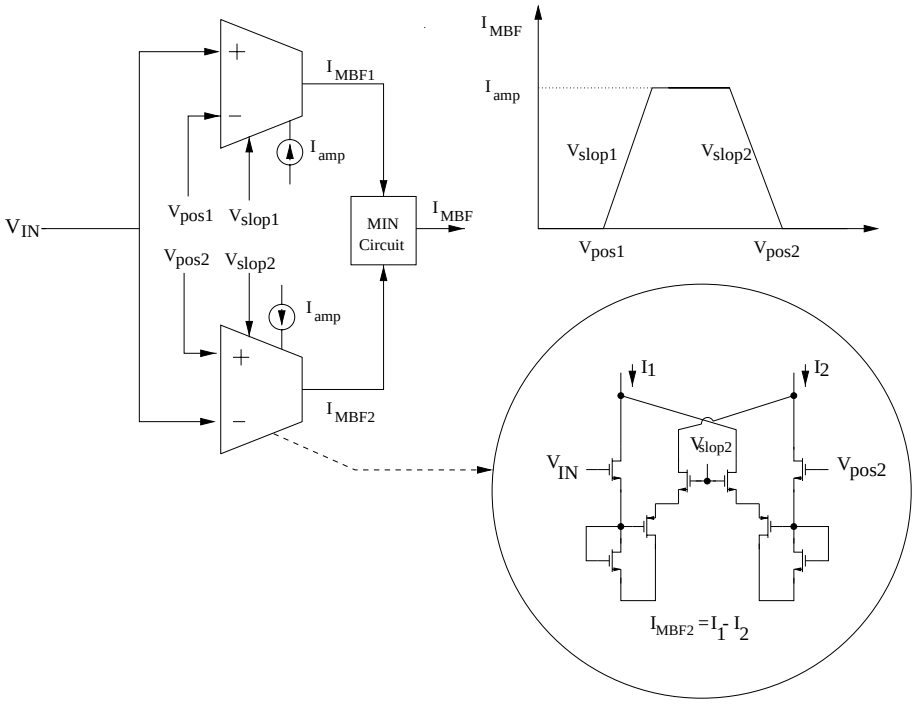

Figure 3: Membership Function Generator

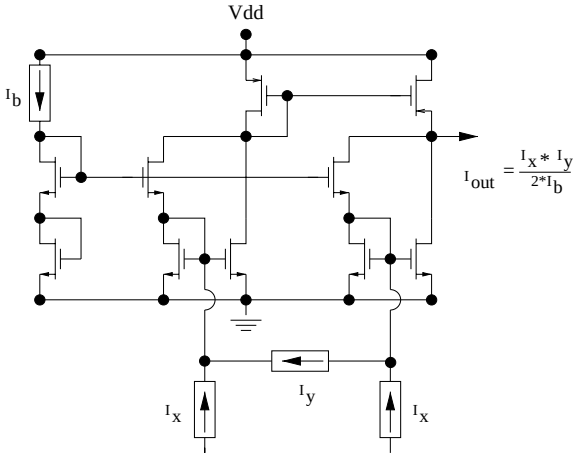

Figure 7: Current mode Multiplier / Divider

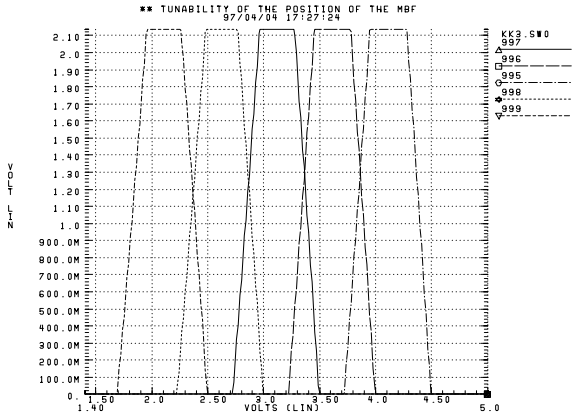

Figure 8: Tunability of the position of the MBF

slope and shapes of the membership functions. In figure 11 can be seen the transient transient of the *MIN* circuit. Finally in figure 13 is showed the DC performance of the current multiplier and in figure **??** is showed the transient response of this multiplier. Presently a library of cells is being designed using Cadenca Software.

V. Acknowledgments

The authors would like to acknowledge financial support by CICYT through the TIC86-0860 project.

References

[1] J. Ramirez–Angulo, K. Treece, P. Andrews and T. Choi. “Current–Mode and Volage–Mode VLSI fuzzy processor architecture”. *Proc. Int. Conf. on Circuits and Systems, ISCAS’95*, pp 1156–1159, Seattle 1995.

[2] Special issue on “Engineering Applications of Fuzzy Logic”. *Proc. of the IEEE*, March 1995.

[3] A.Costa, A.de Gloria, P.Faraboshi, and A.Pagni. “A tool for automatic synthesis of fuzzy controllers”, in *Proc. of the IEEE Int. Conf. on Fuzzy Systems*, Orlando 1994, pp. 1771–1775.

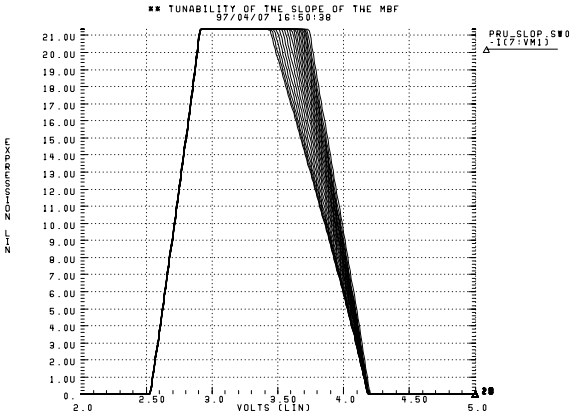

Figure 9: Tunability of the slope of the MBF

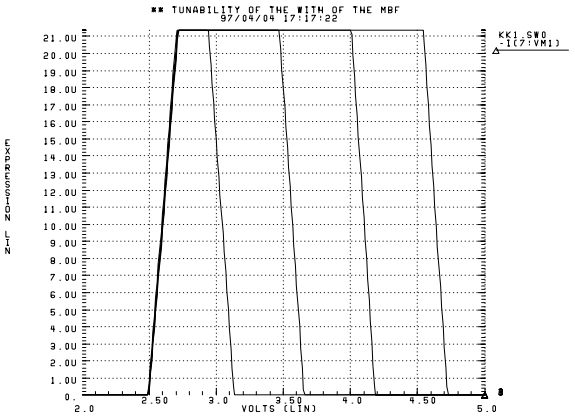

Figure 10: Tunability of the with of the MBF

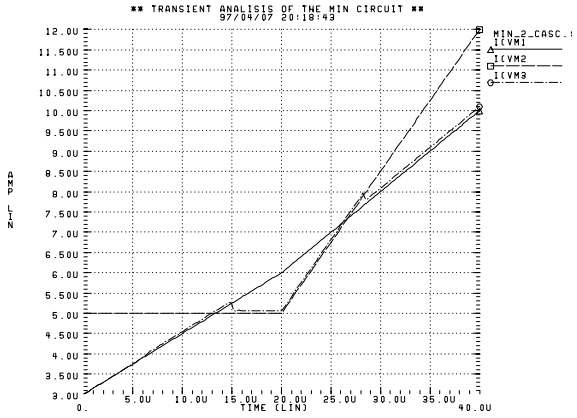

Figure 11: Transient analisis of the MIN circuit

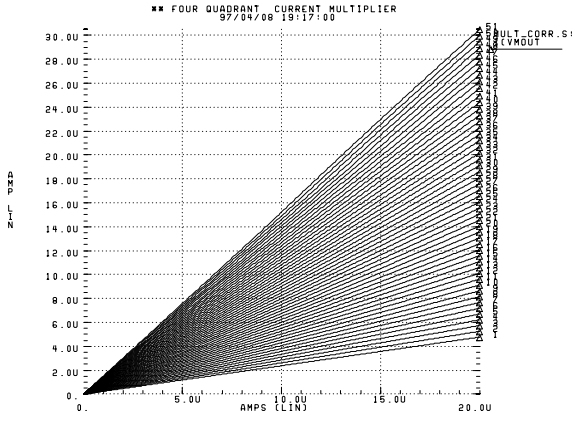

Figure 12: DC performance of the multiplier circuit

[4] T. Hollstein, S. K. Halgamuge and M. Glesner. "Computer-Aided Design of Fuzzy Systems Based on Generic VHDL Specifications".*IEEE Trans. on Fuzzy Systems*, vol. 4 no. 4 pp. 403–417, November of 1996.

[5] R. G. Carvajal, A. Torralba and L. G. Franquelo. "AFAN, A Tool for the Automatic Synthesis of Neural and Fuzzy Controllers with Architecture Optimization", *1997 IEEE International Symposium on Circuits and Systems, ISCAS'97*. June 9-12, Hong-Kong

[6] N. Manaresi, R. Rovatti, E. Franchi, R. Guerrieri and G. Baccarani. "A Silicon Compliler of Analog Fuzzy Controllers: From Behavioral Specifications to Layout".*IEEE Trans. on Fuzzy Systems*, vol. 4 no. 4 pp. 418–428, November of 1996.

[7] C.C.Lee. "Fuzzy logic in control systems: Fuzzy logic controller, Part I". *IEEE Trans. Syst., Man, and Cybern.*, vol. 20, no. 2, pp. 404–418, 1990.

[8] C.C.Lee. "Fuzzy logic in control systems: Fuzzy logic controller, Part II". *IEEE Trans. Syst., Man, and Cybern.*, vol. 20, no. 2, pp. 419–435, 1990.

[9] R. G. Carvajal, A. Torralba, F. Colodro and L. G. Franquelo. "An Analog CMOS Universal Membership Function Generator with Fully Independent Adjustable Parameters". submitted for publication

[10] S. C. Huang and M. Ismail, "Linear tunable COMFET transconductors", *Electronics Letters*, vol 29, pp. 459-461, March 1993.

[11] J. Lazzaro, S. Ryckebusch, M. A. Mahowald and C. A. Mead. "Winner–Take–All Networks of O(n) Complexity". *Advances in Neural Information Processing Systems*, vol. 1, D.S. Toureztky, ed. Morgan Hauffmann, 1989.

[12] Bin-Da Liu and Chun-Yueh Huang. "Array Based Fuzzy Inference Mechanism Implemented with Current–Mode CMOS Circuits".*Proc. Int. Conf. on Circuits and Systems, ISCAS'94* vol. 5, London, June 1994.

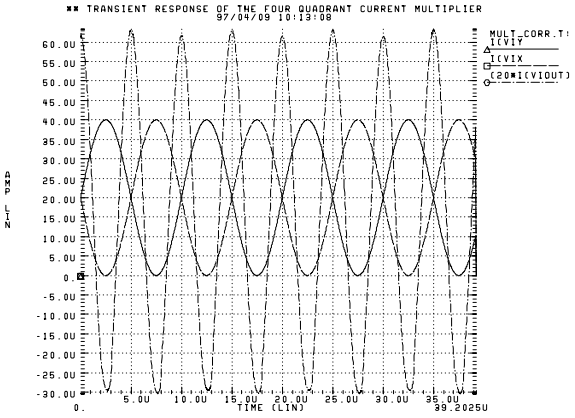

Figure 13: Transient response of the multiplier circuit

[13] M. Sasaki, T. Inoue, Y. Shirai and F. Ueno. “Fuzzy Multiple–Input Maximum and Minimum Circuits in Current Mode and Their Analyses Using Bounded-Difference Equations”. *IEEE Transactions on Computers*, vol. 39, no. 6, June 1990.

[14] K. Bult and H. Wallinga. “A Class of Analog CMOS Circuits Based on the Square–Law Characteristic of an MOS Transistor in Saturation”.*IEEE Journal of Solid–State Circuits*, vol. SC-22, no. 3, pp. 357–365, June 1987.