A Tunable Floating-Gate CMOS Transconductor Based on Current Multiplication

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Abstract - In this paper a novel transconductor based on floating gate techniques that performs current multiplication for tuning is presented. The multiplication is achieved using transistors operating in weak and moderate inversion together with floating voltage sources implemented conveniently by floating capacitors. Besides, a tuning scheme is proposed to set the transconductance parameter accurately. The resulting circuit features compactness, low voltage operation, and rail-to-rail input range. Measurement and simulation results using a 0.5um CMOS technology are presented to confirm all the circuits and strategies proposed.

Index Terms—OTA, Floating gates, CCII-R, Low voltage

I. INTRODUCTION

Operational Transconductance Amplifiers (OTAs) are versatile analog building blocks featuring high bandwidth and tunability that can find application in many fields. However, the linearity and input voltage are relatively poor. Some attempts have been proposed in order to improve the linearity of OTAs, such as adaptive biasing or nonlinearity cancellation, but they often require generating extra currents increasing the area and power consumption, and/or rely on the MOS square law which is unrealistic in modern processes [1]. Another alternative is to use Current Conveyors (CCII) [2] and a passive resistor for forming the OTA obtaining very low distortion, but continuous tuning of the resistor is not possible and the input range can also be limited. To overcome these drawbacks in this paper floating-gate techniques together with CCIs and passive resistors are introduced for providing tunability, low voltage operation, and rail-to-rail input range. Tunability is achieved using a current multiplication cell based on a floating-gate current mirror operating in weak or moderate inversion.

The paper is organized as follows. Section II provides a quick review of floating gate transistors and a solution based on a layout technique for avoiding the initial trapped charge. Section III presents the general block diagram of our proposal and a compact implementation at transistor level allowing a rail-to-rail input and tunability of the OTA. A transconductance tuning scheme is mentioned in Section IV. Measurement and simulation results from a fabricated prototype using a 0.5um CMOS technology are presented in Section V validating all the techniques and ideas proposed in this paper. Finally some conclusions are drawn in Section VI.

Fig. 1. Equivalent circuit of a \( n \)-input floating gate transistor.

II. A BRIEF INTRODUCTION TO THE FLOATING-GATE TRANSISTORS

The equivalent circuit of a floating-gate transistor (FGT) [3] is shown in Fig. 1. The gate voltage is set though the input terminals that are capacitively coupled to the floating gate. Assuming that input capacitors are much larger than the parasitic capacitances of the transistor, the gate voltage can be expressed as

\[
V_{FG} = a_1 \cdot V_1 + a_2 \cdot V_2 + ... + a_n \cdot V_n
\]

where

\[
a_k = \frac{C_k}{\sum_{i=1}^{n} C_i}
\]

Hence a weighted averaging of the input voltages is achieved in a compact way. Here, it has been supposed that trapped charge at the gate is zero, which can be enforced during manufacturing process (hence not requiring post-fabrication removal of such charge) using the technique reported in [4].

III. TUNABLE TRANSCONDUCTOR BASED ON FGMOS CURRENT MIRRORS

The tunable transconductor presented is shown in Fig. 2. Both input and output are differential, and the circuit is composed of two current conveyors. The CCIs have been
built using voltage followers and current mirrors that can scale the buffer output current by a factor $K$. Input signal is scaled by the factor “$a$” using techniques based on floating-gate transistors (FGT) in order to allow rail-to-rail input range. The element which performs the V-I conversion is a passive transistors (FGT) in order to allow rail-to-rail input range. The buffer output current by a factor $K$ using techniques based on floating-gate transistors (FGMOS) in order to allow rail-to-rail input range. The current mirror are operating in weak or moderate inversion [7]. Thus high aspect ratios were selected for these FGTs to make them operate in weak or moderate inversion, in order to achieve a dependence as linear as possible between control voltages and current gain and to minimize distortion [7]. A more detailed analysis of the inversion level of transistors $M_{IP}$ ($M_{2P}$) and $M_{IP}$ ($M_{2P}$) is done in Section V.

**B. Input Range Increase.**

Note from Fig. 2(b) that, using conventional current mirrors, drain voltage of transistor $M_{1N}$ would be $V_{DD}-V_{FGND}$, so the upper limit of the range over which $V_{in}^+$ can swing keeping $M_{1N}$ in saturation would be very limited when low supply voltages are used. The same problem would occur with $M_{2N}$ and $V_{in}^-$. However, if FGMOS mirrors are used, drain voltages of $M_{1N}$ and $M_{2N}$ can be adjusted by varying the common mode voltage of $V_{F1}$ and $V_{F2}$. Specifically, when $V_{F1}=V_{F2}=V_{FCM}$ these two voltages can be expressed as

$$V_{B1N} = \frac{1}{1-b} V_{G3P} + \frac{b}{1-b} V_{FCM}$$

and

$$V_{B2N} = \frac{1}{1-b} V_{G4P} + \frac{b}{1-b} V_{FCM}$$

where $b$ is a constant ($0 < b < 1$) determined by the ratio between the capacitors of the floating-gates. Therefore, the signals at the drains of $M_{1N}$ and $M_{2N}$ are $V_{G3P}$ and $V_{G4P}$ respectively, expanded by $1/(1-b)$ and dc shifted by $b/(1-b)V_{FCM}$, so that $V_{FCM}$ must be set properly in order to increase the input range without affecting the operation of the upper current sources. In turn, transistors $M_{1N}$ and $M_{2N}$ have been replaced by a couple of two-input FGMOS transistors. One of the inputs is set to $V_{DD}$, and input signal ($V_{in}^+$ and $V_{in}^-$ in each case) is applied to the other terminal. A detailed view of $M_{1N}$ is shown in Fig. 3(a). The gate voltage $V_{GIN}$ is given by

$$V_{GIN} = \frac{C_1}{C_1+C_2} V_{DD} + \frac{C_2}{C_1+C_2} V_{in}^-$$

so it is an attenuated and up-shifted version of $V_{in}^+$, allowing rail-to-rail input signals as shown in Fig. 3 [3]. Note from (7) that when $V_{in}^+=V_{DD}$ then $V_{GIN}=V_{DD}$. However, when $V_{in}^+=V_{SS}$, the value of $V_{GIN}$ depends on the relation between the capacitors $C_1$ and $C_2$. In order to get rail-to-rail operation, $C_1$ and $C_2$ have to be chosen properly, so that when $V_{in}^+=V_{SS}$, $V_{GIN}$ (and therefore $V_{GIN}$) is high enough to allow bottom current sources to work correctly. This idea is represented in Fig. 3(b). Note that factor $a$ that appears in (3) and (4) is given

![Fig. 2. Tunable transconductor based on FGMOS current mirrors. (a) Diagram (b) Schematic.](image-url)
by \( a = C_f(C_T + C_f) \). In the other half of the circuit the situation is similar.

### IV. Transconductance Tuning

One of main drawbacks of the programmable current mirrors is the fact that the value of \( V_{T1} \) and \( V_{T2} \) should be set precisely in order to guarantee that transistors are operating in weak or moderate inversion. Thus it could be desirable to set the transconductance parameter externally using known currents and/or voltages. Also this approach allows compensation for fabrication tolerances of resistors.

Tuning has been achieved using a replica circuit. In our case only one half of the circuit has been replicated because it is completely symmetrical. For this reason the replica circuit, which is shown in Fig. 4, has been named \( Gm1/2 \). The voltage \( V'_{CM} \) is sensed from the central point of \( R \) in the transconductor of Fig. 2(b) (between two \( R/2 \) resistors placed in series). This voltage \( V'_{CM} \) is copied to the negative input of the amplifier, so half of the transconductor is simulated. A simple one-stage differential amplifier has been used, because a more complex topology is not required to operate as voltage follower. \( C_C \) is a compensation capacitor. The output current of \( Gm1/2 \) circuit is given by

\[
i_{OUT} = K I_B + \frac{K a}{R/2} \left( V_{IN} - V_{CM0} \right)
\]

where \( V_{CM0} \) is the common mode input voltage. Hence, if transconductors of Fig. 2(b) and the control block share \( V_{F1} \) and \( V_{F2} \), the transconductance \( Gm \) will be controlled by \( V_{BIAS} \) and \( I_{TUN} \). The whole system is shown in Fig. 5. \( V_{F1} \) has been set externally, so the only adaptive parameter is \( V_{F2} \), which has been connected to the output terminal of the control block. Under these conditions, the current gain \( K \) of the programmable current mirrors will be given by

\[
K = \frac{I_{TUN}}{I_B + \frac{a R}{2} (V_{BIAS} - V_{CM0})}
\]

### V. Measurement and Simulation Results

The transconductor of Fig. 2(b) was fabricated in a 0.5\( \mu \)m CMOS technology, with nominal nMOS and pMOS threshold voltages of 0.78V and -0.94V, respectively. A microphotograph is shown in Fig. 6. The resistance \( R \) of 40\( K\Omega \) was made of nonsilicided polysilicon. A supply voltage of ±1.65V and a bias current \( I_B \) of 50\( \mu \)A were applied. The current sources were implemented with cascode sources. Cascode transistors are biased with dc voltages \( V_p = 0.1V \) (for nMOS) and \( V_p = 0.2V \) (for pMOS). \( V_p \) is the same for the cascode transistors of programmable current mirrors, which have been introduced in order to increase the output resistance. Aspect ratios (in \( \mu \)m/\( \mu \)m) of the transistors of the current sources were (30/1.05) in the case of nMOS and (199.95/1.05) for pMOS. The ratio \( W/L \) is twice for the nMOS transistors which have to provide a current of 2\( I_B \). The input transistors \( M_1 \) and \( M_2 \) have \( W = 30 \mu \)m and \( L = 1.05 \mu \)m. Finally, in order to achieve weak or moderate inversion, an aspect ratio of (250.05\( \mu \)m/0.90\( \mu \)m) was chosen for the transistors of the programmable current mirrors \( (M_{1p}, ..., M_{8p}) \). \( V_{F1} \) and \( V_{F2} \) common mode voltage was 0.5V.

The two FGMOS input capacitances of the current mirrors were identical (1 pF). In the differential input pair, a capacitance of 1 pF was associated to input signal \( (V_{in} + V_{in'}) \) and \( V_{DD} \) input is applied to a capacitance of 1.5 pF. Hence, the attenuation factor \( a \) is 0.4, so the maximum current across \( R \) will be 0.4(3.3/40.10\(^3\))=33\( \mu \)A. Therefore, the input currents of the mirrors swings between 17\( \mu \)A \( (I_B - I_{Rmax}) \) and 83\( \mu \)A \( (I_B + I_{Rmax}) \). The characteristic current for the pMOS
transistors of the programmable mirrors is \( I_S = 2K_V/|W/L|nU_T = 15.5 \mu A \). The inversion factor \( I/I_S \) is employed to define the MOS inversion level. Weak inversion corresponds to \( I/I_S << 1 \), strong inversion to \( I/I_S >> 1 \) and moderate inversion to intermediate values (typically \( 1 < I/I_S < 10 \)). In our case \( 17 \mu A < I_S < 83 \mu A \). Thus, the inversion factor ranges in \( 1 < I/I_S < 5.3 \), so the transistors operate in moderate inversion. Fig. 7 shows the \( I/I_S-\)dc response for five different \( V_{F1}-V_{F2} \) values, and harmonic distortion measured at 100KHz is shown in Fig.8. Second-order distortion is quite high due to the experimental setup (made by off-chip Op-Amps and resistors), as \( HD3 \) should be dominant in a fully differential circuit like this, and in fact it is dominant in simulation. Fig. 9 shows harmonic distortion for several values of \( V_{F1}-V_{F2} \). Note that distortion has a minimum when current mirrors have unity gain \( (V_{F1}-V_{F2}=0) \) and increase with \( |V_{F1}-V_{F2}| \), although this increment stops around \( |V_{F1}-V_{F2}|=100 \text{mV} \).

Finally, the system of Fig. 5 has been simulated for \( K \) values from 0.5 to 2. Aspect ratio for \( M_N \) is \( (120 \mu m/1.05 \mu m) \), and \( C_c = 3 \text{pF} \). Results are shown in Table I. Note that the achieved \( K \) is similar to its theoretical value (error \( <8\% \) in the worst result of the table), and harmonic distortion increases as we move away from \( K=1 \). However, the minimum distortion is situated at a value of \( K \) slightly less than 1. Also, note that linearity deteriorates faster for \( K>1 \) (amplification) than for \( K<1 \) (attenuation). In general, amplification affects linearity more than attenuation, as the output transistors are closer to strong inversion in this case.

## VI. Conclusion

In this paper a novel tunable transconductor has been proposed. The structure is based on CClIs and programmable current mirrors using floating gate transistors operating in weak or moderate inversion. In order to set the transconductance accurately a replica bias dc tuning has been proposed. Measurement results from a fabricated CMOS prototype have been shown for demonstrating the viability of the cells and techniques proposed in the paper.

## REFERENCES