Voltage balancing in three-level neutral-point-clamped converters via Luenberger observer

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Abstract

This paper addresses the problems associated with the dc-link capacitor voltages of the three-level neutral-point-clamped power converter: the imbalance of the capacitor voltages as well as the presence of an ac-voltage low-frequency oscillation in the dc link of the converter. In order to cope with them, a mathematical analysis of the capacitor voltage difference dynamics, based on a direct average continuous model, is carried out, considering a singular perturbation approach. The analysis leads to a final expression where a sinusoidal disturbance appears explicitly. Consequently, the two problems can be handled together using the ordinary formulation of a problem of regulating the output of a system subject to sinusoidal disturbances, applying classical control theory to design the controller. In this way, the controller is designed including the disturbance estimate provided by a Luenberger observer to asymptotically cancel the disturbance, while keeping also balanced the capacitor voltages. Experiments for a synchronous three-level neutral-point-clamped converter prototype are carried out to evaluate the performance and usefulness of the converter working as a grid-connected inverter under the proposed control law.

Keywords: Multilevel power converter, neutral-point-clamped (NPC) converter, voltage balancing, disturbance rejection, Luenberger observer

1. Introduction

In the field of power conversion, more specifically in the three-level neutral-point-clamped (NPC) converter [1], there exists a phenomenon concerning the presence of sinusoidal disturbances: a low-frequency voltage ripple is present in the neutral point of the dc link [2, 3]. Concretely, the voltage difference of the dc-link capacitors fluctuates at three times the fundamental frequency of the ac-side voltage. Note that, in this topology, probably the most extensively applied at present multilevel topology [4, 5], the dc link consists of two capacitors. Thus, if the converter is connected to the grid, the ac-voltage fluctuation has a frequency of 150 Hz, that is, 3×50 Hz.

This phenomenon affects the balance of the capacitor voltages, and although, based on results reported by other researches, it does not limit the usefulness of the converter for practical applications, it represents a significant drawback since the capacitors must be designed to stand the oscillation. In this way, several strategies have been proposed [6, 7] to cope with the problem, including the use of novel modulation techniques [8], or improving the performance of others previously considered [9], to name a few. Important research is still being made in this field considering various approaches [10, 11].

In addition to the elimination of the neutral-point voltage oscillation, the balancing of the dc-link capacitor voltages, which is the main technical challenge of the NPC topology, should be guaranteed. The voltage imbalance problem, that produces a voltage difference between the capacitors causing undesirable distortion at the converter ac side, has been widely investigated for this topology [12, 13]. Some modulation strategies provide natural voltage balancing. Nevertheless, in any other case, additional control effort is required. Significant results concerning the implementation of distinct voltage balancing techniques have been achieved [14, 15, 16, 17]. Among these techniques, some are based on the exploitation of the redundant switching states of the converter [18]. In other words, they are based on the use of those different positions of the converter switches that lead to the same generated voltage, but they cause different effects on the capacitor voltages.

Therefore, there are two problems associated with the dc-link capacitor voltages of the three-level NPC converter: (i) the voltage imbalance of the dc-link capacitors and (ii) the presence of the ac-voltage low-frequency oscillation in the dc link. This paper addresses both problems, considering a continuous model of the converter [19], which includes the dynamics of the voltage difference between the dc-link capacitors. Focusing on these dynamics, a mathematical analysis of their behavior is carried out, under the assumption of different time scales, that it, adopting a singular perturbation approach[1]. This analysis yields an approximated model where a sinusoidal function of time whose frequency is three times the fundamental frequency of the ac-side voltage appears explicitly. Consequently, the two problems related to the dc-link capacitor voltages can be han-

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[1] The authors also have worked out analysis of the converter dynamics in other multilevel topologies, e.g., in the five-level diode-clamped converter [20] and in the three-level diode-clamped back-to-back converter [21].

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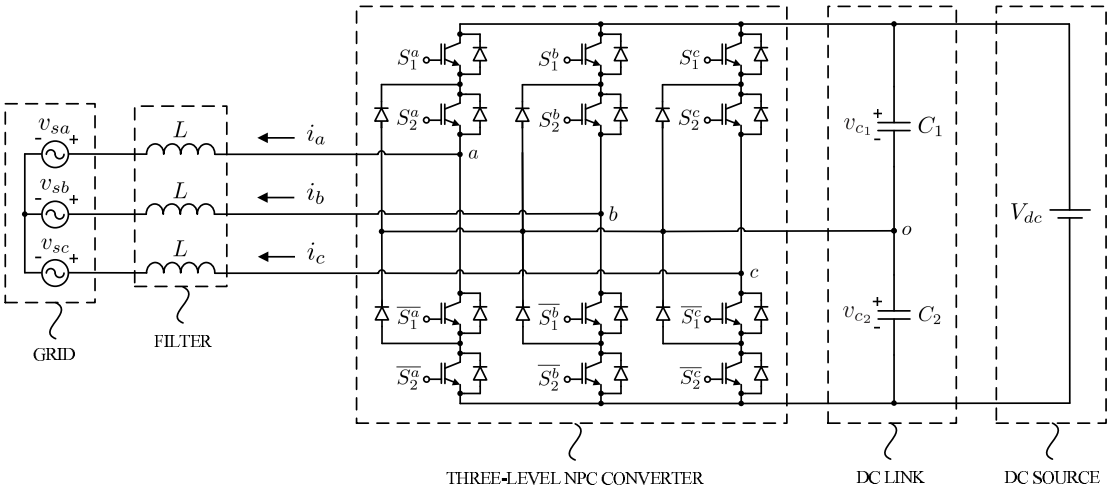


Figure 1: Grid-connected three-phase three-level NPC inverter.

dled together using the conventional formulation of a problem of regulating the output of a system under the presence of sinusoidal disturbances [22, 23], applying also classical control theory to design the controller. In this manner, the analysis provides, compared with the strategies usually considered to deal with these problems, an alternative control approach.

1.1. Rejection of sinusoidal disturbances

The effectiveness of a system can be seriously deteriorated by the presence of sinusoidal disturbances. In the field of power electronics, some well-known examples are the harmonic currents generated by non-linear loads in systems that incorporate rectifiers such as variable speed drives or uninterruptible power supplies [24], and the harmonic current in the neutral conductor of four-wire three-phase dc-ac converters [25]. However, sinusoidal disturbances also appear in many other engineering applications such as active noise and vibration control systems [26], optical and hard disk drives [27], helicopter rotor blades [28], and dc and stepper motors [29], among others.

Even though the problem of identifying and asymptotically rejecting sinusoidal disturbances has been widely studied over the years, it continues attracting special interest [30, 31, 32]. In what follows, some control approaches considered to deal with this problem are mentioned:

1. One of the most popular methods is based on the internal model principle [33]. This property states that, to achieve perfect cancelation, any regulator which solves the problem in question should incorporate in the feedback a reduplicated model of the dynamic structure of the disturbance which must be tracked and/or rejected.

2. Adaptive control techniques are commonly used when the disturbance parameters are unknown, applying the estimate of the disturbance to reject the disturbance at the input of the plant [34, 35, 36].

3. Other approach proposed solves the posed problem by implementing an adaptive observer of the disturbance [37, 38]. This observer is then incorporated in the controller.

In this paper, considering the approximated model derived from the analysis of the converter dynamics, an asymptotic disturbance rejection approach is considered. Thus, the controller proposed implements a Luenberger observer to estimate the disturbance. Then, the disturbance estimate is used to asymptotically cancel the sinusoidal disturbance, including also in parallel another control action for ensuring the regulation of the capacitor voltages as well.

It is important to point out that this paper is an extension of the work presented in [39], showing some remarkable differences and improvements. In that paper, the mathematical analysis is formulated in a NPC rectifier for a particular operating condition. Nevertheless, in the current paper, the analysis is carried out considering the inverter operation mode, leading to a general result valid for any converter operating point. In addition, experimental results for a synchronous three-phase three-level converter prototype are included, corroborating in this manner the mathematical analysis worked out. Conclusions derived from the study of the frequency spectrum of the capacitor voltage difference also are discussed in this paper.

The outline of the paper is as follows. First, the model of the converter is described in Section 2, and the control objectives to achieve are stated in Section 3. Then, Section 4 is devoted to the analysis of the dc-link capacitor voltage difference dynamics. Afterwards, Section 5 presents the proposed controller, which is based on the disturbance estimation carried out by a Luenberger observer. Simulation and experimental results obtained with a laboratory converter prototype are discussed, respectively, in Section 6 and in Section 7. Finally, some conclusions are presented in Section 8.

2. Model of the system

Figure 1 illustrates a schematic diagram of the three-phase three-level NPC converter working as an inverter connected to

the grid, which is the setup considered in this paper. The dc link of the converter is composed of capacitors C_1 and C_2, both of same capacitance C. Their respective voltages are represented by v_{c_1} and v_{c_2}. Besides, the total dc-link voltage is defined by V_{dc}. Phase voltages are denoted by v_{sa}, v_{sb} and v_{sc}, and the phase currents in the inductors L by i_a, i_b and i_c. Notice that no fourth wire is introduced in the circuit.

The voltages generated in points a, b and c, with respect to dc-link neutral point o, are denoted by v_a, v_b and v_c, respectively. These generated voltages depend on the switching states of the converter, which are determined by the set of discrete values of the gating signals δ_a^*, δ_b^* and δ_c^* as follows

$$\delta_i^* = \begin{cases} 1 & \rightarrow & S_1^i \text{ on}, & S_2^i \text{ on} & \rightarrow & v_i = v_{c_1} \\ 0 & \rightarrow & S_1^i \text{ off}, & S_2^i \text{ on} & \rightarrow & v_i = 0 \\ -1 & \rightarrow & S_1^i \text{ off}, & S_2^i \text{ off} & \rightarrow & v_i = -v_{c_2}, \end{cases} \tag{1}$$

for $i = a, b, c$.

Considering this preliminary description, the model of the three-level NPC back-to-back converter presented in [19] is adapted to the three-level NPC inverter application of the present paper. This model is based on a direct average of the characteristics and waveforms associated with each of the components of the converter. Besides, the control inputs of the model are defined by δ_a, δ_b and δ_c, and they represent the averaged values of the gating signals (1) in a switching period. Because these control inputs are implemented through a modulator to obtain the gating signals, they should be located within the domain

$$D_{\delta_{abc}} \in \mathbb{R}^3 := D_{\delta_a} \times D_{\delta_b} \times D_{\delta_c}, \tag{2}$$

where $D_{\delta_i} = [-1, 1]$ for $i = a, b, c$, to generate correctly the switching sequence.

As a result, the inverter model, expressed in stationary $\alpha\beta\gamma$ orthogonal coordinates by means of the power-invariant form of the Clarke Transform, describes the dynamics of the phase currents and of the voltage difference between the dc-link capacitors. It is defined by

$$L\frac{di_\alpha}{dt} = -v_\alpha + \delta_\alpha\frac{V_{dc}}{2} + \left(\frac{\delta_\alpha\delta_\gamma}{\sqrt{3}} + \frac{\delta_\alpha^2 - \delta_\beta^2}{2\sqrt{6}}\right)v_d \tag{3}$$

$$L\frac{di_\beta}{dt} = -v_\beta + \delta_\beta\frac{V_{dc}}{2} + \left(\frac{\delta_\beta\delta_\gamma}{\sqrt{3}} - \frac{\delta_\alpha\delta_\beta}{\sqrt{6}}\right)v_d \tag{4}$$

$$\begin{aligned} C\frac{dv_d}{dt} = &-\frac{2}{\sqrt{3}}\left(\delta_\alpha i_\alpha + \delta_\beta i_\beta\right)\delta_\gamma \\ &-\frac{1}{\sqrt{6}}\left(\left(\delta_\alpha^2 - \delta_\beta^2\right)i_\alpha - 2\delta_\alpha\delta_\beta i_\beta\right), \end{aligned} \tag{5}$$

where v_d is the dc-link capacitor voltage difference

$$v_d = v_{c_1} - v_{c_2}. \tag{6}$$

Notice that the phase currents and the phase voltages are transformed from abc into $\alpha\beta\gamma$ coordinates, yielding the current variables i_α and i_β, and the voltage variables v_α and v_β, respectively. Moreover, the control inputs also are transformed into δ_α, δ_β and δ_γ. Table 1 summarizes the variables of the system.

Table 1: Variables of the system model.

Variable	Description
i_α, i_β	Phase currents
v_α, v_β	Phase voltages
δ_α, δ_β, δ_γ	Control inputs
v_d	Dc-link capacitor voltage difference

3. Control objectives

As pointed out before, this paper addresses the problems associated with the dc-link capacitor voltages of the three-level NPC converter. With the aim of overcoming them, two specific control objectives are stated:

1. The dc-link capacitor voltage difference v_d should be kept close to zero, remaining within a domain containing zero.
2. The low-frequency voltage ripple present in the dc-link neutral point should be reduced to an acceptable level.

Concerning the first control objective, it entails the practical stability [40] of the system. This concept, also referred to as ultimate boundedness [41], deals with the boundedness properties of the state of a dynamic system. This requirement is due to factors such as component imperfections, transients, or other imbalances in the converter [12]. Moreover, it is also related to the fact that the positions of the power switches of the converter are restricted to belong to a finite set [42].

With regard to the second control aim, it is defined to ensure a good performance of the converter. Note that if the sinusoidal disturbance is neglected and no control method is devoted to mitigate its effect, there is an increase in the power losses of the system, and the operating life of the capacitors is decreased.

It is worth stressing that there also exists another control objectives which can be defined in relation to the instantaneous powers of the three-phase circuit:

3. The instantaneous active and reactive powers, denoted by p and q, respectively, and defined as

$$p = v_{sa}i_a + v_{sb}i_b + v_{sc}i_c = v_\alpha i_\alpha + v_\beta i_\beta \tag{7}$$

$$\begin{aligned} q &= \frac{1}{\sqrt{3}}\left(\left(v_{sa} - v_{sb}\right)i_c + \left(v_{sb} - v_{sc}\right)i_a + \left(v_{sc} - v_{sa}\right)i_b\right) \\ &= v_\alpha i_\beta - v_\beta i_\alpha, \end{aligned} \tag{8}$$

should be driven to their respective references p^* and q^*.

Remark 1. *Although the rest of the paper is focused on the first two control objectives, it is necessary to design some other control loop, because the third control objective should be also fulfilled. In the following, it is assumed that there exist certain appropriate controller that deals with the regulation of the variables p and q. Specifically, the control inputs δ_α and δ_β are used to this end. In this manner, the control input δ_γ remains as a degree of freedom for coping with the voltage imbalance problem and with the reduction of the low-frequency ripple.*

4. Analysis of the converter dynamics

This section is devoted to analyze the dc-link capacitor voltage difference dynamics (5), with the purpose of studying the phenomenon of the voltage ripple that is present in the neutral point of the dc link. In order to work out this mathematical analysis, an essential assumption related to a singular perturbation approach is first posed [43].

Assumption 1. *The instantaneous power dynamics are much faster than the dc-link capacitor voltage difference dynamics.*

Concerning this assumption, it leads to suppose in order to study the behavior of (5) that the instantaneous powers have been correctly regulated around their respective references[2]

$$p \simeq p^* \tag{9}$$
$$q \simeq q^*. \tag{10}$$

To that end, an appropriate controller that uses the inputs δ_α and δ_β to control the instantaneous powers is assumed to be implemented in the system.

Besides, since the previous assumption is related to the instantaneous powers, but the voltage difference dynamics (5) contain the current terms i_α and i_β, the analysis begins expressing these dynamics in terms of power instead of current. Thereby, according to (9) and (10), the phase currents are approximated, considering (7) as well as (8), by

$$i_\alpha \simeq \frac{1}{|\boldsymbol{v}_{\alpha\beta}|^2}\left(v_\alpha p^* - v_\beta q^*\right) \tag{11}$$

$$i_\beta \simeq \frac{1}{|\boldsymbol{v}_{\alpha\beta}|^2}\left(v_\beta p^* + v_\alpha q^*\right), \tag{12}$$

defining in this manner a change of variables. It is important to mention that the phase voltages in $\alpha\beta$ coordinates can be expressed as

$$v_\alpha = |\boldsymbol{v}_{\alpha\beta}|\cos\left(2\pi f t + \theta\right) \tag{13}$$

$$v_\beta = |\boldsymbol{v}_{\alpha\beta}|\sin\left(2\pi f t + \theta\right), \tag{14}$$

where f and $|\boldsymbol{v}_{\alpha\beta}|$ are, respectively, the frequency and amplitude of these variables. Parameter θ is the phase.

In the same way, concerning inputs δ_α and δ_β, their expressions are obtained introducing (11) and (12) in the phase current dynamics, that is, in (3) and (4), and assuming that the capacitor voltage imbalance is small, i.e., $v_d \simeq 0$. Note that (5) also depends on these control inputs, which regulate the instantaneous powers of the system. Consequently, control inputs δ_α and δ_β can be described by

$$\delta_\alpha \simeq \lambda_1 v_\alpha - \lambda_2 v_\beta \tag{15}$$

$$\delta_\beta \simeq \lambda_1 v_\beta + \lambda_2 v_\alpha, \tag{16}$$

[2] In [39], a mathematical analysis of converter model is formulated for the particular case when q^* is set to zero to guarantee a power factor close to the unity. Nevertheless, the analysis carried out in the present paper is completely general, that is, it is valid for any converter operating point.

where λ_1 and λ_2 are the constant parameters defined by

$$\lambda_1 = \frac{2}{V_{dc}}\left(1 - \frac{2\pi f L q^*}{|\boldsymbol{v}_{\alpha\beta}|^2}\right) \tag{17}$$

$$\lambda_2 = \frac{4\pi f L p^*}{V_{dc}|\boldsymbol{v}_{\alpha\beta}|^2}. \tag{18}$$

Both parameters λ_1 and λ_2 are included in the expressions (15) and (16) for simplifying the notation used.

Finally, moving on to the dynamics under analysis, introducing (11)-(16) in (5), and considering some trigonometric identities and the constants μ_1 and μ_2 defined by

$$\mu_1 = \frac{|\boldsymbol{v}_{\alpha\beta}|}{\sqrt{6}}\left(\lambda_1^2 + \lambda_2^2\right)\sqrt{p^{*2} + q^{*2}} \tag{19}$$

$$\mu_2 = \frac{-\left(\lambda_1^2 - \lambda_2^2\right)p^* + 2\,\lambda_1\lambda_2\,q^*}{\left(\lambda_1^2 - \lambda_2^2\right)q^* + 2\,\lambda_1\lambda_2\,p^*}, \tag{20}$$

the reduced expression defined as follows

$$C\,\frac{dv_d}{dt} = -\frac{4\,p^*}{\sqrt{3}\,V_{dc}}\,\delta_\gamma + \mu_1\sin\left(3\cdot 2\pi f t + 3\theta + \arctan\left(\mu_2\right)\right), \tag{21}$$

is derived. This result is the final expression of the analysis carried out, and it represents an approximated model of (5). In addition, notice that (21) corresponds to the dynamics that describe the internal behavior of the system when control inputs δ_α and δ_β are chosen to guarantee (9) and (10). Consequently, the approximated model is related to the zero dynamics of the system [44].

4.1. Conclusions and problem statement

The final expression (21) obtained is a general result valid for any operating point of the system, i.e., for any desired value of the instantaneous power references. Furthermore, it shows that, under the assumption of a singular perturbation approach, the highly nonlinear dynamics of the dc-link capacitor voltage difference defined by (5) can be noticeably simplified. The analysis yields a linear differential equation that depends on control input δ_γ and that also contains a sinusoidal function of time whose frequency is three times the frequency of the grid.

This sinusoidal function represents, in the approximated model derived from the analysis, the low-frequency voltage ripple that is present in the neutral point of the dc link and that affects the balance of the dc-link capacitor voltages. Therefore, since this sinusoidal disturbance appears explicitly in (21), it leads to rewrite this final expression as

$$C\,\frac{dv_d}{dt} = -k_d\,\delta_\gamma + \phi(t)\ . \tag{22}$$

Parameter k_d is the following constant

$$k_d = \frac{4\,p^*}{\sqrt{3}\,V_{dc}}, \tag{23}$$

and $\phi(t)$ is the sinusoidal disturbance defined as

$$\phi(t) = \mu_1\sin\left(3\cdot 2\pi f t + 3\theta + \arctan\left(\mu_2\right)\right). \tag{24}$$

Notice that (22) takes the form of the formulation of a problem of regulating the output of a system in presence of disturbances [22, 23], for the linear case. In this way, to achieve the control objectives in order to satisfactory cope with the problems associated with the dc-link capacitor voltages, control theory can be applied to design the controller. This result, which is a key point of the paper, provides a new approach to cope with the problems addressed in this work.

Remark 2. *An important observation is that the classical concept of output regulation means that, for all possible initial conditions of the closed-loop state variables, the error between the system output and the tracking reference should tend to zero as time tends to infinity. However, in this paper, it is not aimed for* $v_d(t) \to 0$ *as* $t \to \infty$*. The requirements are related to the practical stability of the difference between the capacitor voltages. Consequently, the control goals are related to a problem of practical output regulation [45].*

5. Design of the controller

The design of the controller to meet the control requirements is based on the approximated model derived from the analysis of the converter dynamics. Considering (22), the control algorithm proposed adopts a disturbance rejection approach. In this way, the sinusoidal disturbance of the approximated model is estimated by a state space observer, and this estimate is then applied to asymptotically reject the disturbance. Besides, a proportional-integral (PI) controller is implemented in parallel to ensure the regulation of the capacitor voltages.

5.1. Estimation of the sinusoidal disturbance

In order to estimate $\phi(t)$, i.e., the sinusoidal disturbance present in (22), the first step is to express that equation as the augmented linear system $\mathcal{S}$ described by

$$\mathcal{S}: \begin{cases} \dot{x}_d &= \frac{1}{C}\, x_{\phi_1} - \frac{k_d}{C}\, u \\ \dot{x}_{\phi_1} &= x_{\phi_2} \\ \dot{x}_{\phi_2} &= -(3\cdot 2\pi f)^2\, x_{\phi_1}. \end{cases} \tag{25}$$

The capacitor voltage difference v_d is represented by x_d, while variables x_{ϕ_1} and x_{ϕ_2} are the sinusoidal disturbance $\phi(t)$ and its derivative over time, respectively. The system input u represents the control input δ_γ. In this manner, system $\mathcal{S}$ describes the dynamics of (22), exploiting the knowledge and properties of the disturbance, particularly, the fact that its frequency, which is three times the frequency of the grid, is known.

Considering that the output of the system is the variable x_d, the state space representation of system $\mathcal{S}$ is

$$\mathcal{S}: \begin{cases} \dot{\boldsymbol{x}} &= \boldsymbol{A}\boldsymbol{x} + \boldsymbol{B}u \\ y &= \boldsymbol{C}\boldsymbol{x}, \end{cases} \tag{26}$$

where $\boldsymbol{x} \in \mathbb{R}^3$ is the system state vector defined by

$$\boldsymbol{x} = \begin{bmatrix} x_d & x_{\phi_1} & x_{\phi_2} \end{bmatrix}^T, \tag{27}$$

$y \in \mathbb{R}$ is the output, and $u \in \mathbb{R}$ is the control input. The matrices $\boldsymbol{A} \in \mathbb{R}^{3\times 3}$, $\boldsymbol{B} \in \mathbb{R}^{3\times 1}$ and $\boldsymbol{C} \in \mathbb{R}^{1\times 3}$ are, respectively, the state, input and output matrices

$$\boldsymbol{A} = \begin{bmatrix} 0 & \frac{1}{C} & 0 \\ 0 & 0 & 1 \\ 0 & -(3\cdot 2\pi f)^2 & 0 \end{bmatrix},\ \boldsymbol{B} = \begin{bmatrix} -\frac{k_d}{C} \\ 0 \\ 0 \end{bmatrix},\ \boldsymbol{C} = \begin{bmatrix} 1 \\ 0 \\ 0 \end{bmatrix}^T. \tag{28}$$

Since the observability matrix of (26) is full rank, system $\mathcal{S}$ is observable. Thus, it is possible to use the system input and output to construct an estimate of the state vector. In this way, the second step is the design of a state space observer to estimate the sinusoidal disturbance. Specifically, a Luenberger observer, denoted by $\mathcal{S}_o$, is considered in this paper, assuming that the dc-link capacitor voltage difference is measurable. It is defined by the equations

$$\mathcal{S}_o: \begin{cases} \dot{\hat{\boldsymbol{x}}} &= \boldsymbol{A}\hat{\boldsymbol{x}} + \boldsymbol{B}u + \boldsymbol{L}(y - \hat{y}) \\ \hat{y} &= \boldsymbol{C}\hat{\boldsymbol{x}}, \end{cases} \tag{29}$$

where $\hat{\boldsymbol{x}} \in \mathbb{R}^3$ is the estimated state vector described by

$$\hat{\boldsymbol{x}} = \begin{bmatrix} \hat{x}_d & \hat{x}_{\phi_1} & \hat{x}_{\phi_2} \end{bmatrix}^T, \tag{30}$$

the estimated output is $\hat{y} \in \mathbb{R}$, and the observer gain matrix, with dimension 3×1, is represented by $\boldsymbol{L}$. The rest of variables and parameters have been already defined in (26). Consequently, the estimate of the disturbance $\phi(t)$ corresponds to the variable $\hat{x}_{\phi_1}$ of the observer state vector.

The motivation for considering a Luenberger observer is the simplicity in the design and implementation of this state space observer, compared with other possible disturbance estimation approaches. Once the sinusoidal disturbance (24) is expressed as an harmonic oscillator defining system $\mathcal{S}$, this augmented linear system is observable and the application of the observer is direct, only requiring an appropriate selection of the values of the elements of the observer gain matrix $\boldsymbol{L}$. Notice that these elements should be chosen in such a way that the observation error dynamics are faster than the dynamics of system $\mathcal{S}$.

5.2. Control Law

Finally, considering the disturbance estimate provided by the observer, the proposed controller applies this estimated state variable to asymptotically cancel the sinusoidal disturbance that appears in (22). The control law is defined as follows

$$\delta_\gamma = -\frac{1}{k_d}\left(k\left(v_d^* - v_d\right) + k_i \int_0^t \left(v_d^* - v_d\right) d\tau - \hat{x}_{\phi_1}\right). \tag{31}$$

In this way, the controller also includes a PI-type control action, where k is the proportional gain and k_i is the integral gain. Both gains are customary tuning parameters. Note that k_d is the constant defined previously in (23), and v_d^* is the dc-link capacitor voltage difference reference, which is set to zero.

Figure 2 depicts a schematic block diagram of the system, taking into account the final expression (22) of the dc-link capacitor voltage difference dynamics, when both the controller

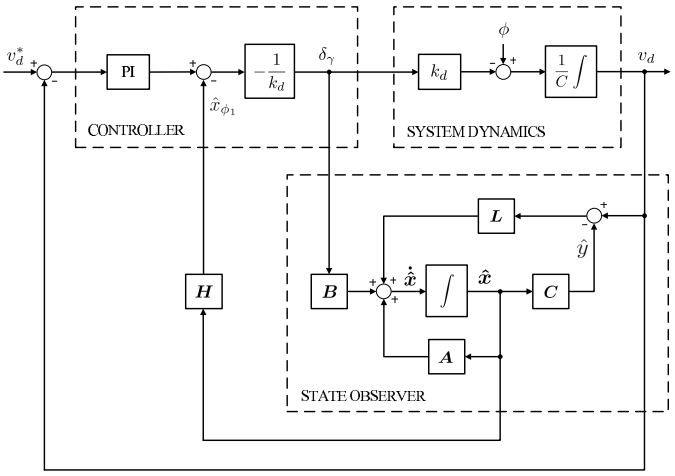


Figure 2: Schematic block diagram of the controller with Luenberger observer.

and the state observer are implemented. The matrix $\boldsymbol{H} \in \mathbb{R}^{1\times 3}$ defined by

$$\boldsymbol{H} = \begin{bmatrix} 0 & 1 & 0 \end{bmatrix}, \tag{32}$$

is introduced to select the estimate of the disturbance, that is, the state variable $\hat{x}_{\phi_1}$ of the observer.

6. Simulation results

This section is devoted to demonstrate the effectiveness of the proposed controller, which is designed with the goal of practically stabilizing the voltage difference between the dc-link capacitors, while attenuating the sinusoidal disturbance present in the neutral point of the dc link as well. For this purpose, the inverter configuration of the three-level NPC converter shown in Fig. 1 together with the proposed voltage balance controller have been implemented and executed under PSCAD environment. The modulation strategy introduced to generate the gating signals of the converter is the space vector modulation presented in [46]. The values of the system parameters considered in the simulation are summarized in Table 2.

It is worth stressing that the system requires other controller to regulate the instantaneous powers, as stated in Section 3. In view of this, the proportional-type direct power control strategy proposed in [47] is adopted, and it is also implemented and executed in PSCAD. The design parameters of this controller together with those of the proposed voltage balance controller are illustrated in Table 3. These parameters are selected in such a way that the assumption of different time scales mentioned in Section 4 is well grounded.

Besides, it should be mentioned that the values of the components of the gain matrix $\boldsymbol{L}$ of the state observer (29) are chosen such that the poles of the observer are faster than the poles of system (26). System $\mathcal{S}$ has three poles: a pair of complex conjugate poles $s_{1,2} = \pm 3\cdot 2\pi f\, j$, which are pure imaginary poles, and a real pole placed at the origin, $s_3 = 0$. Because the value of the grid frequency is 50 Hz, and the simulation has been carried out with a sampling frequency of 5.6 kHz, the poles of the observer have been placed in $s^o_{1,2,3} = -9\cdot 2\pi f$. Thus, these poles are much faster than the poles of the system, but they are slow enough to be well suited for the sampling period.

Table 2: Simulation parameters for the three-level NPC converter.

Parameter	Value
Sampling frequency (f_s)	5.6 kHz
Switching frequency (f_{sw})	5.6 kHz
Grid frequency (f)	50 Hz
Phase voltages (v_{sa}, v_{sb}, v_{sc})	230 V_{RMS}
Total dc-link voltage (V_{dc})	800 V
Inductors (L)	3.5 mH
Capacitors (C_1, C_2)	1100 μF
Instantaneous active power reference (p^*)	10 kW
Instantaneous reactive power reference (q^*)	10 kVAr

Table 3: Design parameters of the voltage balance controller and of the instantaneous power controller.

Design parameter	Value
Voltage balance controller proportional gain (k)	1
Voltage balance controller integral time (k_i)	2.5
Instantaneous power controller constants (k_p, k_q)	$4\cdot 10^{-6}$

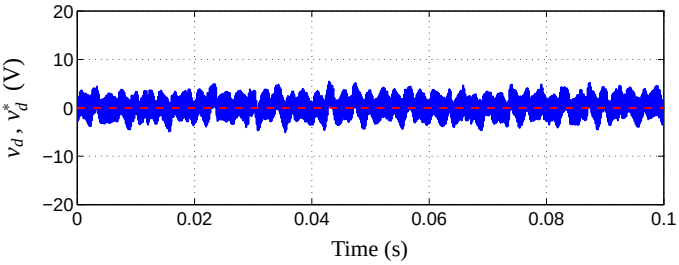


Figure 3: Evolution of v_d (solid) applying the proposed controller, and reference value v_d^* (dashed) of this variable.

Figure 3 illustrates the behavior of the variable v_d, that is, the time evolution of the voltage difference between the dc-link capacitors. In this way, variable v_d is kept close to zero at all times, guaranteeing a solid voltage balancing. In addition, concerning the second of the control objectives described in Section 3, that is, the attenuation of the voltage ripple at three times the fundamental frequency of the grid voltage, notice that applying the proposed controller there is no frequency content at the frequency of the disturbance, i.e., at 150 Hz, as can be seen in Fig. 4. Hence, the second control objective is also achieved.

7. Experimental verification

In order to validate the simulation results obtained before, some experiments have been worked out. To than end, the 50 kVA laboratory prototype of the three-level NPC converter shown in Fig. 5 has been used as inverter, connecting the ac

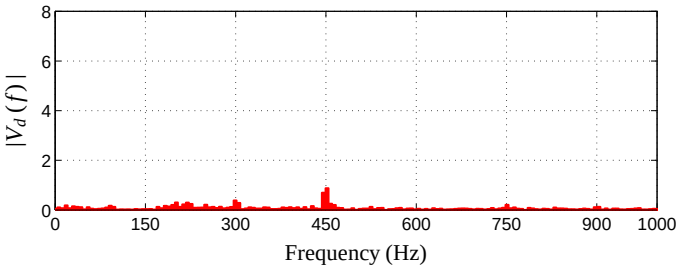


Figure 4: Single-sided amplitude frequency spectrum of the dc-link capacitor voltage difference.

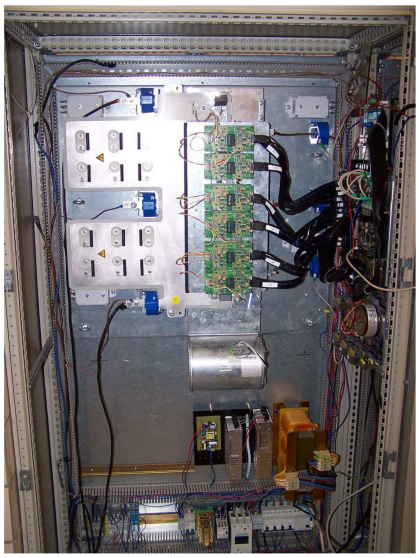


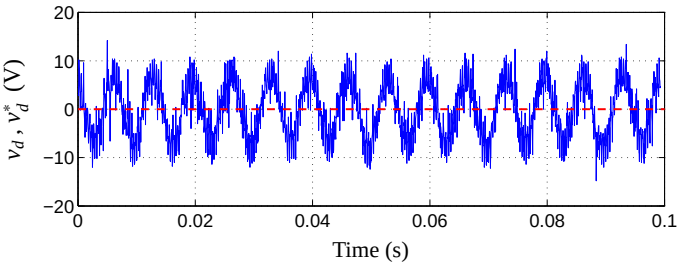
Figure 5: Laboratory prototype: 50 kVA three-phase three-level NPC converter.

side of this converter prototype to the grid. In addition, a digital implementation of the controllers has been executed in a TMS320VC33 floating point DSP homemade board running at 50 MHz. From the control action calculated by the DSP board, the gating signals of the converter power switches are generated by programmable gate logic devices. Besides, the same system parameters described in Table 2 as well as the modulation strategy considered in the previous section have been used in the experiments. It is worth noticing that due to the low computational cost of the modulation strategy considered [46], there is no need of special software optimization of the controllers, so they can be directly implemented in the system.

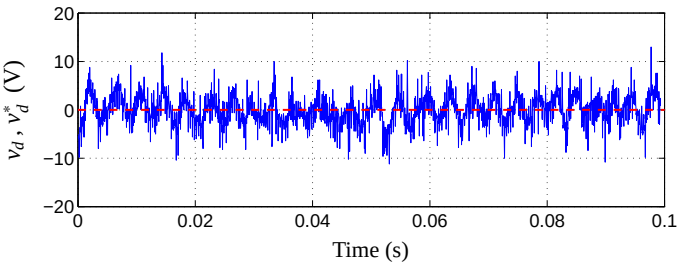
The experiments are focused on the analysis of the steady-state response of the system. In particular, the behavior of the dc-link capacitor voltage difference is studied, comparing the experimental results obtained when two different control algorithms are applied. The first one is the control method proposed in this paper, which is based on a disturbance rejection approach and is developed in Section 5. The second one implements the conventional PI controller defined by

$$\delta_\gamma = -\frac{1}{k_d}\left(k\left(v_d^* - v_d\right) + k_i \int_0^t \left(v_d^* - v_d\right) d\tau\right). \tag{33}$$

Consequently, this PI controller, which is also applied with the



(a) Evolution of v_d (solid) applying a conventional PI controller, and reference value v_d^* (dashed) of this variable.



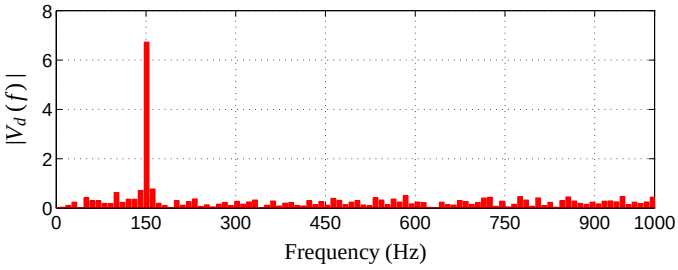
(b) Evolution of v_d (solid) applying the proposed controller, and reference value v_d^* (dashed) of this variable.

Figure 6: Behavior of the difference between the dc-link capacitor voltages during the experiments carried out.

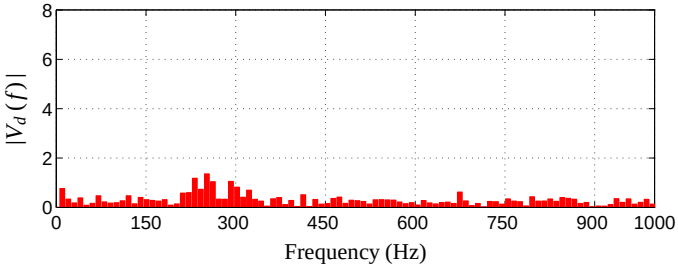
purpose of achieving the capacitor voltage balancing, does not include any estimate of the sinusoidal disturbance (24). Besides, identical tuning parameters k and k_i have been used for both controllers. They are illustrated in Table 3, together with the parameters of the instantaneous power controller also implemented in the system.

Figure 6 depicts the evolution of variable v_d. The two voltage balance controllers considered show solid performance concerning the requirement of practical stability of the system, because the voltage difference is kept close to zero. The results obtained are better when the disturbance estimate of the state observer is included in the control law, since v_d remains around zero presenting lower voltage deviations with respect to the reference v_d^*. These voltage deviations are lower that approximately 10 V, so they represent, in the worst of the situations, 2.5% of the reference of each dc-link capacitor voltage, denoted by v_c^*. Note that, in the three-level NPC converter, there are two capacitors in the dc link, so v_c^* is defined by the half of the total dc-link voltage, which is in this case $V_{dc} = 800$ V.

However, the main difference between the application of either the proposed controller or the conventional PI controller is related to the attenuation of the low-frequency ripple present in the dc link, which is the main benefit of the controller proposed in this paper. Figure 7 illustrates the amplitude frequency spectrums of the variable v_d. Considering the controller based on the disturbance rejection approach, there is a very important reduction of the frequency content at the frequency of the disturbance, that is, at 150 Hz. In this way, there is almost an exact disturbance cancelation, as can be seen in Fig. 7(b). In contrast, when the PI controller is implemented, the frequency content at



(a) Single-sided amplitude frequency spectrum of v_d, when a PI controller is implemented.



(b) Single-sided amplitude frequency spectrum of v_d, when the proposed controller is implemented.

Figure 7: Single-sided amplitude frequency spectrums of the difference between the dc-link capacitor voltages obtained experimentally.

that particular frequency is much higher, since the controller is not designed to mitigate the effects caused by the disturbance. Essentially, this result is due to the fact that the PI controller does not incorporate in the feedback any specific reduplicated model or approximation of the dynamic structure of the disturbance to reject [33]. Therefore, the proposed control method provides better results, and it is able to deal with the problems associated with the dc-link capacitor voltages of the converter.

Besides, regarding the evolution of v_d depicted in Fig. 6(b) and the one that this variable presents in a simulation environment in Fig. 3, note that both show quite similar behaviors. The voltage deviations of v_d with respect to its reference are some volts higher in Fig. 6(b), but this is a typical situation when comparing real and practical cases with idealised ones. Additionally, the mitigation of the dc-link voltage ripple is achieved in the experimental test as well as in the simulation. Hence, the experimental results obtained serve to validate the proposed control method but also to corroborate the mathematical analysis carried out previously in Section 4, supporting in this way the approximated model (22) valid for any converter operating point derived from this analysis.

Finally, Fig. 8 shows the phase currents of the system, when the instantaneous active and reactive power references are set to $p^* = 10$ kW and $q^* = 10$ kVAr, respectively. It is worth stressing that the regulation of these variables is carried out indirectly via the adopted direct power control strategy [47]. In addition, it should be mentioned that since no fourth wire is introduced in the NPC system addressed in this paper, the effects of the low-frequency voltage ripple present in the dc link, with or without compensation, are not significant in the phase current behavior.

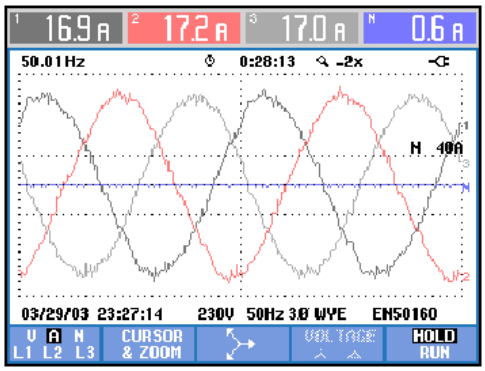


Figure 8: Phase currents of the system obtained experimentally.

8. Conclusions

This paper has coped with several problems associated with the dc-link capacitor voltages of the three-level NPC converter. Specifically, it has coped with the imbalance problem of the capacitor voltages and with the problem of the presence of a low-frequency voltage ripple in the dc link. Considering a continuous model of the converter, an analysis of the converter dynamics has led to an approximated model that allows treating both problems together using the classical formulation of a problem of regulating the output of a system subject to disturbances. This key result facilitates the design of the proposed controller, which is based on an asymptotic disturbance rejection approach.

Focusing on the experiments carried out, the results obtained have proved the solid performance and usefulness of the proposed controller, which is able to carry out the balancing of the dc-link capacitor voltages, achieving almost an exact disturbance cancelation. It also has been shown that if no specific action is introduced to reduce the dc-link voltage ripple, its damaging effect is not mitigated. Besides, it should me mentioned that the implementation of the controller is not difficult and does not require additional elements, which is a relevant feature, and that the computational time is low.

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References

[1] Nabae, A., Takahashi, I., & Akagi, H. (1981). A new neutral-point clamped PWM inverter. *IEEE Transactions on Industry Applications*, IA-17(5):518–523.

[2] Celanovic, N., & Boroyevich, D. (2000). A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters. *IEEE Transactions on Power Electronics*, 15(2):242–249.

[3] Pou, J., Pindado, R., Boroyevich, D., & Rodríguez, P. (2005). Evaluation of the low-frequency neutral-point voltage oscillations in the three-level inverter. *IEEE Transactions on Industrial Electronics*, 52(6):1582–1588.

[4] Rodríguez, J., Bernet, S., Steimer, P. K., & Lizama, I. E. (2010). A survey on neutral-point-clamped inverters. *IEEE Transactions on Industrial Electronics*, 57(7):2219–2230.

[5] Abu-Rub, H., Holtz, J., Rodríguez, J., & Baoming, G. (2010). Medium-voltage multilevel converters – state of the art, challenges, and requirements in industrial applications. *IEEE Transactions on Industrial Electronics*, 57(8):2581–2596.

[6] Ceballos, S., Pou, J., Zaragoza, J., Robles, E., Villate, J. L., & Martín, J. L. (2011). Fault-tolerant neutral-point-clamped converter solutions based on including a fourth resonant leg. *IEEE Transactions on Power Electronics*, 58(6):2293–2303.

[7] Busquets-Monge, S., Somavilla, S., Bordonau, J., & Boroyevich, D. (2007). Capacitor voltage balance for the neutral-point-clamped converter using the virtual space vector concept with optimized spectral performance. *IEEE Transactions on Power Electronics*, 22(4):1128–1135.

[8] Pou, J., Zaragoza, J., Rodríguez, P., Ceballos, S., Sala, V. M., Burgos, R. P., & Boroyevich, D. (2007). Fast-processing modulation strategy for the neutral-point-clamped converter with total elimination of low-frequency voltage oscillations in the neutral point. *IEEE Transactions on Industrial Electronics*, 54(4):2288–2294.

[9] Pou, J., Zaragoza, J., Ceballos, S., Saeedifard, M., & Boroyevich, D. (2012). A carrier-based PWM strategy with zero-sequence voltage injection for a three-level neutral-point-clamped converter. *IEEE Transactions on Power Electronics*, 27(2):642–651.

[10] Maheshwari, R., Munk-Nielsen, S., & Busquets-Monge, S. (2013). Design of neutral-point voltage controller of a three-level NPC inverter with small dc-link capacitors. *IEEE Transactions on Industrial Electronics*, 60(5):1861–1871.

[11] Umbría, F., Gordillo, F., Salas, F., & Vázquez, S. (2010). Voltages balance control in three phase three-level NPC rectifiers. *Proceedings of the 19th IEEE International Symposium on Industrial Electronics - ISIE'10* (pp. 3018–3023), Bari, Italy.

[12] du Toit Mouton, H. (2002). Natural balancing of three-level neutral-point-clamped PWM inverters. *IEEE Transactions on Industrial Electronics*, 49(5):1017–1025.

[13] Shen, J., Schröder, S., Rösner, R., & El-Barbari, S. (2011). A comprehensive study of neutral-point self-balancing effect in neutral-point-clamped three-level inverters. *IEEE Transactions on Power Electronics*, 26(11):3084–3095.

[14] Lewicki, A., Krzeminski, Z., & Abu-Rub, H. (2011). Space-vector pulsewidth modulation for three-level NPC converter with the neutral point voltage control. *IEEE Transactions on Industrial Electronics*, 58(11):5076–5086.

[15] Akagi, H., & Hatada, T. (2009). Voltage balancing control for a three-level diode-clamped converter in a medium-voltage transformerless hybrid active filter. *IEEE Transactions on Power Electronics*, 24(3):571–579.

[16] Vargas, R., Cortés, P., Ammann, U., Rodríguez, J., & Pontt, J. (2007). Predictive control of a three-phase neutral-point-clamped inverter. *IEEE Transactions on Industrial Electronics*, 54(5):2697–2705.

[17] Shen, J., Schröder, S., Duro, B., & Roesner, R. (2013). A neutral-point balancing controller for a three-level inverter with full power-factor range and low distortion. *IEEE Transactions on Industry Applications*, 49(1):138–148.

[18] Malinowski, M., Stynski, S., Kolomyjski, W., & Kazmierkowski, M. P. (2009). Control of three-level PWM converter applied to variable-speed-type turbines. *IEEE Transactions on Industrial Electronics*, 56(1):69–77.

[19] Portillo, R. C., Prats, M. M., León, J. I., Sánchez, J. A., Carrasco, J. M., Galván, E., & Franquelo, L. G. (2006). Modeling strategy for back-to-back three-level converters applied to high-power wind turbines. *IEEE Transactions on Industrial Electronics*, 53(5):1483–1491.

[20] Umbría, F., Gómez-Estern, F., Gordillo, F., & Salas, F. (2013). Voltage balancing in five-level diode-clamped power converters. *Proceedings of the 9th IFAC Symposium on Nonlinear Control Systems - NOLCOS'13* (pp. 365–370), Toulouse, France.

[21] Umbría, F., Gordillo, F., Salas, F., Aracil, J., & Gómez-Estern, F. (2013). Asymptotic rejection of sinusoidal disturbances based voltage balance control in back-to-back power converters. *International Journal of Robust and Nonlinear Control*, 1–21 (doi: 10.1002/rnc.3036).

[22] Francis, B. A. (1977). The linear multivariable regulator problem. *SIAM Journal on Control and Optimization*, 15(3):486–505.

[23] Isidori, A., & Byrnes, C. I. (1990). Output regulation of nonlinear systems. *IEEE Transactions on Automatic Control*, 35(2):131–140.

[24] Schonek, J. (2001). The singularities of the third harmonic. *Cahier Technique Schneider Electric*, 202:1–16.

[25] Zhong, Q.-C., Liang, J., Weiss, G., Feng, C., & Green, T. C. (2006). H^{∞} control of the neutral point in four-wire three-phase dc-ac converters. *IEEE Transactions on Industrial Electronics*, 53(5):1594–1602.

[26] Leva, A., & Piroddi, L. (2011). FPGA-based implementation of high-speed active noise and vibration controllers. *Control Engineering Practice*, 19(8):798–808.

[27] Xu, C., & Tomizuka, M. (2012). A minimum parameter adaptive approach for rejecting multiple narrow-band disturbances with application to hard disk drives. *IEEE Transactions on Control Systems Technology*, 20(2):408–415.

[28] Patt, D., Liu, L., Chandrasekar, J., Bernstein, D. S., & Friedmann, P. P. (2005). Higher-harmonic-control algorithm for helicopter vibration reduction revisited. *Journal of Guidance, Control, and Dynamics*, 28(5):918–930.

[29] Chen, D., & Paden, B. (1993). Adaptive linearization of hybrid step motors: stability analysis. *IEEE Transactions on Automatic Control*, 38(6):874–887.

[30] Landau, I. D., Alma, M., Constantinescu, A., Martinez, J. J., & Noë, M. (2011). Adaptive regulation – rejection of unknown multiple narrow band disturbances (a review on algorithms and applications). *Control Engineering Practice*, 19(10):1168–1181.

[31] Li, R., & Khalil, H. K. (2012). Nonlinear output regulation with adaptive conditional servocompensator. *Automatica*, 48(10):2550–2559.

[32] Pigg, S., & Bodson, M. (2013). Adaptive harmonic steady-state disturbance rejection with frequency tracking. *Asian Journal of Control*, 15(1):1–10.

[33] Francis, B. A., & Wonham, W. M. (1976). The internal model principle of control theory. *Automatica*, 12(5):457–465.

[34] Brown, L. J., & Zhang, Q. (2004). Periodic disturbance cancellation with uncertain frequency. *Automatica*, 40(4):631–637.

[35] Guo, X., & Bodson, M. (2012). Adaptive rejection of disturbances having two sinusoidal components with close and unknown frequencies. *Asian Journal of Control 2012*, 14(1):36–44.

[36] Orivuori, J., Zazas, I., & Daley, S. (2012). Active control of frequency varying disturbances in a diesel engine. *Control Engineering Practice*, 20(11):1206–1219.

[37] Marino, R., Santosuosso, G. L., & Tomei, P. (2003). Robust adaptive compensation of biased sinusoidal disturbances with unknown frequencies. *Automatica*, 39(10):1755–1761.

[38] Ding, Z. (2003). Global stabilization and disturbance suppression of a class of nonlinear systems with uncertain internal model. *Automatica*, 39(3):471–479.

[39] Umbría, F., Vázquez, S., Gordillo, F., & Gómez-Estern, F. (2009). Observer-based direct power control for three-level NPC rectifiers. *Proceedings of the 35th Annual Conference of the IEEE Industrial Electronics Society - IECON'09* (pp. 1663–1668), Porto, Portugal.

[40] LaSalle, J. P., & Lefschetz, S. (1961). *Stability by Liapunov's direct method with applications*. Academic Press: New York, NY, USA.

[41] Khalil, H. K. (2002). *Nonlinear systems* (3rd edition). Prentice Hall: Upper Saddle River, NJ, USA.

[42] Aguilera, R. P., & Quevedo, D. E. (2011). On the stability of MPC with a finite input alphabet. *Proceedings of the 18th World Congress of the International Federation of Automatic Control - IFAC'11* (pp. 7975–7980), Milan, Italy.

[43] Umbría, F., Aracil, J., Gordillo, F., Salas, F., Sánchez, J. A. (2013). Three-time-scale singular perturbation stability analysis of three-phase power converters. *Asian Journal of Control*, 1–12 (doi: 10.1002/asjc.818).

[44] Isidori, A. (1995). *Nonlinear control systems* (3rd edition). Springer-Verlag: London, England, UK.

[45] Marconi, L., & Praly, L. (2008). Uniform practical nonlinear output regulation. *IEEE Transactions on Automatic Control*, 53(5):1184–1202.

[46] Prats, M. M., Franquelo, L. G., Portillo, R., León, J. I., Galván, E., & Carrasco, J. M. (2003). A 3-D space vector modulation generalized algorithm for multilevel converters. *IEEE Power Electronics Letters*, 1(4):110–114.

[47] Vázquez, S., Sánchez, J. A., Carrasco, J. M., León, J. I., & Galván, E. (2008). A model-based direct power control for three-phase power converters. *IEEE Transactions on Industrial Electronics*, 55(4):1647–1657.