Preliminary experiments for the fabrication of thermally actuated bimorph cantilever arrays on non-silicon wafers with vertical interconnects

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Abstract:

This paper describes the first steps for the fabrication of low-cost cantilever arrays, developed at RAL, on non-silicon polymer substrates with vertical interconnects, produced at Profactor. The deflection and actuation of these cantilevers is based on the bimorph thermal actuation principle. The fabrication of the cantilever arrays requires many process steps which are presented in this article. The first step is the planarization between the via-holes interconnects with a uniform layer. This was achieved by spin coating of a thick (~58µm) SU-8 layer. In the subsequent step, two thin metal layers of Cr (500Å) and Au (1000Å) were thermally deposited and patterned, using UV lithography with a mask alignment process and wet etching. The following step was the coating of a 1µm structural Au layer, in which the deposited layer had a very poor adhesion. Alternative procedures were explored to overcome this problem in the future. Modifications of the photo masks design and the substrates will be carried out to make the RAL microcantilevers technology more compatible with Profactor substrates.

Keywords: bimorph cantilever, vertical interconnect, epoxy glass fibre, FR4

1. Introduction

Low-cost cantilever arrays on non-silicon wafers are of great interest for fabricating microsystems such as autonomous mobile platforms for microrobots. In order to fabricate the arrays of cantilevers on one side of the substrate and add batteries to the other side, vertical interconnects have been used. A system with vertical interconnects presents considerable improvement in packing because of compacter and denser circuit board wiring. The exploration for alternative materials (other than silicon) was done to reduce the weight and costs of fabrication of the devices. Non-silicon substrates with vertical interconnects for the production of the cantilever arrays, which are based on the bimorph thermal actuation principle were studied. This can be the innovative approach which paves the way for highly efficient mechanical and electrical integration of polymer actuator devices.

2. Design and development

Choosing the appropriate substrate material was the first challenge. The wafer had to be cheap, light, and thermally stable with specific mechanical and electrical properties.

2.1. Non-silicon wafers; comparison and selection

The survey of substrate materials was focused mainly on studying two different classes: ceramics and polymers. The following important features were taken into account : dimension and thickness of the plate; distribution, number and diameter of the through holes as well as method of making via-holes, metallization and planarization processes.

Some of the useful properties of ceramics include high melting temperature, wear resistance, and corrosion resistance. Many ceramics are good electrical and thermal insulators. Table 1 below shows selected properties of different ceramics. From among different ceramics shown below, aluminum and zirconium oxides were chosen due to their excellent thermal properties, mechanical characteristic and reasonable price. Al_2O_3 is the most cost effective and widely used material in the family of engineering ceramics. On the other hand ZrO_2 is an extremely refractory material. It offers chemical and corrosion inertness to temperatures well above the melting point of alumina. The material has ten times lower thermal conductivity then silicon.

Polymers are useful because they are low weighted, corrosion resistant and easy to process at low temperatures. However the biggest advantage is their low cost. Polymers have in general low strength that can be improved by reinforcing them with other structures transforming them into composite materials. Table 2 shows selected properties of different polymeric materials.

Table 1. Selected properties of ceramics [1].

Mechanical and Physical Properties of Some Common Engineering Ceramics

	Zirconia Y-stabilised $ZrO_2(Y_2O_3)$	Silicon Carbide SiC	Aluminium Titanate Al_2TiO_5	Titanium Diboride TiB_2	Aluminium Oxide Al_2O_3	Stainless Steel
Bending Strength (MPa)	1000	400	30	600	350	200 (σ_y) 490 (σ_r)
Compressive Strength (MPa)	2200	2200	200	3000	4100	200 (σ_y) 490 (σ_r)
E-modulus (GPa)	210	400	20	570	390	200
Resistivity (ohm·cm)	$25\,10^{12}$	10^{-1}	---	$1.5\,10^{-7}$	10^{14}	10^{-4}
Thermal Expansion ($10^{-6}K^{-1}$)	10.5	3.5	1.0	7.2	7.5	16.8
Thermal Conductivity ($Wm^{-1}K^{-1}$)	1.5	100	1.4	110	30	15

Table 2. Selected properties of different polymeric materials [2].

Group	Composition	Tg	ε_r	Relative costs
BT	Bismaleinimide-triazine resin with silica glass	180-220	3.9-4.9	5.3
CE	Cyanate ester with silica glass	230	3.6	4.5
CEM1	Paper phenolic core with FR4-outer layers	130	4.7	0.95
CEM3	Glass mat (or glass felt) core with FR4-outer layers	130	5.2	0.95
FR2	Phenolic resin paper	105	4.7	0.73
FR3	Epoxy paper	110	4.9	0.85
FR4	Epoxy glass fibre laminate	135-170	4.7	1 Reference
FR5	Epoxy glass fibre laminate with crosslinked resin system	160	4.6	1.4
PD	Polyimide resin	260	4.2-4.6	6.5

After studying those two groups of different materials in respect of cost and quality, the Epoxy glass fiber (FR4) laminate has been selected. Epoxy glass laminate belong to high pressure laminated materials. They are made out of base material impregnated with a particular resin system. Due to the high pressure lamination process, these materials typically have very high mechanical strength characteristics, and good electrical and thermal properties at the same time these substrates are much cheaper than Si. Even though alumina has better thermal and mechanical properties, the wafer processing costs are considerably reduced by using FR4 with parameters coming up with our requirements.

2.2. Vertical interconnects

Vertical interconnects are essential and in some cases irreplaceable for production of complicated and advanced micro-tools and micro-systems. Such interconnects have reduced interconnect distances, thus resistance, parasitic capacitance and inductance are reduced. This means that the power consumption is lower and signal processing is faster. A system with vertical interconnects presents also considerable improvement in packing density and packaging itself can be performed much easier in some applications.

In this work, the vertical interconnects have been used to fabricate arrays of bimorph cantilevers on one side of the substrate and batteries added to the other side. That means less area is lost for wiring and the weight of the system containing such connects is reduced.

Figure 1 shows the design of FR4 substrate with via-holes and a cantilever array above (a), and a picture of the via-holes taken by an optical microscope (b).

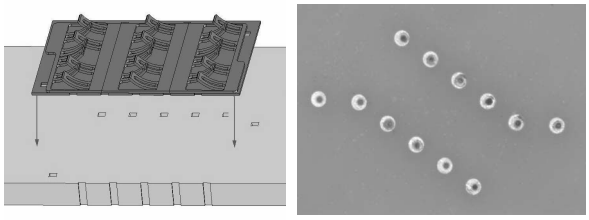

Fig. 1. Design of FR4 substrate with via-holes and a cantilever array above (a), the image taken by an optical microscope (b).

2.3. Low cost bimorph cantilever arrays

The micromachined cantilever is a very sensitive and versatile sensor with broad applications in a variety of fields, including surface science, lithography, data storage, and biology, as the tip can be functionalized to measure magnetic, electrical, thermal, chemical, stress, and flow signals [3].

Silicon based cantilevers are rather expensive, therefore there is a need for alternative materials. Polymers are the promising materials for cantilevers that are competitive with silicon. Polymer based cantilevers have smaller young modulus than silicon and they can be more sensitive than similar silicon based cantilevers.

The cantilever used here consists of a sandwich of structural materials with different coefficients of thermal expansion (CTE) and is thermally activated. If the cantilever comprises two different layers, then it is know as bimorph structure. In case that the top layer has a greater CTE than the bottom layer, the cantilever curls when cooled and flattens when heated. For actuation of the microstructures, microheaters are embedded in the bimorph layers and short current pulses from an external supply are used to activate the structure [4, 5, 6].

3. Experimental methods and results

The substrates used were wafers of epoxy glass fiber (FR4) that were drilled and electroplated with Ni, to produce the via-holes that protrude the surface of the substrate in a average height of 58μm.

The design of the via-holes was made according to requirements of RAL's cantilever process in order to fit the cantilevers arrays (diameter dimension and thickness of the plate as well as the distribution, number and diameter of the through holes) (fig. 1). Polyimide-gold bimorphs where chosen due to simplicity of fabrication and large initial deflection [4]. The cantilevers are designed with 600μm length, 80μm width and 10μm thickness [5, 6].

Figure 2 shows the epoxy glass fiber 4'' wafer with via-holes metalized with Ni and a SEM image of polyimide-gold bimorph cantilever arrays.

Forming the cantilever arrays requires many fabrication steps, as outlined in Figure 3 and 4 [5,6].

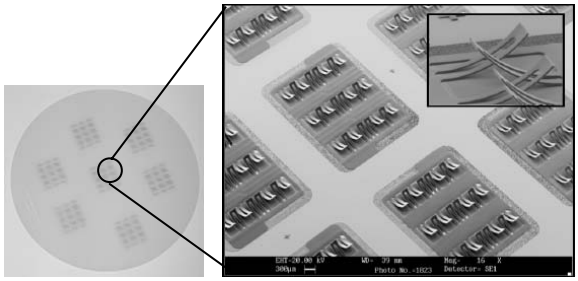

Fig. 2. The FR4 wafer with via-holes metalized with Ni (left), SEM image of polyimide-gold bimorph arrays (right) [6].

Based on the existing technology developed at RAL for the fabrication of the bimorph cantilevers, the following steps are made to combine the cantilever arrays with the novel substrates:

1. The wafer is coated with an SU-8 photoresist layer to planarize the surface between the via-holes.
2. A thin layer of Cr is deposited to promote adhesion, followed by a layer of Au immediately afterwards, to prevent oxidation of Cr. These layers are patterned, by standard lithography and wet etching techniques,

to define the areas where the final structures will be released.

3. A structural Au layer is deposited by plasma sputtering, followed by a Cr layer to act as an adhesion promoter for the subsequent polyimide layer.
4. Polyimide (2μm thick) is spin coated and soft baked at 120°C in an oven for 20min.
5. An Al coating is sputtered onto the wafer and patterned to form the heater tracks, contact pads and signal lines.
6. A second layer of polyimide (2μm thick) is spin coated to embed the microheater structure for improved thermal insulation and also mechanical protection. Standard photolithography and wet chemical etching is used to pattern the polyimide
7. After the formation of the bimorph structures a wet Au etching is performed to release the cantilevers.

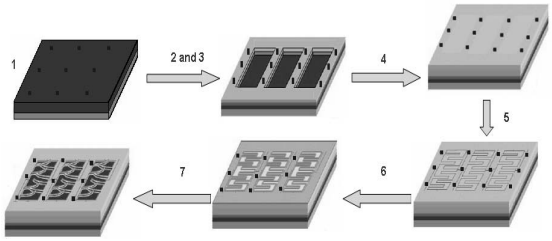

Fig. 3. Fabrication of bimorph cantilevers [6].

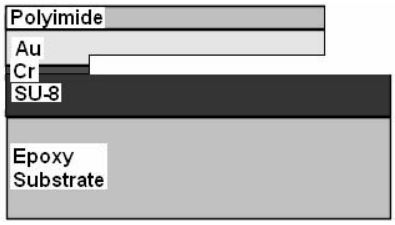

Fig. 4: Cross section of the bimorph structure after the release of the cantilevers.

The following preliminary experiments were performed:

The substrate was cleaned with acetone (Sigma) and DI water, followed by dehydration bake at 120°C for 10min. The SU8-2035 (Microchem) was dispensed by pouring on the wafer directly from the bottle and spin-coated next. Pre-exposure bake was performed on a hotplate. The resist is exposed to UV light, using MA6 Karl Suss Mask Aligner, and finally post exposure baked on a hotplate. The resist thickness and surface profile is measured using a Zygo New View 200 optical profilometer and Tencor P15 profilometer (Fig. 5 & 6).

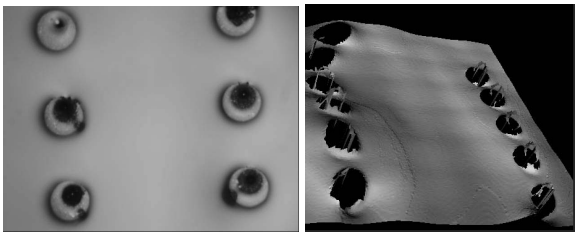

Fig. 5. Optical microscope (left) and optical profilometry (right) images after planarization.

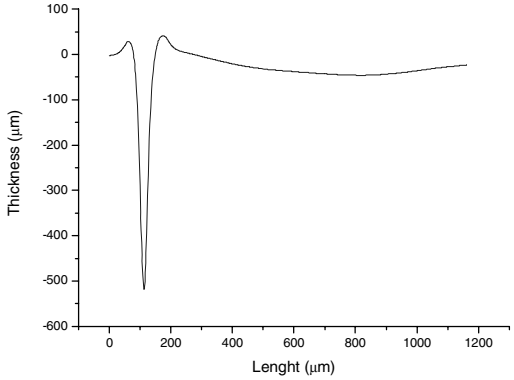

Fig. 6: Surface profile for the 58μm thick SU-8 planarization layer.

A 500Å Cr layer was deposited followed by a 1000Å Au layer using an electron beam thermal evaporator (SVS V2000). The sample was spin coated (Karl Suss Gyrset spinner) with 2mL dispensed JSR resist (JSR Corporation). The resist was exposed for 8s to UV light using the mask aligner in soft contact mode. The next step was the wet chemical etching of Au, by immersion in Gold Etchant (Rockwood) for 8s, and of Cr, by immersion in Cr Etch (Rockwood) for 12s (fig. 6).

Finally the patterned sample is flood exposed for 12s and developed in TMA238WA (Clariant) for 3min, followed by plasma descum. Figure 7 shows samples after the Au deposition.

A 1μm gold layer was deposited using a CVC Veeco Systems plasma sputtering.

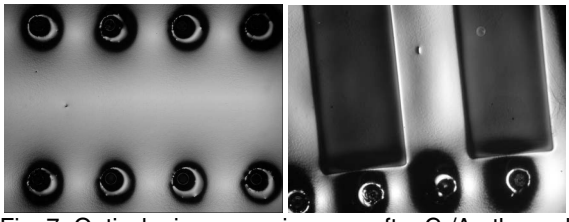

Fig. 7. Optical microscope images: after Cr/Au thermal deposition (left); after the first pattering (right).

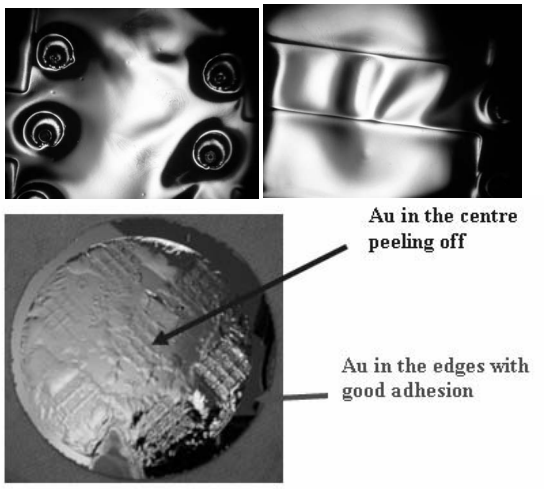

Fig. 8. Optical microscope images (top) and picture of the wafer (bottom) after Au coating with plasma sputtering.

4. Discussion and future outlook

The planarization step by spin coating of SU-8 was successful, generating a uniform surface between the via-holes (fig. 5 and 6). The layer surface was found suitable for the next fabrication steps of the cantilevers. The best results were achieved with a SU-8 thickness of 58μm, in a single coating step. It should be noted that 58μm is also the average height of the protruding via-holes. The deposition of thicker SU-8 layers would cause the total covering of the protruding via-holes in some parts of the wafer, due to the edge bead effect. On the other hand, thinner layers of SU-8 had a more uneven and wavy surface between the via-holes. The thermal deposition and patterning of the thin Cr/Au layers was also successful (fig. 7).

The deposition of the 1μm structural Au layer generated a coating with very poor adhesion in the areas with the previously deposited Cr/Au layers (fig.8). The loss of film adhesion is caused both by high stress and weak bonding at the interface to the adjoining layer or substrate. The results show delamination in the film, which forms an uneven top surface with bubbles and "mole tunnels" underneath [7]. However, in the areas at the edge of the wafer, which had only an SU-8 coating and no Cr/Au layer prior to the thick Au layer deposition, the adhesion of the thick Au layer was good. This problem of bad adhesion of the Au layer after the plasma sputtering must be overcome. Some of the suggestions are: more efficient cleaning of the wafers (using other solvents and ultra sounds), replacing of the thin Cr layer by another metal (like Al or Ti) and performing plasma etching on the SU-8 surface to improve the adhesion of the thermally deposited metal layers.

Additional modifications in the RAL cantilevers masks design must be done to make the electric pads of the cantilevers compatible with the metallic interconnects of Profactor's wafers. In addition, it will be necessary to hard bake the polyimide layers at temperatures lower than the glass transition of the substrates instead of the hardbake temperature recommended in the material datasheet for polyimide. The possibility of using other types of substrates (alumina or zirconium oxides) is of consideration. Although more expensive, they offer excellent thermal and mechanical properties and will not require the planarization layer.

5. Conclusions

The aim of this work was to combine the FR4 epoxy substrates with metalized via-holes from Profactor with the cantilever arrays technology from RAL.

The epoxy glass fiber has been chosen as the alternative material for silicon. The wafer processing cost is reduced while showing very good mechanical, electrical and thermal properties. After selecting the preferred material for substrates, designing and machining of vertical interconnects was carried out. After the planarization of the substrate with a thick SU-8 layer and the subsequent metallization was achieved, the plasma deposition of Au was not successful due to bad adhesion between the Cr/Au/SU-8 layer and the thick Au layer.. Alternative methods were evaluated to overcome this problem. Also other process modifications were foreseen, in order to achieve the complete fabrication of the bimorph cantilevers.

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