DISEÑO DE CIRCUITOS INTEGRADOS PARA INTERFACES NEURONALES IMPLANTABLES

INTEGRATED CIRCUIT DESIGN FOR IMPLANTABLE NEURAL INTERFACES

José Luis Valtierra Sánchez de la Vega

Tesis presentada para la obtención del
Grado de Doctor

Departamento de Electrónica y Electromagnetismo
Universidad de Sevilla

Abstract

by José Luis Valtierra Sánchez de la Vega

Progress in microfabrication technology has opened the way for new possibilities in neuroscience and medicine. Chronic, biocompatible brain implants with recording and stimulation capabilities provided by embedded electronics have been successfully demonstrated. However, more ambitious applications call for improvements in every aspect of existing implementations. This thesis proposes two prototypes that advance the field in significant ways. The first prototype is a neural recording front-end with spectral selectivity capabilities that implements a design strategy that leads to the lowest reported power consumption as compared to the state of the art. The second one is a bidirectional front-end for closed-loop neuromodulation that accounts for self-interference and impedance mismatch thus enabling simultaneous recording and stimulation. The design process and experimental verification of both prototypes is presented herein.

Acknowledgements

First of all, I am deeply grateful to Manuel Delgado Restituto and Ángel Rodríguez-Vázquez for their invaluable advice, guidance and support for this work's vision.

I must thank Norberto Pérez Prieto and Rafaella Fiorelli, their direct involvement in many aspects of this work was fundamental for its completion.

I shuold also thank everyone at PA-34 for keeping my sanity.

Finally, I feel obligated to communicate the support of CONACyT via scholarship 385244.

Contents

List of Figures

List of Tables

Chapter 1

Introduction and Background

Research in neural implants has significantly increased in the last few years owing to parallel progress in the fields of microelectronic circuits, material science and neuroscience. In its most basic form, an implant either *reads* (records) from the brain, *writes* (stimulates) in it, or both. This operation is executed by a neural interface which is in turn governed by some sort of digital controller. A neural implant is also known as a neuroprosthesis or brain chip.

1.1 Electrode-Electrolyte interface

The definitions vary depending on the setup but in general a neural implant is comprised by an electrode, which in practice is typically a microelectrode array (Fig. 1.1), and in-situ integrated electronics where recording and/or stimulation takes place. The electrode is the medium through which neural signals reach the electronics (recording) or the current reaches the brain tissue (stimulation). When a metal (e.g. electrode) is put in contact with an electrolyte (e.g. brain tissue) a double layer of charge modeled as a capacitance (C_{DL}) emerges from its unequal distribution across the interface [1]. In addition, charge leaked across the interface experiences a faradaic resistance (R_{CT}) while a diffusion current from the electrolyte experiences an impedance (Z_W). Finally, the resistance of the electrolyte is modeled as resistance R_S. These four elements constitute the model for the electrode-electrolyte interface (Fig. 1.2).

The characteristics of the electrode drive fundamental specifications for recording and stimulation. Although data regarding characterization of electrodes is generally available, their characteristics tend to change due to temperature, mechanical stress and

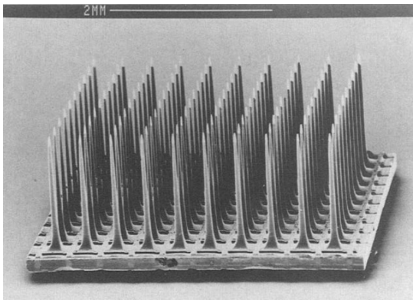

FIGURE 1.1: Micrograph of the Utah array (from [2])

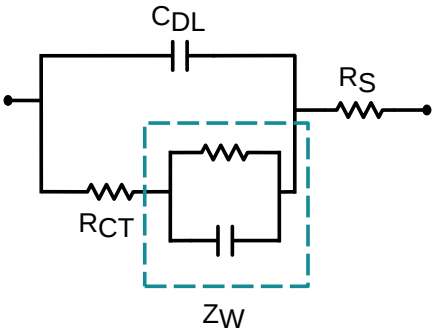

FIGURE 1.2: Electrode model

quality of the implant. In any case, taking into account the electrode from the very beginning of the interface design is a must. It should be said that a single C_{DL} is enough to model the interface for electrical simulation purposes [3].

1.2 Neural Recording

Neural signals are typically recorded by an amplifier in direct contact with an the electrode. This section covers the basics of said signals as well as the considerations to record them.

1.2.1 Neural Signals

Extracellular electric fields in the brain cortex are the product of multiple cellular processes [4]. At low frequencies (¡ 500 Hz), contributions mainly from synaptic events give rise to an arrhythmic broadband field with narrow-band oscillations known as the local field potential (LFP) [5]. Spectral power is concentrated at lower frequencies (Fig.1.3(a)) and exhibits several oscillation bands across the spectrum [6] (Fig. 1.3(b)). At higher frequencies (¿ 500 Hz) and up to 5-10 kHz, action potentials (AP) or spikes are the main

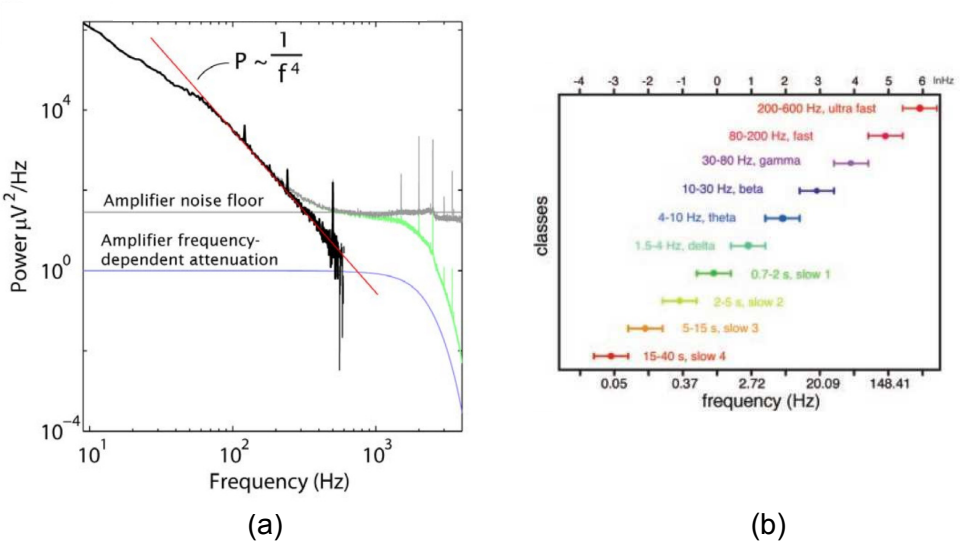

FIGURE 1.3: (a) LFP frequency spectrum (from [8]) (b) LFP oscillation bands (from [6])

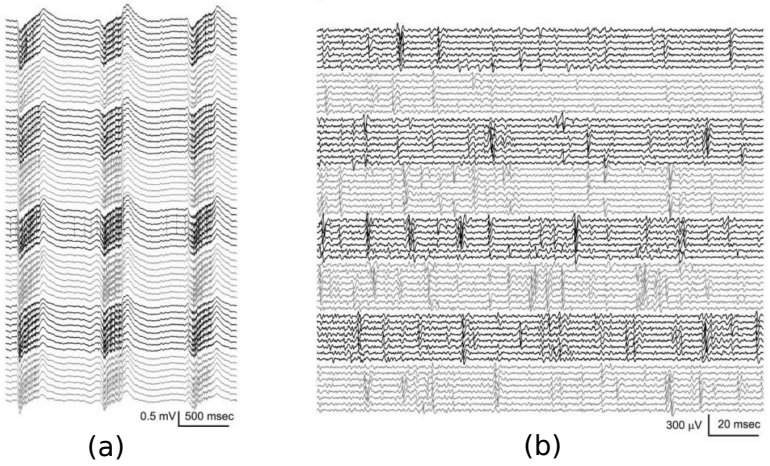

FIGURE 1.4: Extracellular field recording from (a) 1 Hz to 5 kHz (b) 500 Hz to 5 kHz (from [9])

contributors to the extracellular electric field [4]. Spikes fire across frequency as a white spectrum [7] and each one of them represents the activity of a single neuron. Fig. 1.4 shows extracelullar action potential recordings from a 64-site array.

The extracellular electric field in the brain can be detected as a voltage signal at different observational levels (Fig. 1.5). Each level is related to the anatomical place where the detection takes place. Detection at each level differs from the others in neural signal

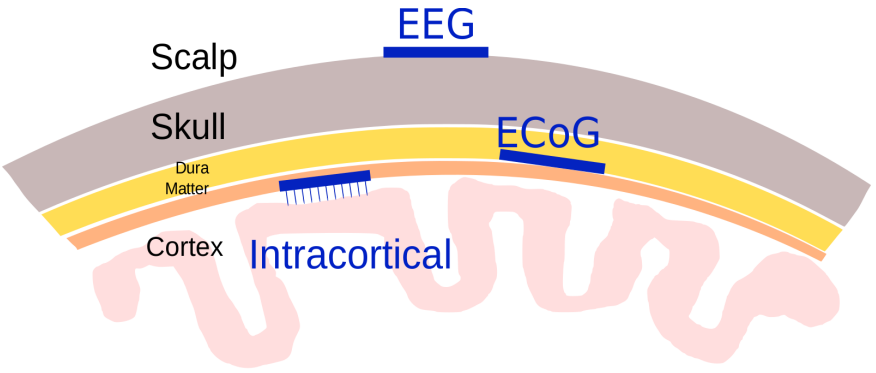

FIGURE 1.5: Observational levels.

magnitude as well as environment-specific constraints to the point that each observational level is considered a unique technique. In general, detection requires an electrode in addition to amplification electronics. Each technique offers different advantages in terms of mobility, stability, invasiveness etc. Nonetheless, only a cortical implant offers the possibility to detect the entire spectrum of brain activity. Moreover, cortical recordings have been directly linked to biophysics in the brain from which mathematical models related to the origins of the neural signal have been constructed [4].

Neural signals carry information fundamental for the understanding of the brain. For instance, movement [10], sleep [11], speech [12] and aging [13] have been found to correlate to neural signal patterns. They have also been shown to contain information regarding diseases such as epilepsy [14], Parkinson's [15], depression [16] and obsessive-compulsive disorder [17]. Even the understanding of consciousness itself has been under investigation through the analysis of neural signals [18].

1.2.2 Considerations for Neural Recorders

The requirements for neural recording stem from electrode properties, characteristics of the neural signal and implant related needs. Fig. 1.6 shows the requirements of a neural recording front-end.

The initial considerations for the neural recording interface come from electrode impedance (Z_E), electrode mismatch and electrode DC offset (EDO). Electrode impedance depends on electrode material, surface area, frequency and environment [19]. As a rule of thumb, a smaller area implies higher impedance, which in turn implies higher noise [20]. A smaller surface area is necessary for recording of action potentials though, as it translates to higher spatial resolution. This means that the electrode arrays for intracortical recording exhibit the highest impedance out of any other type of implantable electrode

Electrode Parameter	Front-end Specification	
Impedance	Input impedance	> 10 x Z_E
Mismatch	CMRR	> 60 dB
DC Offset	DC rejection mechanism	> ± 50 mV

Neural Signal Property	Front-End Specification	
Magnitude	Low-noise, Gain	< 10 µVrms, > 30 dB
Frequency	Bandwidth	100-500 Hz for LFP 5-10 kHz for AP

Implant Safety/Longevity	Front-end Specification	
Energy efficiency and Heat	Power consumption	< 10 µW
Footprint	Area	< 0.3 mm^2
DC Leakage	Input impedance	> 100 MΩ

Implant Environment	Front-end Specification	
Environmental Interference	CMRR, PSRR	> 60 dB for 100 mVpp

FIGURE 1.6: Requirements for neural recording

array. Z_E in intracortical arrays reaches as high as tens of MΩ at low frequencies. Their surface area is typically ¡ 100 × 100 μm^2. To avoid signal attenuation, the neural recording interface requires an input impedance (Z_{IN}) at least 100 times that of Z_E [20].

The electrode mismatch problem originates from the fact that electrode impedances are not the same due to fabrication non-idealities. This increases the susceptibility of the interface to common-mode interference that can only be counteracted by high common-mode rejection (CMRR) [21].

The EDO is caused by polarization in the electrodes and it can reach tens of mV, which might be enough to saturate the interface. An offset rejection mechanism such as a high-pass filter or DC servo-loop should be employed to deal with this issue [22].

Low-noise is one of the fundamental specifications for the neural interface [23]. It is necessary in order to obtain high signal-to-noise ratio (SNR) considering that the neural signal is on the μV order and the extracellular neural background noise has a noise floor of tens of nV order of magnitude. It is specially important in applications that include detection of oscillations or spikes based on algorithms that rely on a recorded signal with sufficient SNR. High gain is also required in order to relax the noise requirements of subsequent stages.

Bandwidth is an obvious requirement for the interface. As seen in Section 1.2.1, it has been shown that LFPs spread their energy up to 100 - 500 Hz, whereas spikes are present up to 5 - 10 kHz. The choice of bandwidth in the recording interface depends on

the application. Electrode capabilities and power consumption should also inform this decision.

Low power is probably the most important concern in an implant. This preoccupation comes from the fact that the implant must operate at the lowest possible power consumption since its energy source is typically implanted batteries or an energy harvesting scheme. Power consumption is therefore directly related to the longevity of the device. Its status as the most fundamental specification in an implant is increasing even more as the field progresses into more ambitious applications such as all-cortex recording [24]. From this perspective, area is also a fundamental concern, not only with the aim to reduce the footprint of the implant but also its cost.

From a medical safety point of view, low-power consumption is essential as its directly related to the temperature of the implant. It has been shown that neural tissue can be damaged due to excess heat [25]. DC current leakage from the interface inputs into the tissue can also be a source of damage to tissue and electrodes. For instance, intracortical electrodes tolerate a DC current up to 10 nA. [26] recommends at least Z_E= 100 MΩ assuming a worst case DC offset of 50 mV, which would yield an acceptable leakage current of 0.5 nA.

Finally, considerations emerging from large environmental interference should also be accounted for. It has been reported that coupling from the supply voltages generates large common-mode interference [27]. Muscle activity can be a source of interference as well [28]. As a consequence, the interface needs to be designed for common-mode and power-supply rejection of large signals.

It is clear that the design of the neural recording interface represents an unique problem. Achieving these specifications together is a significant challenge, specially considering the existence of several trade-offs among them. It can be said that a proper design involves meeting all of these specifications without significant penalty on each other. Multidisciplinary teams can take advantage of their expertise in areas such as materials science and neuroscience to take the load off the specifications of the recording interface in order to avoid overdesign.

1.3 Neural Stimulation

Neural stimulation involves the delivery of charge to neural tissue for clinical purposes. This section covers the basics and considerations of neural stimulation.

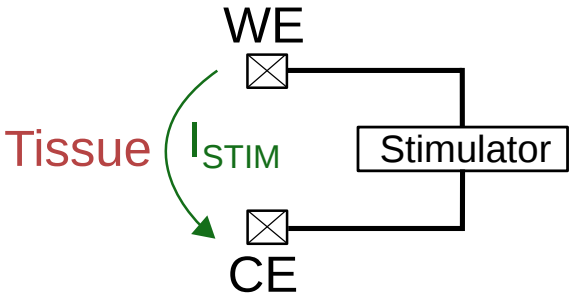

FIGURE 1.7: Basic setup for neural stimulation.

1.3.1 Basic concepts

The process by which neural activity is evoked via electrical stimulus is known as neural stimulation. In order to trigger an action potential an artificial depolarization of neural tissue must take place. This is achieved when the extracellular potential is more negative with respect to the intracellular potential [29]. The most basic setup requires two electrodes located in neural tissue, as shown in Fig. 1.7. Current flows from the working electrode (WE) to the counter electrode (CE) causing a change in the potential at the tissue. A cathodic stimulus wave causes negative charge accumulation under the WE which results in depolarization. Thus, action potentials are evoked away from WE. It is also possible to initiate action potentials by an anodic stimulus wave at the cost of higher amounts of charge.

Charge transfer from the stimulator to the tissue is a phase transition process between electron and ion flow. This occurs as a result of different reactions at the electrode-electrolyte interface [30]. Multiple mechanisms are involved in this process and the predominant one depends on the type of electrode. For instance, platinum electrodes transfer electrons across the electrode-electrolyte interface (faradaic process). This process has been described as a pseudocapacitance [30].

A fundamental issue in stimulation is tissue safety. In general, it is required that the net delivered charge is zero in order to avoid tissue damage. A way to achieve this is with a biphasic waveform comprised by two phases that inject the same amount of current with different polarity [31]. Fig. 1.8 shows traditional stimulation waveforms. The principle behind them is the same: all injected charge must be recovered in order to avoid tissue damage.

From an electrical circuits perspective, there are three different stimulation schemes (Fig. 1.9): voltage-controlled stimulation (VCS), current-controlled stimulation (CCS) and switched-capacitor stimulation (SCS). VCS offers the highest energy efficiency out of them, however, this scheme has no precise control over the injected charge since it

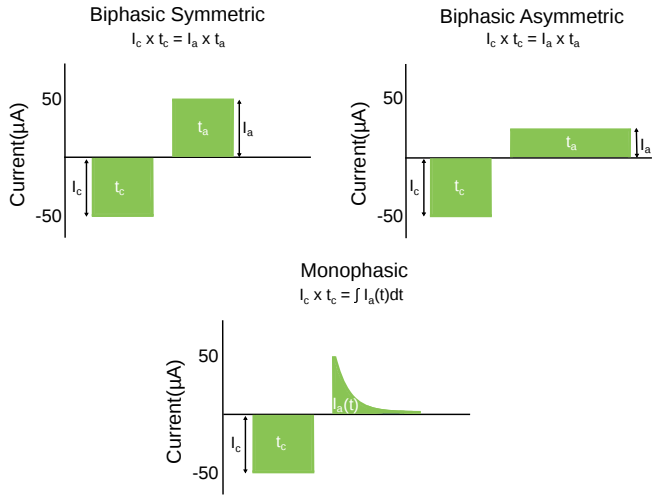

FIGURE 1.8: Waveforms for neural stimulation.

depends entirely on Z_E. In contrast, CCS offers the best control of charge as it is independent on electrode characteristics with minimal efficiency. SCS is a middlepoint between the two: It depends on the electrode characteristics but is bounded by design parameters while its efficiency is limited by the intrinsic loss in the capacitor charging process [32]. From a safety perspective, CCS outperforms every other scheme purely because it does not depend on electrode characteristics. As a consequence, CCS has become the predominant technique in neural stimulators. From here on, all discussion will be assuming current-controlled stimulators.

1.3.2 Considerations for Neural Stimulators

Safety is the utmost concern in a neural stimulator. As stated before, the injected net charge to the tissue must be zero in order to avoid damage. However, due to circuit non-idealities such pretense becomes only an approximation in practice. Nevertheless, chronic neural stimulation can be made viable if safety margins in residual voltage, charge mismatch and DC current error are established. These margins are highly dependent on the electrode type as well as the amount of stimulation current. For example, charge mismatch is a priority in platinum electrodes where the reaction products of the interface can be recovered by a biphasic pulse as they remain on the surface of the electrode [21]. In contrast, residual voltage is the first consideration in electrodes where the reaction products diffuse away from the surface. A voltage safety limit is set in in these cases in order to avoid damage.

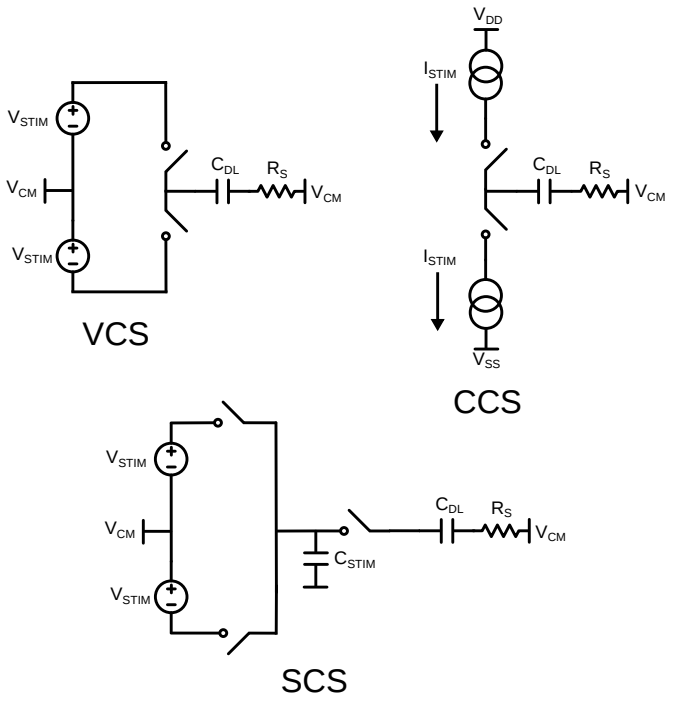

FIGURE 1.9: Electrical stimulation schemes.

Safety Specifications	
Residual Voltage	±100 mV
Charge Mismatch	< 1%
DC Current Error	< 100 nA

Z_E Dependent Specifications	
Voltage Compliance	1.8 V – 9 V
Output Impedance	> 100 MΩ

Programmability	
Current	10 µA – 10 mA
Waveforms	Biphasic, Monophasic, High-frequency pulses

FIGURE 1.10: Requirements for neural stimulation.

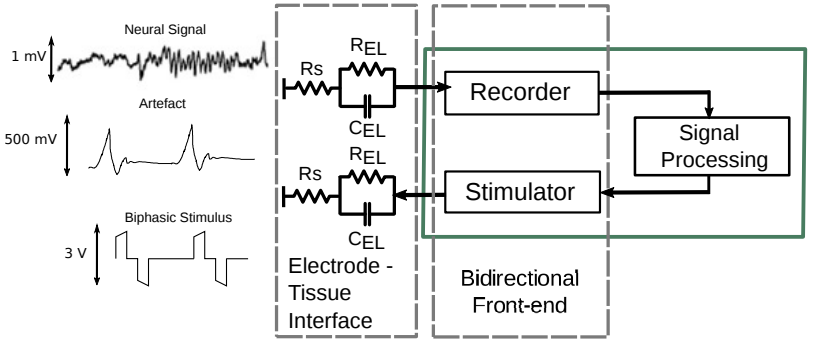

FIGURE 1.11: Bidirectional front-end for closed-loop neuromodulation.

Although CCS is known to be independent of Z_E, this is only achieved if the circuit topology and biasing conditions allows so. This is accomplished by approximating as much as possible the output characteristics of the stimulator to those of an ideal current source. In practice, a constant current can only be kept for a given load as long as there is enough voltage compliance. The same goes for the output impedance of the neural stimulator. The good news is that these specifications are not necessarily hard to meet, as they do not involve any sort of crucial trade-off.

As opposed to neural recording, neural stimulation requires as much flexibility as possible. Not only are patients expected to respond differently from each other to varied forms of neural stimulation but this response would probably change over time. As a result, the amount of injected charge (via current control) should be made programmable. Similarly, the neural stimulator should allow for the programming of different waveforms and their respective characteristics: pulse width, interphase delay, frequency etc.

1.4 Closed-Loop Neuromodulation

Neural recording and neural stimulation come together in a single concept known as closed-loop neurmodulation or closed-loop neurostimulation. The idea behind it is pretty straightforward: to establish closed-loop control of brain activity via stimulation informed by recording. This scheme offers a more efficient use of stimulation in terms of power consumption as the traditional periodic stimulation is replaced by one in which stimulation occurs only when necessary. This is specially important in clinical applications for Parkinson's disease and epilepsy [33]. It is also useful in applications where prosthetics feed information back into the brain via stimulation [34]. In other cases, it enables advanced applications. For example, in brain-spine interfaces the recorder is placed in the cortex and its output is sent to stimulators that bypass a spine injury [35].

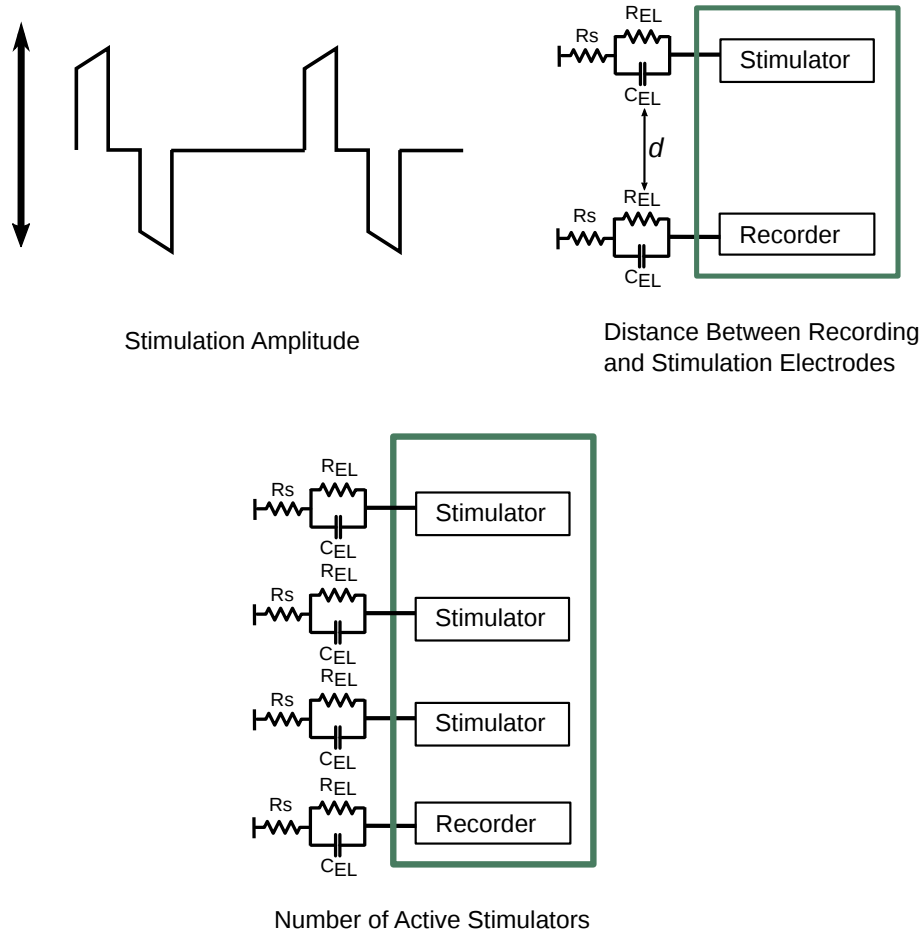

FIGURE 1.12: Factors that contribute to artefacts.

A recording and stimulation interface placed in the same chip for reading and writing purposes can be thought of as a bidirectional front-end. It can therefore be said that a bidirectional front-end is the block in the chip in charge of closed-loop neuromodulation (Fig. 1.11). This is not true for all applications though, such as those where the recorder is far away from the stimulators (i.e. placed on different chips).

1.4.1 Self-Interference

The neuromodulation setup shown in Fig. 1.11 exhibits an inherent self-interference in the form of stimulation artefacts that contaminate the recorded neural signal. Artefacts

present themselves at the inputs of the recording front-end as large ac common-mode interference occurring at the stimulation frequency, which generally falls inside the recording bandwidth. Artefacts are also comprised by a differential component that is caused by path mismatches as well as a ratcheting effect [36]. Their magnitude is proportional to the residual charge in the electrodes [37] after stimulation, which is in turn proportional to the amplitude of the stimulation pulses. Proximity between recording and stimulation electrodes as well as a number of active stimulators are also contributors to the magnitude of artefacts. Even unconnected electrodes are a contributor to artefacts due to accumulated charge caused by current flow between nearby electrodes [38]. The main factors that contribute to artefacts are depicted in Fig. 1.12.

The fact that residual charge in the electrodes from stimulation causes artefacts leads us to consider the design of the stimulator. In a closed-loop neuromodulator, residual voltage in the electrodes takes on an even greater importance. The same can be said of charge mismatch, which is product of unbalanced stimulation pulses and as a consequence, directly proportional to charge drops in the electrodes during stimulation. A properly designed closed-loop neuromodulator should therefore implement design strategies both in the stimulation and recording front-ends in order be able to operate in the presence of self-interference.

1.4.2 Classification

Closed-loop neuromodulators can be classified by the manner in which they are connected to the electrode array. Fig. 1.13 shows these classification. The electrode sharing configuration offers double functionality for each electrode. However, this functionality is not simultaneous due to the large artefact experienced. Indeed, a high-voltage switch is necessary to isolate the recording front-end from the stimulator [39]. The same-electrode array configuration places either a stimulator or a recorders per electrode. This configuration experiences artefacts of a manageable magnitude. As a result, this setup can demonstrate simultaneous recording and stimulation if an appropriate artefact handling scheme is included. Finally, simultaneous recording and stimulation can also be achieved if the recorders and stimulators are placed in different brain regions. This scheme exhibits artefacts of much lower magnitude or no artefact if they are placed in entirely different parts of the nervous system. The result is that the established closed-loop control is between different regions, which is a drawback in most applications.

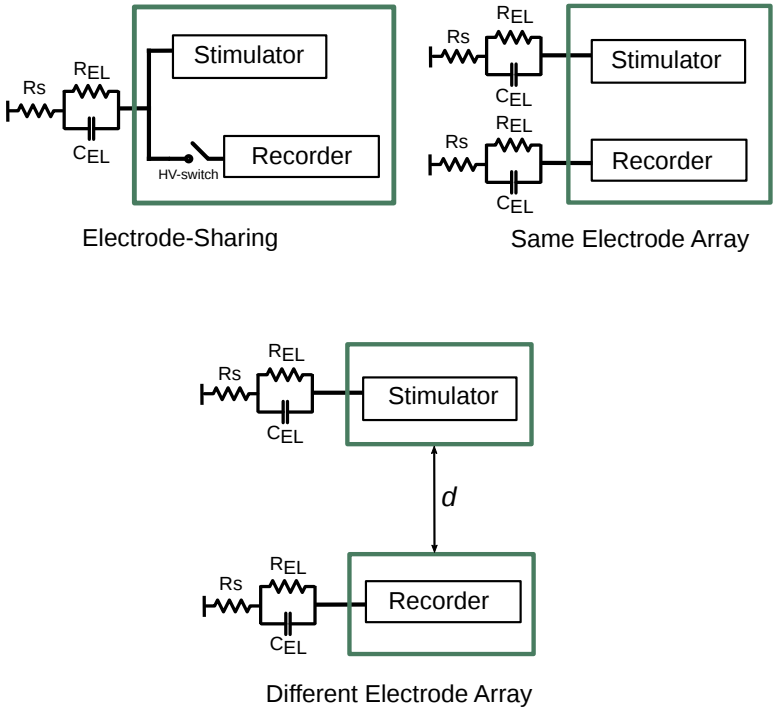

FIGURE 1.13: Classification of closed-loop neuromodulation schemes.

1.5 Contributions of this Work

This work introduces two different contributions to the field of implantable neural interfaces.

The first one is a sub-μW ac-coupled reconfigurable front-end for multichannel invasive wideband neural signal recording. The proposed topology embeds filtering capabilities enabling the selection of different frequency bands inside the neural signal spectrum. Power consumption was optimized by designing for proposed neural signal band-specific noise targets. These noise targets are informed by the spectral characteristics of the wideband neural signal. As seen in subsection 1.2.1, LFPs exhibit $1/f^x$ magnitude scaling while APs shows uniform magnitude across frequency. This work demonstrates how significant power savings are obtained by exploiting the characteristics of the neural signal. The proposed noise targets also take into account electrode noise as well as the spectral distribution of the noise generators in the circuit.

The second contribution is a multichannel bidirectional front-end for closed-loop neuromodulation. The link between stimulation design parameters and artefact magnitude is acknowledged. Stimulation artefacts are reduced by way of a 4-channel H-bridge current

sink sharing stimulator front-end that minimizes residual charge drops in the electrodes via topology-inherent charge balancing. A 4-channel chopper front-end that is capable of multichannel recording in the presence of artefacts is proposed. This is accomplished by making the total common-mode rejection ratio (TCMRR) the centerpiece parameter in the design process. This specification accounts for CMRR degradation due to electrode mismatch in a multichannel recording interface.

Both contributions offer a unique perspective in the design of implantable neural interfaces.

1.6 Thesis Outline

The rest of this thesis is organized as follows. The state of the art is covered in Chapter 2. Chapter 3 introduces the sub-μW ac-coupled reconfigurable front-end for multichannel invasive wideband neural signal recording. Chapter 4 introduces the proposed multichannel bidirectional front-end for closed-loop neuromodulation. The work concludes in Chapter 5.

Chapter 2

Literature Review

This chapter presents a review on the state of the art of implantable neural interfaces. The focus is on power consumption in neural recording front-ends and closed-loop neuromodulators in the same electrode array.

2.1 Power consumption in neural recording front-ends

Recent research in implantable neural front-ends has converged to a set of commonly agreed requirements: an offset-rejection mechanism, low-noise, high input impedance, high gain and minimal area impact. In addition, many front-ends include spectral selectivity, which is normally done by subsequent filter stages either in the digital or analog domain. As explained in Section 1.2.2, power consumption has emerged as the most important concern in neural implants. Research has focused on reducing the front-end consumption since it is typically one of the power-hungrier blocks in an implant.

Wideband neural recording front-ends can be classified as follows: conventional front-ends, front-ends with spectral selectivity and sub-μW front-ends.

2.1.1 Conventional wideband neural front-ends

Conventional wideband neural front-ends are those that achieve a satisfactory trade-off between all specifications while excluding any kind of special functionality.

The authors in [40] proposed a switched-capacitor front-end that obviates the need for pseudoresistors and improves input impedance by employing a small input capacitor. This front-end consumes 22 μW.

[27] introduced and architecture that enhances CMRR for environmental interference. The base amplifier is a simple inverter and implements common-mode feedback through rails. This front-end consumes 3.28 μW.

In [41], a chopper amplifier with digitally assisted offset calibration was introduced. The front-end also includes a gain calibration mechanism as this front-end has an open loop architecture. The power consumption is 9.1 μW including analog to digital conversion.

The authors in [26] proposed a chopper amplifier that features high-dynamic range to amplify stimulation artefacts. It also introduces alternatives to the traditional pseuroresistors as well as novel schemes for input impedance boosting. The power consumption in this work is 2 μW.

[42] introduced a novel stacked current mirror topology. This work improves heavily on the efficiency between power and noise. The power consumption is 4.5 μW.

[28] introduced a DC coupled topology aimed at high CMRR performance. This work shows a power consumption of 28 μW.

2.1.2 Sub-μW neural front-ends

Sub-μW neural front-ends are sparse in the literature and they generally involve the penalization of a non-trivial circuit specification. In other words, the cost of sub-μW operation is the degradation of another circuit specification, often to prohibitive levels.

The low-power consumption in [43] is achieved through the extreme reduction of the supply voltage which comes at the cost of a limited input swing. The input swing of the amplifier is 10 μV without clipping issues.

The front-end introduced by [44] omits large parts of the local field potential spectrum. More specifically, the high-pass corner is 80 Hz. This means that no power is spent on the amelioration of low-frequency noise, which is what enables low-power consumption.

The front-end in [45] omits large parts of the action potential band. This is because the first stage, which is proportional to the bandwidth of the amplifier, is biased with a smaller current than usual. Thus, the recording bandwidth is only 1 kHz.

Single-ended front-ends also manage sub-μW operation [46]. Indeed, single ended topologies are less consuming than their differential counterparts, however, this comes at the cost of insufficient CMRR (=40 dB) and PSRR (=45 dB).

The topology introduced in [47] achieves significant power savings by employing and extremely simple topology. This topology exhibits an inherently prohibitive PSRR= 5.5 dB!

2.1.3 Front-ends with spectral selectivity

Those front-ends that implement some form of spectral selectivity consume over 10 μW. In [48–50], this consumption is to a large extent due to additional analog filter stages.

In [51], the power consumption is produced by a higher than average bandwidth (15 kHz) that ends up impacting its tuning flexibility. Finally, analog to digital conversion integrated directly after the sensing electrodes has been proposed at the cost of a power consumption of 5 μW [52].

2.1.4 NEF and Power consumption

The noise efficiency factor (NEF) was introduced in [53] to codify the efficiency of the design in terms of the relationship between noise and current. The NEF is defined as

$$NEF = V_n\sqrt{\frac{2I}{\pi V_T 4kTBW}}. \tag{2.1}$$

Where V_n is the integrated noise of the front-end, BW is the bandwidth and I is the supply current. Fig. 2.1 shows a plot of the previously discussed works. The group in orange is clearly favorable in terms of power consumption, however as noted in Section 2.1.2, this performance comes at the cost of the penalization of some other specification.

2.2 Same Electrode Array Closed-loop neuromodulators

As stated in Section 1.4.1, a bidirectional interface connected to the same electrode array exhibits self-interference that should be managed in some form. Traditional designs of closed-loop neuromodulators involve the unilateral placement of stimulators alongside recording amplifiers with minimal to no regard for self-interference [54–59]. As a consequence, these prototypes are unable to record during stimulation as their front-ends saturate due to artefacts.

Commercial neuromodulators work around this issue by limiting the bandwidth of the amplifiers to 100 - 200 Hz [60–63]. This strategy is somewhat successful since stimulation frequencies are typically chosen at ¿ 200 Hz. However, this impedes the recording of

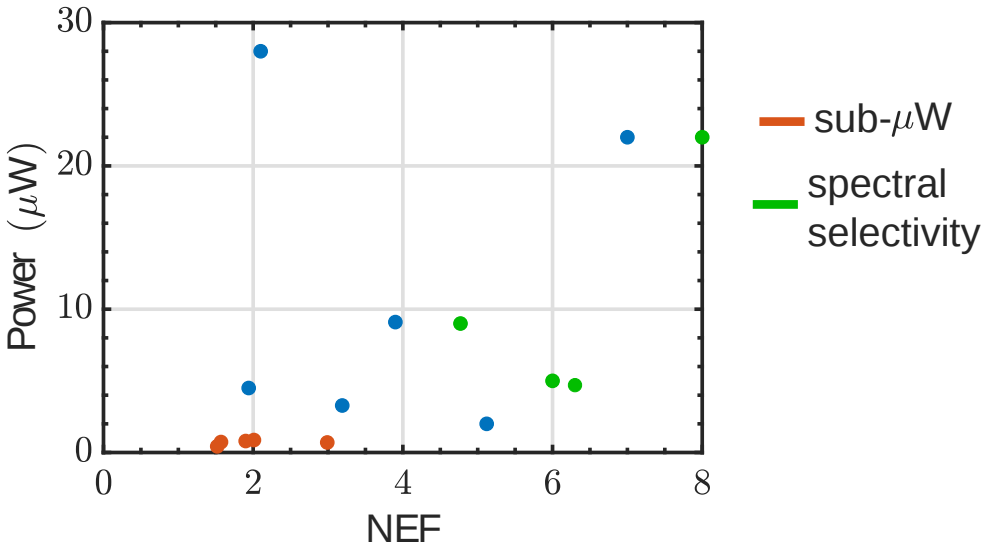

FIGURE 2.1: Power consumption vs NEF of recording front-ends.

high frequency biomarkers. For example, it has been shown that the 250 - 600 Hz band contains biomarkers for epilepsy [64] or Parkinson's [65].

The work introduced by [66] employs input blanking in order to avoid saturation. This consists in shutting down the inputs of the recording front-end during stimulation. A different technique known as frequency pole shifting was employed in [49]. This boils down to a change in the frequency response of the recording front-end during stimulation in order filter the artefacts. In [67] a technique that forces a fast recovery was introduced. This is achieved by setting the output of the front-end to a reference voltage to recover its functionality immediately after stimulation. Although these works are successful in dealing with self-interference, they entail loss of information during stimulation as they are not capable of recording in the presence of artefacts.

As explained in Section 1.4.1, artefacts stem from residual charge drops in the electrodes due to stimulation pulses. This suggests that artefacts should be accounted for in the design of the neural stimulator as well. In the literature only [37, 63, 68] consider the role of artefacts at their origin. These works minimize artefacts through charge balance schemes in the stimulator.

Recent works have demonstrated tolerance to self-interference, still, they are not without issues. For instance, [69] is vulnerable to large common-mode interference, mostly due to the low supply voltage in the input stage. [70] employs a passive high-pass filter prior

TABLE 2.1: State of the art of closed-loop neuromodulators

	[49]	[63] [71]	[69]	[70]	[68, 72]	[67]
Year	2016	2018	2018	2018	2019	2019
Process (nm)	180	800 HV, 250	65	40,180 HV	180 HV	130
Channels Rec. / Stim.	16 / 16	4 / 16	64 / 16	64 / 8	64 / 4	32 / 4
BW (Hz)	7k	-	8.3 k	250	500	15k
Noise	4.57 μVrms	100 nV/rtHz	8.2 μVrms	2.2 μVrms	68 nV/rtHz	3 μVrms
Input	-61dB THD for 10mVpp	-	77dB DR for 200mVpp	81dB SFDR for 100mVpp	0.012% THD for 100mVpp	-
CMRR (dB)	81 unspecified	¿80 unspecified	12 for 100 mVpp	-	85 unspecified	-
Self-interference strategy	input blanking tunable high-pass filter	input blanking tunable low-pass filter high-dynamic range charge-balance	analog/digital canceller	high dynamic range	digital canceller high-dynamic range charge-balance	fast recovery

to the recording front-end which substantially degrades the CMRR while [68] features a front-end with insufficient input impedance.

From this literature overview, it can be concluded that the field is leaning towards achieving simultaneous recording and stimulation. Thus, an artefact-aware design of the neuromodulator has become a fundamental necessity. The current state of the art in closed-loop neuromodulation front-ends is shown in Table 2.1.

Chapter 3

A Sub-μW Reconfigurable Front-End for Invasive Neural Recording that Exploits the Spectral Characteristics of the Wideband Neural Signal

This chapter introduces a front-end with reconfigurability that enables spectral selectivity. The idea was to produce a design that met the following conditions:

- Operation at state of the art sub-μW power consumption.
- Included bandwidth selectivity functionality that is only available at high (¿ 10 μW) power consumption.
- Did not compromise any other specification, thus achieving a satisfactory trade-off among all specifications as in conventional front-ends.

The following discussion covers the design of such front-end.

3.1 Introduction

The proposed two-fold strategy for power reduction is as follows: first, instead of including additional filters, filtering capabilities are embedded in the front-end. This is made

possible by introducing a reconfigurable topology that produces different frequency responses in the same circuit. Second, a power-efficient low-noise design based on multiple noise targets that depend on the type of neural signal is derived. This strategy takes the place of the traditional single integrated noise target for the entire neural bandwidth. The proposed noise targets are motivated by three main factors: 1) the bandwidths of the noise generators in the front-end, 2) electrode noise distribution, and more importantly, 3) the spectral characteristics of the neural signal. It has been shown that LFPs, extended to the HFO frequency range, exhibit a $1/f^x$ magnitude scaling [73, 74] while APs show an uniform magnitude [7]. A spot-noise target at the worst case signal-to-noise ratio (SNR) is thus chosen for the low-frequency band [75] while the integrated noise specification is kept for higher frequencies. This strategy translates directly to power savings since the chosen spot-noise target is located at a frequency after the front-end's noise corner. At this frequency, the noise floor is mostly thermal and can be efficiently controlled by the bias currents in the front-end without needing to compensate for low-frequency noise contributions. Furthermore, since the power consumption is not dependent on the topology, other fundamental specifications such as input swing, PSRR or CMRR are not impacted. The basics of this work were originally introduced in [76].

3.2 Proposed reconfigurable front-end

Figure 3.1 shows the proposed capacitively-coupled wideband neural front-end with reconfigurable topology. The idea is that four different front-end configurations (modes), each with its own frequency bandwidth, can be accessed through digitally-controlled switching. Thus, the front-end can be tuned to a specific frequency band inside the neural signal spectrum with no impact on power consumption. The configuration modes are named after the bandwidth they are set to: wideband (WB) neural signal, LFP, AP and Fast Ripple (FR). The fast ripple is a form of high-frequency oscillation that rides LFPs and appears above 100 Hz and extends up to 1 kHz [77].

The front-end is comprised by two OTAs in the forward path and one in the feedback loop. OTA_1 provides the first stage of amplification and sets the thermal noise floor of the circuit. OTA_2 acts as a low-pass filter [78] with a switchable high-frequency corner (f_H) [43]. OTA_3 is an active feedback that biases the inputs of OTA_1 and generates a switchable low-frequency corner (f_L) [79]. This corner is fundamental in biological front-ends for electrode offset rejection and in this case, filters low-frequency noise in the AP and FR modes. The use of pseudoresistors has been avoided since it has been suggested that they exhibit much larger variability than active feedback [80]. The employed active feedback thus allows for more robust topology reconfigurability and avoids the need

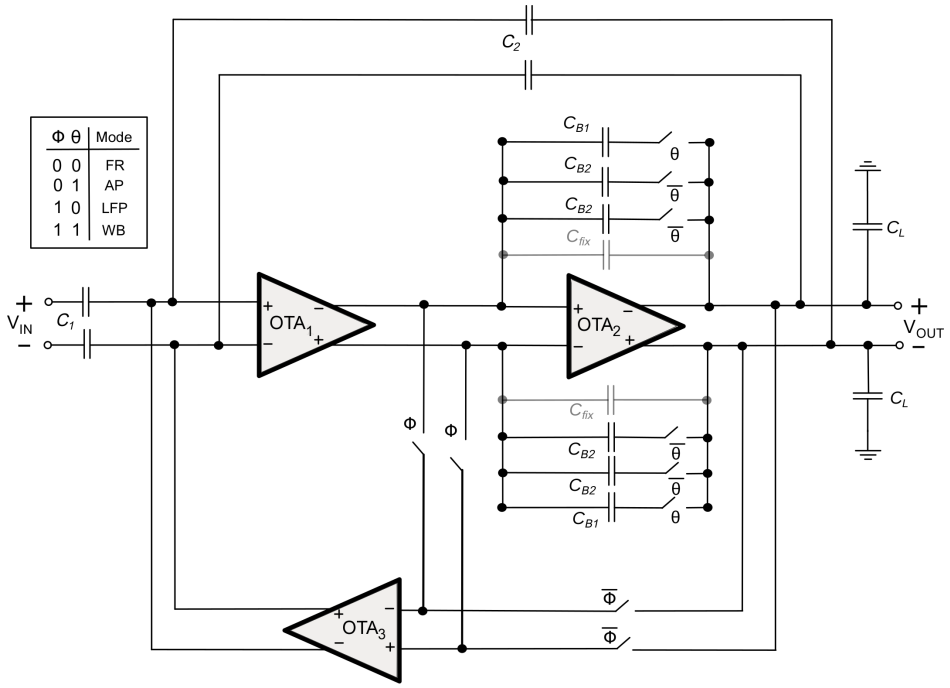

FIGURE 3.1: Proposed reconfigurable front-end

for external pseudoresistor tuning. The gain for all modes of operation is defined by capacitor ratio C_1/C_2. The reconfigurable modes are as follows.

3.2.1 Wideband Mode

The circuit enters the WB mode that covers both the local field and action potential frequency bands (Fig. 3.2(a)) at $\phi = 1$ and $\theta = 1$. The low-frequency corner is given by:

$$f_{L(WB)} \simeq \frac{gm_3}{2\pi C_2 A_2}. \tag{3.1}$$

Here, $A_2 = gm_2/gds_2$[81] while gm_2 and gds_2 are the transconductance and conductance of OTA_2, respectively; gm_3 is the transconductance of OTA_3. The high-frequency corner is:

$$f_{H(WB)} \simeq \frac{gm_1 C_2}{2\pi C_{B1} C_1}, \tag{3.2}$$

where gm_1 is the transconductance of OTA_1.

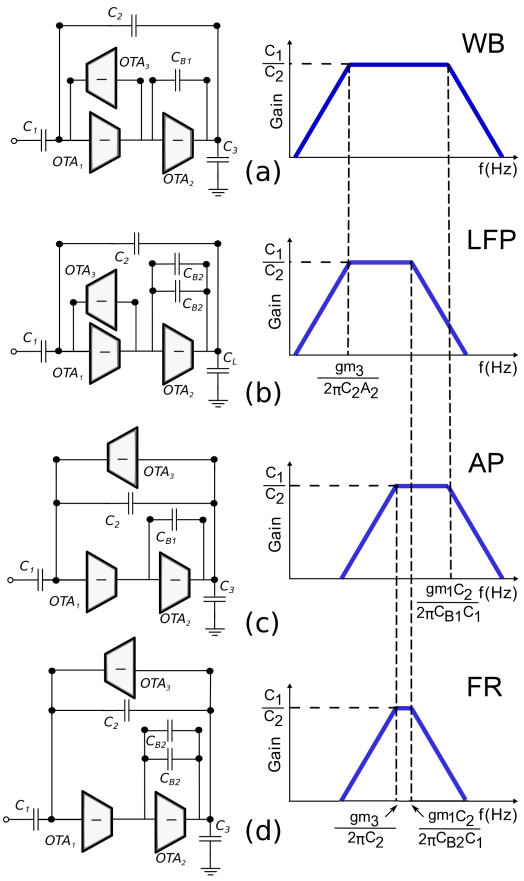

FIGURE 3.2: Reconfigurable Modes. (a) Wideband mode (b) Local field potential mode (c) Action potential mode (d)Fast ripples mode.

3.2.2 Local Field Potential Mode

The LFP mode of operation is accessed at $\phi = 1$ and $\theta = 0$ (Fig. 3.2(b)). The low-frequency corner $f_{L(LFP)}$ is the same as the WB mode. The high-frequency corner is given by:

$$f_{H(LFP)} \simeq \frac{gm_1 C_2}{2\pi C_{B2} C_1}. \tag{3.3}$$

Thus, the bandwidth is reduced considering $C_{B2} > C_{B1}$.

3.2.3 Action Potential Mode

The AP mode (Fig. 3.2(c)) reconfigures the feedback of the circuit at $\phi = 0$ and $\theta = 1$ meaning that OTA_3 connects to the output of OTA_2. This has the following effect on the low-frequency corner:

$$f_{L(AP)} \simeq \frac{gm_3}{2\pi C_2}. \tag{3.4}$$

Equation (3.4) shows that by discarding A_2, this corner is boosted to a higher frequency. The high-frequency corner $f_{H(AP)}$ is described by (3.2) as well, since C_{B1} is set as the feedback capacitor.

3.2.4 Fast Ripple Mode

The amplifier enters FR mode (Fig. 3.2(d)) at $\phi = 0$ and $\theta = 0$. The bandwidth is set by a combination of $f_{L(AP)}$ and $f_{H(LFP)}$ corner. The low-frequency corner $f_{L(FR)}$ is thus described by (3.4) while (3.3) describes the high-frequency corner $f_{H(FR)}$.

3.3 Power-efficient low-noise design for neural signals

This section presents the proposed noise targets for the reconfigurable front-end. These targets are independent from the proposed topology and can be employed in other wideband neural front-ends. The main idea is that a power efficient design can be achieved if the spectral characteristics of front-end noise, the input neural signal and electrode noise are taken into account.

3.3.1 Noise analysis

Total noise in the front-end can be approximated by summing the contributions generated by OTA_1 and OTA_3. The noise contribution of OTA_2 is negligible since the first stage is designed for high gain. For the most part, reported neural front-ends also omit the noise contribution by the feedback element (OTA_3 in this case). The commonly used feedback pseudoresistor is sized as large as possible to push the f_L far enough from the bandwidth of interest so that its noise contribution is minimized. This comes at the cost of a larger OTA_1 flicker noise contribution which is partially counteracted by a large differential pair area (or chopper modulation if the noise requirement is too stringent). This strategy is understandable if the circuit is designed under an integrated noise specification. In our case, the feedback element will be accounted for in the analysis in order

to visualize its frequency-dependent impact on the front-end. This will lead us to the generation of power-efficient noise targets that will be introduced in later sections. The following noise analysis is valid for every reconfigurable mode.

For noise analysis OTA_1 and OTA_3 are assumed as single transistors operating in sub-threshold region. The idea is to employ simple noise terms defined by bias currents (I_B) and areas ($W \times L$) that can be linked to any other OTA topology with the addition of a few proportional factors. The open-loop noise related to OTA_1 ($\overline{v_{n,1}^2}$) is comprised by thermal ($\overline{v_{n,th,1}^2}$) and flicker noise ($\overline{v_{n,1/f,1}^2}$) contributions. The thermal component is defined as:

$$\overline{v_{n,th,1}^2} = \frac{4kT\gamma\eta V_t}{I_{B1}}\Delta f, \tag{3.5}$$

where k is the Boltzmann constant and T is the temperature. The process parameters η and V_t describe the sub-threshold slope and thermal voltage respectively, while γ=1/2 in the sub-threshold region. I_{B1} is the current flowing through OTA_1. The flicker component is given by:

$$\overline{v_{n,1/f,1}^2} = \frac{K_F}{W_1 L_1 C_{ox} f}\Delta f, \tag{3.6}$$

where K_F is a process dependent parameter, C_{ox} is the gate oxide capacitance and W_1 and L_1 are the width and length of OTA_1. $v_{n,1}^2$ can then be referred to the input of the front-end by way of:

$$\overline{IRN_1^2} = v_{n,1}^2\left(\frac{C_1 + C_2 + C_{IN}}{C_1}\right)^2 \Delta f, \tag{3.7}$$

where C_{IN} is the input parasitic capacitance of the transconductor and Δf is approximated to $(\pi/2)f_H$. A similar procedure can be deployed for OTA_3. Considering that OTA_3 needs to be biased by a very low current in order to set f_L, the thermal noise contribution will be predominant over the flicker one [82]. As a result, noise in OTA_3 ($\overline{v_{n,3}^2}$) can be approximated as follows:

$$\overline{v_{n,th,3}^2} = \frac{4kT\gamma\eta Vt}{I_{B3}}\Delta f, \tag{3.8}$$

where I_{B3} is the current flowing through OTA_3. The input-referred noise of OTA_3 is:

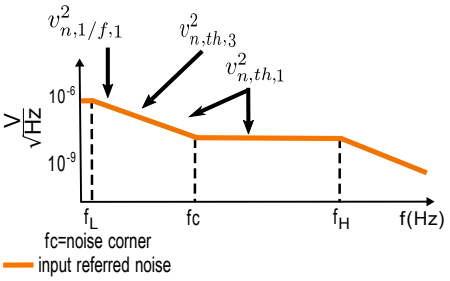

FIGURE 3.3: Input referred noise of the proposed front-end.

$$\overline{IRN_3^2} = \overline{v_{n,3}^2}\left(\frac{1}{G}\right)^2\left|\frac{1}{1+j(f/f_L)}\right|^2. \tag{3.9}$$

where $G = C_1/C_2$ in the AP and FR modes and $G = C_1/C_2A_2$ in the WB and LFP modes. The two noise generators can be summed to obtain the total input-referred noise as follows:

$$\overline{IRN_{Total}^2} = \overline{IRN_1^2} + \overline{IRN_3^2}. \tag{3.10}$$

Fig. 3.3 shows a sketch of (3.10). The noise at lower frequencies (i.e. the LFP band) is mostly $v^2_{n,1/f,1}$ and $v^2_{n,th,3}$, while $v^2_{n,th,1}$ dominates at higher frequencies (i.e. the AP band). At lower frequencies, $v^2_{n,th,3}$ masks $v^2_{n,1/f,1}$ due to the use of an active feedback. This effect causes a deviation from a $1/f$ slope in the front-end's noise [23] and is exacerbated in the WB and LFP modes (see Appendix A).

The main implication in the noise analysis is that, for a fixed gain, the only circuit parameters through which a particular noise target can be reached are I_{B3}, W_1, L_1 and I_{B1}. Moreover, the first three parameters cannot be adjusted unilaterally since $I_{B3} = gm_3/\eta Vt$, which is directly related to f_L by way of (3.1) and (3.4); while W_1 and L_1 heavily impact the area of the circuit and cause a potential gain drop due to C_{IN} loading. Thus, the only parameter left is I_{B1} which necessarily compensates for $v^2_{n,1/f,1}$ and $v^2_{n,th,3}$ if an integrated noise target covering the entire front-end bandwidth is used. As a result, the traditional design strategy inevitably leads to inefficient power consumption considering that I_{B1} is the largest current in the front-end. Therefore, the ideal noise efficiency factor (NEF) [53] can never be reached, especially in limited bandwidth front-ends where NEF>3 [83] even with chopper modulation schemes [78].

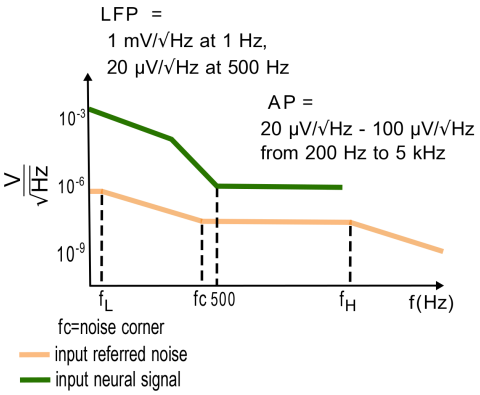

FIGURE 3.4: Spectral characteristic of the wideband neural signal.

3.3.2 Spectral density of neural signals

Traditionally, neural front-ends are designed without any knowledge of the frequency characteristics of the input signal. Doing so necessarily leads to design the front-end under an integrated noise target since the input wideband neural signal is considered only in the time domain. However, research in neuroscience has shed light on previously underexplored details of neural signals that must be considered in the design of neural front-ends. On the one hand, it has been shown in Chapter 1 that the LFP obeys a power law up to 500 Hz. More specifically, the LFP takes a $1/f^2$ form for f¡80 Hz and transitions beyond it to a $\sim 1/f^4$ form. On the other hand, the AP signal displays statistics that translate as a white power spectrum. This characteristic is illustrated in Fig. 3.4 and placed in the context of the front-end's input-referred noise spectrum developed in the previous subsection. The neural signal exhibits higher magnitude at low frequencies where the noise in the front-end is higher while it reaches a flat power spectrum after the front-end's noise corner. As a consequence, the SNR is higher at low frequencies.

The spectral characteristics of neural signals have been exploited in few works. In [84] the authors place a low-frequency corner at a much larger value than usual (f_L ∼100Hz) that flattens the LFP power spectrum before further processing. [40] implements the same concept with a switched-capacitor front-end to avoid some of the pitfalls of the previous implementation. In [75], the authors present an electrocorticography (ECoG) front-end that is designed under a spot-noise specification. The signal is then high-passed to reduce the required analog-to-digital converter (ADC) resolution. Similarly, [85][86] take advantage of the low-frequency slope by performing delta-conversion.

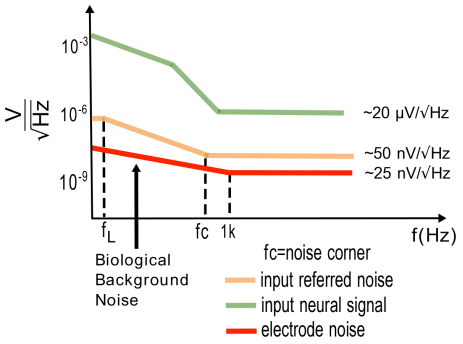

FIGURE 3.5: Noise density of an utah electrode array measured in-vivo (from [19]).

3.3.3 Electrode noise density

Full characterization of microelectrode arrays has become recently available in the literature [87] [19]. In these works the authors characterize multiple sets of microelectrodes both in-vitro and in-vivo and end up reaching some key findings in common: electrode noise is higher in-vivo than in-vitro and it increases significantly at lower frequencies due to background noise. The spectrum for a sputtered iridium oxide film (SIROF) Utah Electrode Array (UEA) measured in-vivo is plotted in Fig. 3.5 with the previously discussed PSDs as a backdrop. Electrode noise is flat for high frequencies but at ¡ 1 kHz picks up background noise from far-apart neural activity [88]. This is an interesting result since background noise is usually quoted at 10 μVrms [89] [22] with no regard for its spectral density. More importantly, the convention is to design for an integrated noise target below the background and electrode noise [26], however, since even the in-vivo noise density (noise floor at 25 nV/$\sqrt{\text{Hz}}$ or 7.5 μVrms from 100 to 150 kHz [19]) is lower than common estimates, actually reaching that target would require significant amounts of power consumption. For instance, the work presented in [89] features a noise floor at 21 nV/$\sqrt{\text{Hz}}$ which requires a supply current of 16 μA.

3.3.4 Proposed noise targets

Fig. 3.6(a) shows the noise model that includes the observations made in the previous subsections. V_A is the amplifier noise magnitude, V_S is the magnitude of the input neural signal and V_E models the electrode thermal noise and the background contribution. The core of the proposed design strategy is to consider a spot noise target at the frequency where the input signal abandons its $1/f^x$ decay and reaches its lowest magnitude (∼500 Hz). This frequency can be considered the worst case SNR. Setting the front-end noise at it guarantees an accurate recording at lower frequencies where the SNR is always higher. Power consumption reduction is obtained as a direct consequence since I_{B1}

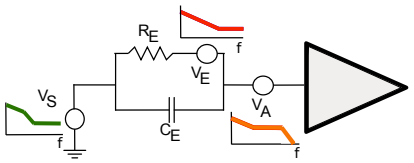

FIGURE 3.6: Noise model of the front-end and electrode interface. R_E is the metal-electrolyte leakage resistor and C_E is the electric double layer capacitor. The model is valid under the assumption that the input impedance of the front-end is several times larger than the electrode impedance.

needs to compensate for lower amounts of $v^2_{n,1/f,1}$ and $v^2_{n,3}$ at 500 Hz meaning it has a more efficient control over the noise floor. The targeted sub-μW operation can therefore be reached without penalizing other characteristics of the front-end. The proposed spot noise target also obviates the need for low-frequency noise removal by way of chopper modulation which brings about a degradation in other specifications such as input impedance and electrode offset rejection that require additional circuitry to compensate for. The proposed design strategy can be generalized to capacitively coupled front-ends with highly resistive feedback elements.

Quantitatively, the spot noise target can be estimated according to the SNR requirements as follows [90]:

$$SNR_{spot} = \frac{V_S}{\sqrt{\frac{V_E^2}{2} + V_A^2}}. \tag{3.11}$$

For an SNR_{spot}¿40 dB at 500 Hz target, a spot-noise target of at least 80 $\text{nV}/\sqrt{\text{Hz}}$ is required in the LFP and WB modes assuming a V_S=20 $\mu\text{V}/\sqrt{\text{Hz}}$ signal and in-vivo electrode noise V_E=25 $\text{nV}/\sqrt{\text{Hz}}$. In addition, a worst case (spatially far-apart) 1 $\mu\text{V}/\sqrt{\text{Hz}}$ LFP can be recorded with at least SNR_{spot}¿20 dB at the proposed noise target.

A spot-noise target at 150 Hz was considered by [75] for an ECoG front-end. This idea can be exploited further in this front-end since it is focused on intracortical signals that are larger in magnitude, hence, allowing for an even greater power reduction. Moreover, [75] made no consideration for the electrode noise in their SNR calculations. The spot noise target is useful for the LFP and WB modes of operation since they cover the frequency band where the input signal maintains a $1/\text{f}^{\text{x}}$ characteristic. The AP and FR modes should keep the traditional integrated noise target since in those frequency bands the input signal is mostly white. As a result, the noise target for these modes is ¡ 5 μVrms. The proposed noise target requirements are shown in Fig. 3.6(b).

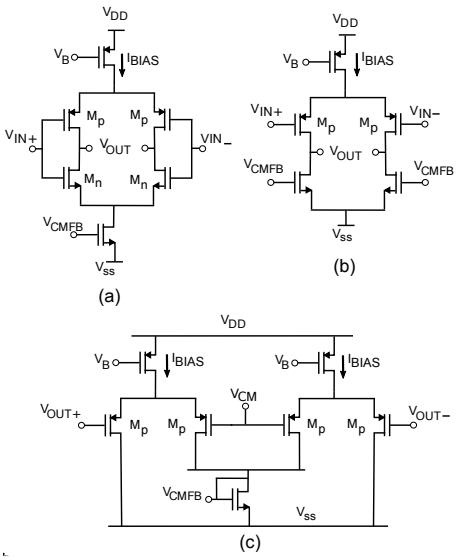

FIGURE 3.7: (a) OTA_1 and OTA_2. (b) OTA_3 (c) Common mode feedback.

It should be said that the $1/f^x$ slope might collapse in some situations [91]. This would effectively cause the low-frequency neural signal to momentarily exhibit a flat PSD, leading to SNR reduction under the proposed design strategy. Considering a worst case low-frequency magnitude at V_S=50 $\mu V/\sqrt{Hz}$, electrode noise at V_E=1 $\mu V/\sqrt{Hz}$ and front-end noise at V_A=5 $\mu V/\sqrt{Hz}$, the recording would show an SNR_{spot}=20 dB. Another aspect to be considered is that the slope in the input neural signal might vary depending on the electrode type [74]. In this case, the proposed design strategy can be modified by choosing a different worst case SNR frequency. The electrode setup also influences the slope of the neural signal. It has been shown that using a single electrode reference enhances the $1/f^x$ slope, thus favoring the application of the proposed design strategy [92].

3.4 Transistor level implementation

Current reuse amplifiers biased in weak inversion were used for OTA_1 and OTA_2 (Fig. 3.7(a)). These OTAs generate the transconductance of a complementary input pair from half the current as they are biased by the same source. Thermal noise for the current reuse amplifier is defined as follows:

$$\overline{v_{n,th}^2} = \frac{16}{3}\frac{kT}{gm_n + gm_p}\Delta f, \tag{3.12}$$

where gm_n (gm_p) is the transconductance of the N (P) input transistor and $gm_n{=}gm_p{=}\frac{I_{BIAS}}{2\eta V_t}$. In the case of OTA$_1$, I_{BIAS} is equivalent to the transconductor bias current I_{B1} described in (3.5). As a consequence, I_{BIAS} sets the noise floor of the front-end at the worst case SNR frequency.

Flicker noise in the current reuse amplifier is:

$$\overline{v_{n,1/f}^2} = \frac{1}{4C_{ox}\Delta f}\left(\frac{K_n}{A_n} + \frac{K_p}{A_p}\right). \tag{3.13}$$

Here, A_n and A_p are the areas of the input n and p transistors, respectively. For OTA$_1$, these areas are directly related to the $W_1 \times L_1$ area described by (3.6). Thus, flicker noise in the front-end is minimized by increasing the input transistor area. The idea is to reduce flicker impact at the worst case SNR frequency to make valid the assumptions of the previous section. Total power consumption is kept low by biasing OTA$_2$ with the least amount of current possible while keeping stability and high enough open-loop gain. Its impact on (3.1) should also be considered. Capacitors C_{B1} and C_{B2} are sized according to (3.2) and (3.3), respectively. OTA$_3$ (Fig. 3.7(b)) is biased with a current in the order of picoamperes and sized with large transistors in order to set $f_{L(WB)}{=}$ $f_{L(LFP)}{=}$ 1 Hz. The common-mode feedback circuit used for every OTA is shown in Fig. 3.7(c). The sizing of C_1/C_2 should consider the gain target (40 dB) and its impact on area and input impedance ($Z_{IN}{=}\frac{1}{j2\pi f C_1}$). A ratio of 28 pF / 255 fF was chosen to counter a plausible process variation induced gain drop. The possibility to fine-tune f_L via external control of I_{B3} was included. This procedure only represents a few nW increase in power consumption. Table 3.1 shows relevant sizing information and Table 3.2 shows the simulated power consumption.

3.5 Measurements

The front-end was designed in a standard 180 nm process. It occupies a non-optimized area of 0.192 mm^2 (Fig 3.8). The relatively large area is due to the capacitors that enable reconfigurability. It is nevertheless on range with other front-ends with spectral selectivity. The area can be reduced by placing the active circuits underneath the capacitors. This would significantly improve the prospects of the circuit for multichannel implementation. The following measurements were performed at 1 V supply.

TABLE 3.1: Sizing information.

Device	**Size**
$M_P(OTA_1)$	300/4 μm
$M_N(OTA_1)$	200/4 μm
$M_P(OTA_2)$	210/0.5 μm
$M_N(OTA_2)$	70/0.5 μm
$M_P(OTA_3)$	38/31 μm
C_1	28 pF
C_2	255 fF
C_{B1}	2 pF
C_{B2}	20 pF
C_L	2.5 pF

TABLE 3.2: Simulated power consumption at V_{DD}=1 V.

Current	**Value (nA)**
$\mathbf{I_{BIAS}}(OTA_1/CMFB_1)$	424 / 140
$\mathbf{I_{BIAS}}(OTA_2/CMFB_2)$	47 / 26
$\mathbf{I_{BIAS}}(OTA_3/CMFB_3)$ (WB,LFP)	0.004 / 0.323
$\mathbf{I_{BIAS}}(OTA_3/CMFB_3)$ (AP,FR)	0.026 / 2
Overall (WB,LFP) / (AP,FR)	803.7 / 807

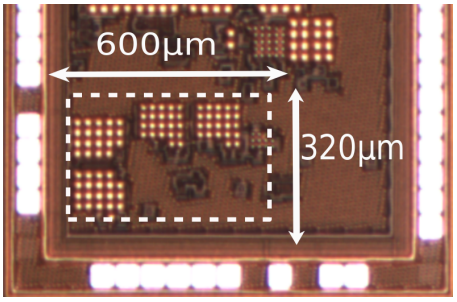

FIGURE 3.8: Die micrograph of the proposed front-end.

3.5.1 Electrical measurements

Results from electrical verification are presented in this section. Measured power consumption was 803 nW in LFP and WB modes and 815 nW in AP and FR modes, which is on range with the expected variation. The four selectable bandwidths are shown in Fig. 3.9. The WB mode covers the 1 Hz - 5 kHz band, AP mode covers 200 Hz - 5 kHz, LFP mode 1 Hz - 700 Hz and the FR 200 Hz - 950 Hz. The input-referred spot noise at 500 Hz is 75 nV/$\sqrt{\text{Hz}}$ (Fig. 3.10(a)) in WB mode and 55 nV/$\sqrt{\text{Hz}}$ in LFP mode (Fig. 3.10(b)). The integrated noise in AP mode is 4.1 μVrms (Fig. 3.11(a)). The integrated noise in FR mode is 2.8 μVrms (Fig. 3.11(b)). CMRR and PSRR were measured for large inputs to account for environmental interference that is present during real-world neural recording scenarios [27, 28]. The measured CMRR for 100 mVpp sine inputs at 50 Hz in LFP and WB modes was 58 dB. This test was repeated at 400 Hz and 1 kHz in FR and AP modes respectively yielding 68 dB in both cases. PSRR was measured by introducing a 100 mVpp sinusoid to the supply input. The measured PSRR was 54 dB at WB and LFP modes at 50 Hz. This same test revealed that the PSRR in AP and FR modes was 64 dB at 1kHz and 65 dB at 400 Hz, respectively. The total harmonic distortion (THD) was found to be ¡1 % for a 1 mVp input for all modes of operation.

3.5.2 In-vitro measurements

The front-end was tested in an emulated real-world environment by means of a prerecorded neural signal loaded to an arbitrary function generator that was injected into a beaker filled with phosphate-buffered saline (PBS). The signal was sensed via titanium nitride surface microelectrodes connected to the chip inputs. The chip was powered by a battery to minimize the impact of power-line interference. The idea was, then, to visualize the raw outputs of the front-end at all operation modes in the time domain for the same neural signal. The output of the front-end in WB mode (Fig. 3.13(a)) shows a number of high-frequency components riding a 1 mVpp local field potential. In

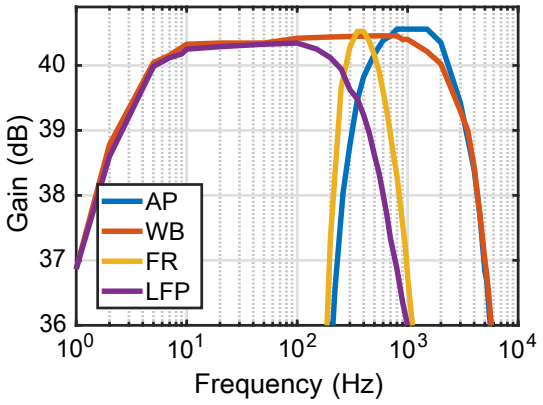

FIGURE 3.9: Frequency Response.

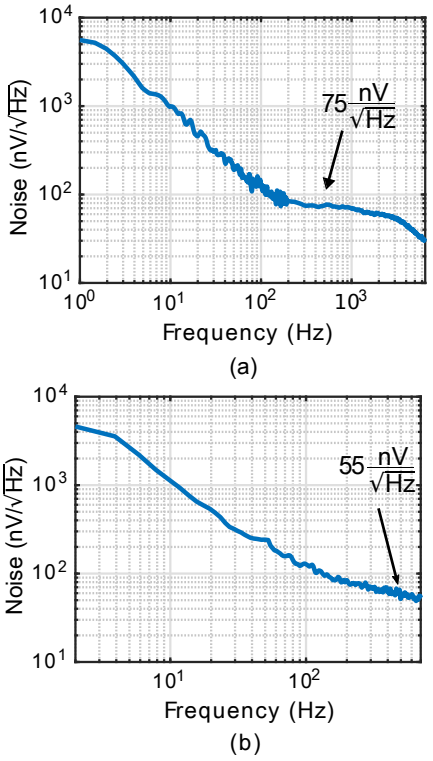

FIGURE 3.10: Input referred noise in WB (a) and LFP (b) mode.

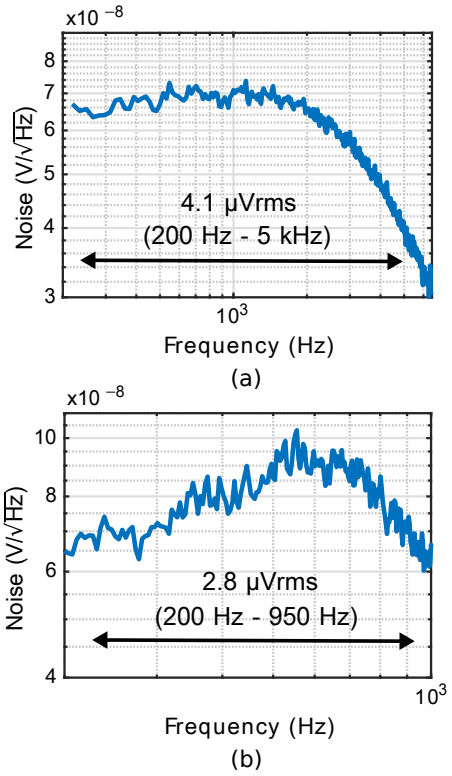

FIGURE 3.11: Input referred noise in AP (a) and FR (b) mode.

contrast, the output in LFP mode (Fig. 3.13(b)) shows a cleaner signal since these high frequency components have been filtered off. Dashed boxes indicate the presence of large high-frequency components in the WB mode that are not present in the LFP mode. A noticeable qualitative change in the neural signal is seen in the AP (Fig. 3.14(a)) mode where the peak-to-peak amplitude drops to that of the action potential after filtering away the much larger in magnitude local field potential. A similar situation was seen in FR mode (Fig. 3.14(b)).

3.5.3 Comparison with previous work

The specifications are summarized in Table 3.3 and compared with the state of the art. This front-end improves by almost an order of magnitude the lowest reported power consumption while keeping comparable performance in all specifications. This work is also the first one to include an specific bandwidth for the observation of fast-ripples. Table 3.4 shows a comparison against reported sub-μW front-ends. In terms of power consumption, this front-end performs on range with the state of the art. However, this work does not incur in any major trade-off such as a degraded CMRR [46] or PSRR [47],

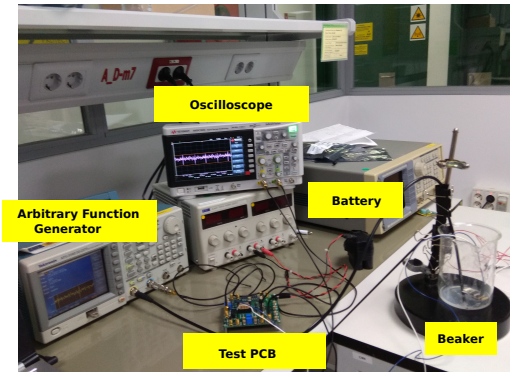

FIGURE 3.12: In vitro test setup.

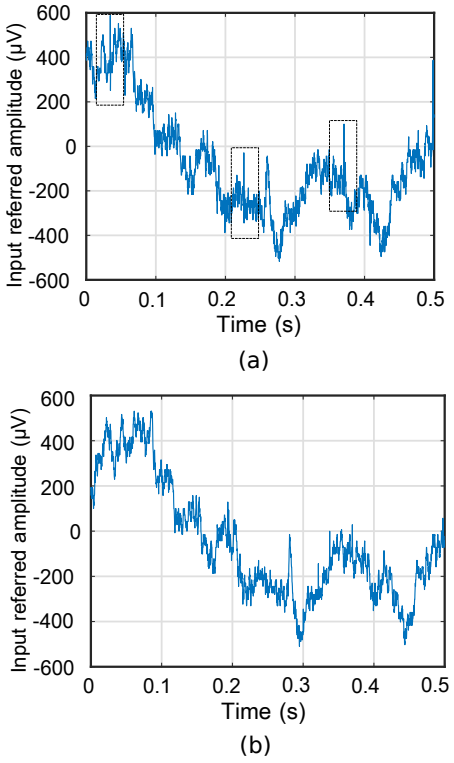

FIGURE 3.13: In-vitro measurements in the WB (a) and LFP (b) modes for a prerecorded neural signal.

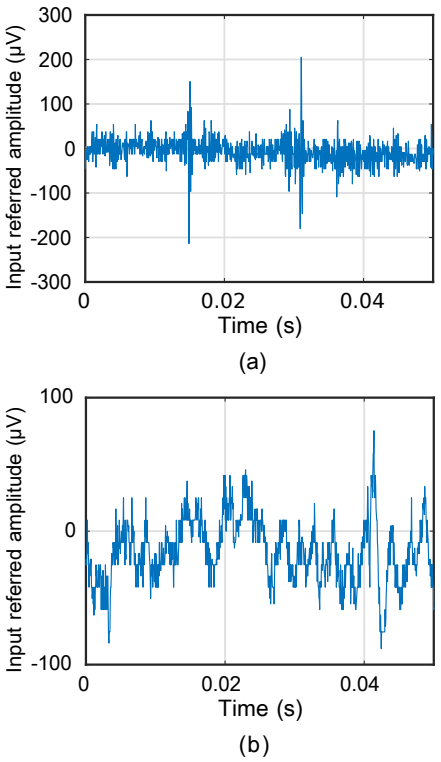

FIGURE 3.14: In-vitro measurements in the AP (a) and FR (b) modes for a prerecorded neural signal.

limited input swing [43] or action potential band omission [45]. Additionally, it includes spectral selectivity functionality which is not present in any other sub-μW front-end.

A comparison with conventional wideband front-ends can be made via $\mathrm{NEF_{Spot}}$[75] defined as follows,

$$\mathrm{NEF_{Spot}} = \mathrm{V_{n,Spot}}\sqrt{\frac{2\mathrm{Isupply}}{\pi \mathrm{V_T} 4\mathrm{kT}}}. \tag{3.14}$$

This figure of merit is a modification of the classic NEF [53] that codifies noise efficiency in terms of supply current and spot noise. SNR is calculated by way of (3.11) at 500 Hz for a worst case V_S=1 $\mu\mathrm{V}/\sqrt{\mathrm{Hz}}$, with V_E being omitted to provide some generality. Fig. 3.15(a) shows that the proposed front-end exhibits the lowest NEF while maintaining sufficient SNR, meaning that the proposed design strategy is the most efficient and it does not imply significant loss of information. It therefore follows one of the principles of low-power design pointed out by [93] which calls for a reduction in the amount of information that needs to be processed. Finally, Fig. 3.15(b) reveals that the supply

TABLE 3.3: Comparison with front-ends with spectral selectivity.

	[52]	[49]	[50]	[48]	**This work**
Process / Year	65 nm / 2012	180 nm / 2017	350 nm / 2017	130 nm SOI / 2017	180 nm / 2019
VDD (V)	0.5	1.8	3-3.3	1.2	1
Power (μW)	2)5.04	1)9	22	2)23.4	0.803 (LFP,WB) / 0.815 (AP,FR)
Area (mm^2)	2)0.013	-	2)0.17	2)0.12	0.192
f_L (Hz)	DC / 300	0.3 / 3)300	0.02 / 74-750	0.5 / 300 / 500 / 1 k	1 / 200
f_H (Hz)	300 / 10 k	3)300 / 7 k	200-330 / 6.34 k - 9.4 k	1 k / 10 k	700 / 950 / 5 k
Offset rejection (mV)	±50 mV	AC-coupled	AC-coupled	AC-coupled	AC-coupled
Noise	4)100 nV/$\sqrt{\text{Hz}}$ (LFP) 4.9 μVrms (AP) -	- - 4.57 μVrms (WB)	1.16 μVrms (LFP) 2.12 μVrms (AP) 4)30 nV/$\sqrt{\text{Hz}}$ (WB)	4)70 nV/$\sqrt{\text{Hz}}$ (LFP) 6.36 μVrms (AP) -	55 nV/$\sqrt{\text{Hz}}$ (LFP) 4.1 μVrms (AP) 75 nV/$\sqrt{\text{Hz}}$ (WB)
CMRR (dB)	75 dB	81 dB	69 dB (LFP) / 70 dB (AP)	¿60 dB	58 dB (LFP/WB) / 68 dB (AP/FR)
PSRR (dB)	64 dB	71 dB	72 dB (LFP/AP)	¿70 dB	54 dB (LFP/WB) / ¿64 dB (AP/FR)
THD	2 % at max. gain	-61 dB at 10mVpp	¡-39 dB	0.4 % at 10 mVpp	¡1 % for 1 mVp

1) Power consumption does not include subsequent filters. 2) Includes ADC. 3) Tunable around 300 Hz. 4) Estimated at 500 Hz.

TABLE 3.4: Comparison with sub-μW front-ends.

	[47]	[45]	[43]	[46]	[85]	**This work**
Process / Year	500 nm / 2012	350 nm / 2014	180 nm / 2013	180 nm / 2018	180 nm / 2018	180 nm / 2019
VDD (V)	1	2.5	0.45	0.5	3)0.5	1
Power (μW)	0.8	0.87	0.73	0.7	0.8	0.803 (WB)
Gain (dB)	36	40.7	52	39.5	38.5	40.4
f_L (Hz)	0.3	0.5	0.25	1	0.4	1 / 200
f_H (Hz)	4.7 k	1 k	2.5 k - 10 k	6.8 k	10.9 k	700 / 950 / 5 k
Spot Noise at 500 Hz (nV/$\sqrt{\text{Hz}}$)	1)50	1)50	1)30	1)40	1)30	75 (WB)
CMRR (dB)	-	¿ 70 dB	73 dB	40 dB	¿60	¿58 dB
PSRR (dB)	5.5 dB	¿ 70 dB	80 dB	45 dB	-	¿54 dB
THD	7.1 % at 1mVpp	1 % at 2.5 mVp	2)0.53% at 90% output	2.2% at 92 mV Output	-74 dB at 3 mVpp input	¡1 % for 1 mVp
Spectral selectivity	No	No	No	No	No	Yes

1) Estimated, 2) Reported an input swing of 10 μV with no clipping issues, 3) Requires additional DC bias circuit for input PMOS due to low VDD.

current in the proposed front-end is the lowest, thus confirming the efficiency of the design.

3.6 Conclusions

This work presented a wideband reconfigurable front-end that consumes up to 815 nW. This power consumption represents a 6.1x reduction compared against previously reported works with similar aim. This is then, the first front-end with spectral selectivity in the sub-μW range. Unlike other sub-μW front-ends, the power consumption in the proposed front-end is achieved without penalizing input swing, CMRR or PSRR. To the best of my knowledge, the use of multiple signal-specific noise targets that take advantage of the spectral characteristics of the LFP an AP with the goal of reducing power consumption has not been reported previously. This front-end is also the first one to

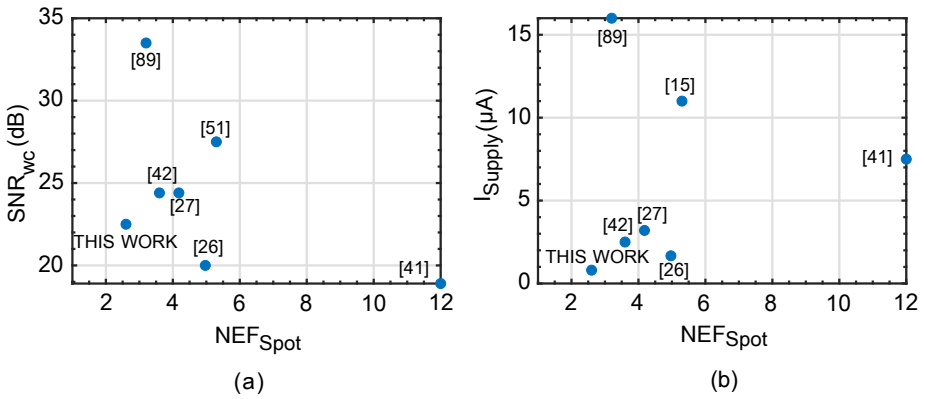

FIGURE 3.15: NEF_{Spot} of conventional front-ends against worst case SNR (a) and supply current (b).

include an specific bandwidth for fast ripples. Moreover, the proposed power-efficient low-noise design strategy can be easily mapped to other front-end topologies. Taking into account recent advances in power-efficient analog to digital converters, this work opens the way for the first sub-μW wideband reconfigurable neural recording channel.

Chapter 4

A High TCMRR, Inherently Charge Balanced Bidirectional Front-End for Multichannel Closed-Loop Neuromodulation

This chapter introduces a bidirectional front-end for simultaneous multichannel recording and stimulation. This is achieved by acknowledging the following points:

- The role the design of the stimulators play in artefact generation
- The impact large stimulation artefacts have on the multichannel recording front-end when impedance mismatch between electrodes and amplifiers is accounted for.

Indeed, recent works have already pointed out the importance of stimulator design in artefact mitigation [94] while single-channel recording front-ends with high tolerance to common-mode interference have being recently reported [95, 96]. The initial assumptions naturally lead us to design the proposed bidirectional front-end with charge balance and TCMRR as the main specifications.

4.1 Introduction

Residual charge in the electrodes due to mismatch in stimulation phases contributes to the increase of artefact magnitude over time. Fig. 4.1 shows a frequency domain view of

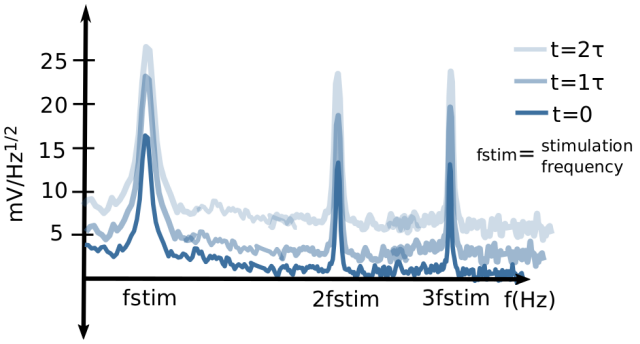

FIGURE 4.1: Frequency domain (Log scale) view of artefacts and their input-referred magnitude increase due to residual charge accumulation over time.

artefacts that reveals the presence of harmonics that can reach considerable magnitude. As covered in Sections 1.4.1, it is possible to picture an scenario in which closed-loop neuromodulation is successful for the first few stimulation pulses, however due to residual charge accumulation over time, artefacts become large enough to saturate the recording front-end.

As covered in Section 2.2, few works are designed for tolerance to self-interference. However, none of them consider the problem of multichannel recording in the presence of artefacts. Additional considerations have to be made in the design of the multichannel recording front-end so that it is able to sense in the presence of artefacts. Ng and Xu [27] described an scenario in which the common-mode rejection of the amplifiers in a multichannel recording front-end is degraded by impedance mismatch between input and reference electrodes (Fig. 4.2(a)). This effect is captured by the concept of total common-mode rejection ratio (TMCRR) as follows[27]:

$$TCMRR = \left(\frac{1}{ICMRR} + \left(\frac{1 + 2(|Z_{IN}/Z_e| + N\epsilon)}{2(N\epsilon - 1)}\right)^{-1}\right)^{-1}, \tag{4.1}$$

where N is the number of channels sharing a single reference electrode, ϵ is the mismatch factor between reference and signal electrodes (ϵ=1 when both electrodes are matched), $|Z_{IN}/Z_e|$ is the impedance ratio between input and electrode impedances and ICMRR is the intrinsic common-mode rejection ratio (i.e. the CMRR of a single channel). In order to maintain a sufficiently high TCMRR, $|Z_{IN}/Z_e|$ should be high, ICMRR high and N should be modest. TCMRR emerged originally as a way to account for common-mode interference from capacitive coupling of electrical supply voltages in mind (as high as 100 mVpp). Evidently, it acquires greater importance in the presence of large common-mode stimulation artefacts (as high as 1 Vpp). A model for a single recording channel in a closed-loop neuromodulator is shown in Fig. 4.2(b).

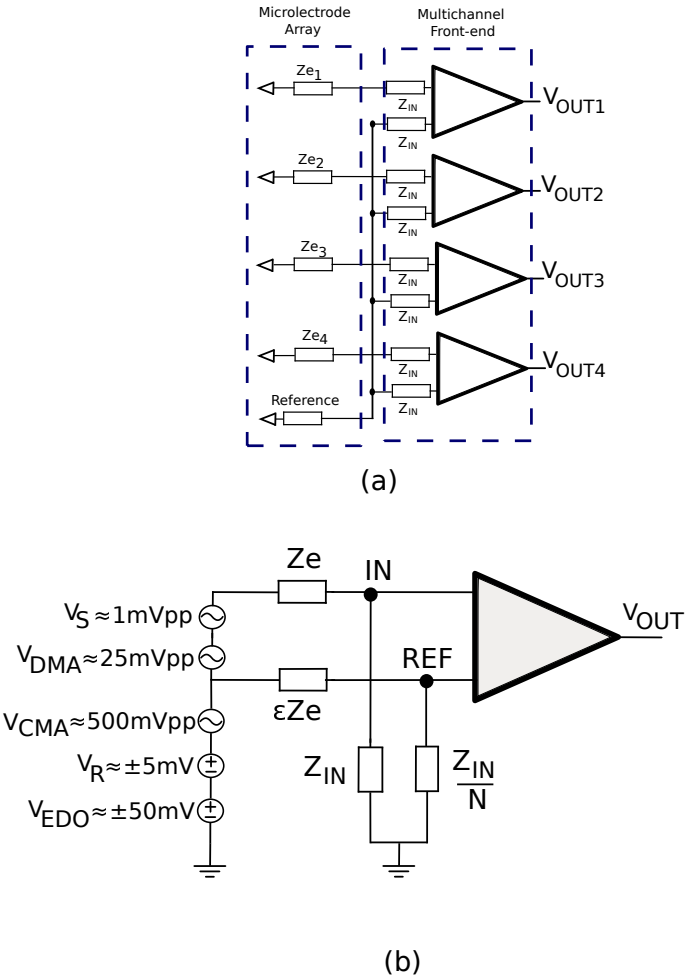

FIGURE 4.2: (a) Configuration for multichannel recording (b) Model for a single channel in a multichannel recording interface in the presence of self-interference (extended from [27]). V_S is the neural signal of interest, V_{DMA} is the differential-mode artefact, V_{CMA} is the common-mode artefact, V_R is the ratcheting effect and V_{EDO} is the electrode DC offset. Amplitudes for V_{DMA}, V_{CMA}, V_R will increase over time if the stimulation pulses are not balanced.

4.2 Bidirectional front-end for multichannel closed-loop neuromodulation

Figure 4.3 shows the block diagram of the proposed 8-channel bidirectional front-end. The circuit is comprised by a 4-channel stimulator front-end and a 4-channel recording front-end. The system is powered by V_{DDH}=3.3 V (stimulator) and V_{DDL}=1.8 V (recording) supply. The stimulation front-end includes input terminals to control stimulation waveform and amplitude. The recording front-end is driven by externally set

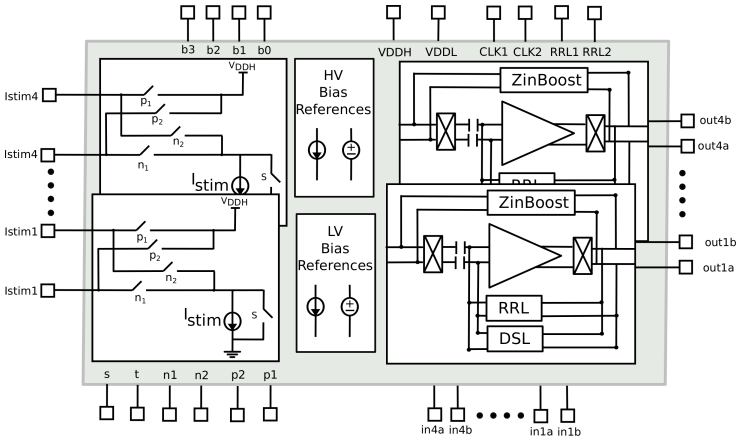

FIGURE 4.3: Proposed bidirectional front-end.

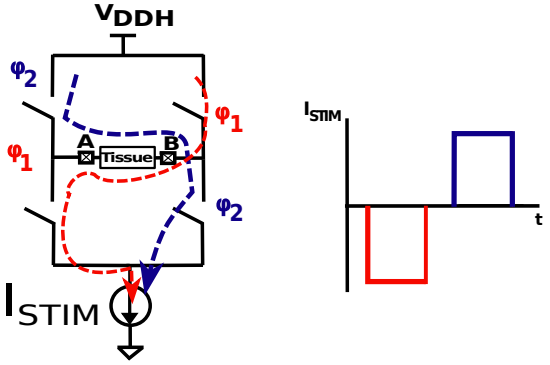

FIGURE 4.4: H-bridge operation.

clocks.

4.2.1 H-Bridge Inherently Charge-Balanced Stimulator

The design of a neural stimulator in a closed-loop neuromodulator differs slightly from its open-loop counterpart in that some specifications become more stringent. The design of such a stimulator is introduced herein.

4.2.1.1 Considerations for neural stimulation in a closed-loop system

Ideally, the biphasic stimulus pulse would be enough to guarantee charge balance. However, this scheme is susceptible to path and current source or sink mismatches that cause a significant deviation from the ideal in the form of residual charge. This deviation is usually corrected with additional strategies such as dynamic current mirror matching

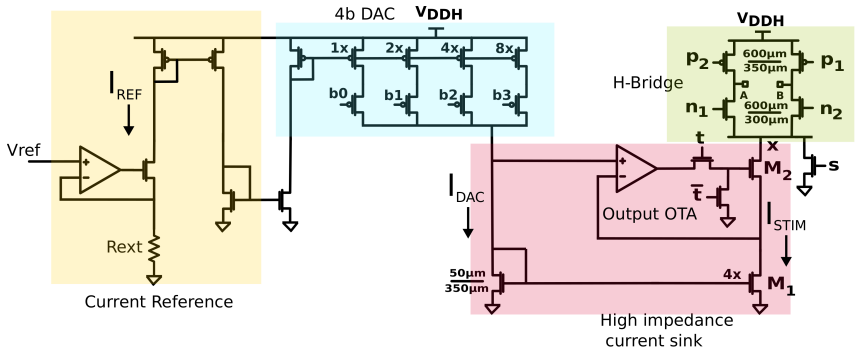

FIGURE 4.5: Proposed Stimulator.

[97, 98], active feedback [98, 99] or current calibration [100, 101]. These solutions do satisfy the requirements for tissue and microelectrode safety, however, since they operate in open-loop fashion (i.e. no amplifiers connected to the same electrode array), they make no consideration for artefacts. As explained before, residual charge accumulation is a fundamental contributor to artefact magnitude and becomes even more so in a multichannel system in which multiple stimulators operate. Although completely eliminating artefacts is not a feasible solution, it is nonetheless possible to conceive a stimulation system that generates non-saturating artefacts that allow for simultaneous recording and stimulation. These non-saturating artefacts can then be either filtered post-amplification [102] or cancelled post-digitization [103, 104]. Evidently, the definition of a non-saturating artefact depends on the recording setup, which in a multichannel system should consider common-mode interferer rejection degradation due to microelectrode mismatch. Considering that a priori artefact magnitude estimates via modeling are unreliable, we are forced to design a stimulator system with the highest possible charge balance in order to minimize residual charge as much as possible.

Fig. 4.4 shows the employed stimulation scheme. It involves an H-bridge operation to produce a biphasic pulse from a single current sink. Since the same current sink is shared in both phases, mismatch between stimulation pulses is practically non-existent. As a consequence, this scheme is inherently charge balanced and requires no additional circuitry. The residual charge due to path mismatches and electrode non-idealities can be easily removed by an additional shorting phase. This scheme has been demonstrated in proprioceptive and cochlear prosthesis [105, 106], peripheral nerve stimulation [107] and general purpose neural stimulation [108, 109]. To the best of the authors knowledge, this scheme was first proposed in [110].

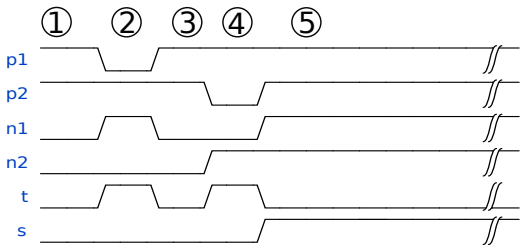

FIGURE 4.6: Stimulator time diagram.

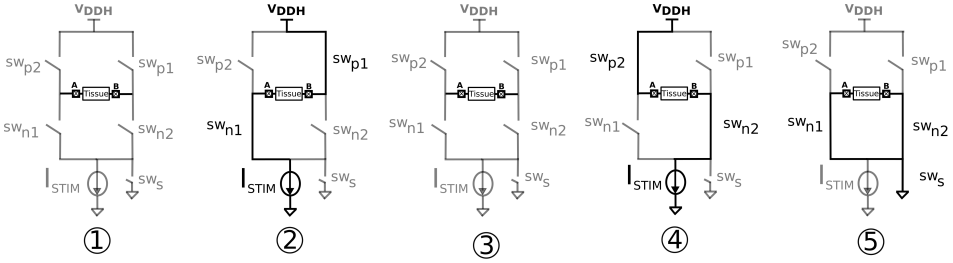

FIGURE 4.7: Stimulator operation.

4.2.1.2 Proposed neural stimulator

The proposed neural stimulator is shown in Fig. 4.5. The 4-channel stimulation front-end uses a single current reference while each channel is comprised by a 4-bit digital to analog converter (DAC), a high-impedance current sink (HICS) and an H-bridge. In fact, the combination of an HICS with an H-bridge was first proposed in [111], however, the focus of [111] is on output impedance and current efficiency. Indeed, the authors of [111] do not mention stimulation artefacts and fail to recognize the advantages of an output H-bridge in terms of charge balance. The focus of this work is mainly on charge balance and non-saturating artefact generation as the stimulation system is part of a bidirectional interface. The proposed stimulator is comprised entirely by 3.3 V devices. The stimulation current (I_{STIM}) flows through the H-bridge built by wide P (600 μm / 350 nm) and N (600 μm / 300 nm) transistors to minimize mismatch. An additional transistor is added to the H-bridge to short the output electrodes to ground after each biphasic pulse (passive discharge). I_{STIM} then sinks into the proposed HICS that exhibits an output impedance defined at node X as:

$$R_{out} \simeq Agm_2ro_2ro_1. \tag{4.2}$$

where A is the gain of the output OTA, gm_2 and ro_2 are the transconductance and output resistance of M_2 and is ro_1 the output resistance of M_1. A high-gain telescopic cascode is used as the output OTA. The DAC is implemented by a binary weighted

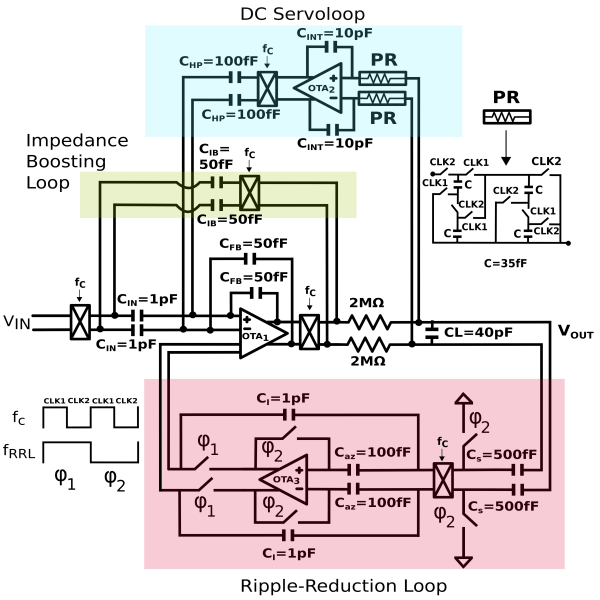

FIGURE 4.8: Proposed CCIA.

current mirror that is fed from a reference current implemented as a current conveyor. A single current conveyor distributes current to each stimulation channel. The reference current is defined as $I_{ref} = V_{ref}/R_{ext}$, where V_{ref} and R_{ext} are externally set.

The timing diagram of the stimulator is shown in Fig. 4.6 and its operation is shown in Fig. 4.7. The stimulator is turned off in State 1. In State 2, switches sw_{p1} and sw_{n1} are turned on. This causes I_{STIM} to flow from B to A, thus creating the cathodic pulse. In State 3 all switches are off. This creates an interphase delay which is usually much shorter than the width of each pulse. The anodic pulse is created in State 4 when switches sw_{p2} and sw_{n2} are turned on. I_{STIM} thus flows from A to B, creating the anodic pulse. State 5 shorts the outputs by closing sw_s off. This discharges the electrodes after each biphasic pulse, thus providing a DC current error that is safe for both the neural tissue and microelectrodes. The stimulator can be programmed to produce different waveforms such as monophasic or high-frequency chopped pulses.

4.2.2 Chopper Amplifier for High TCMRR Recording

High TCMRR recording systems are necessary to tolerate self-interference and thus allow for simultaneous multichannel recording during stimulation. This is valid even if said self-interference comes from a stimulator system that generates non-saturating artefacts as they are still larger in magnitude than what the conventional neural recording systems can handle. High TCMRR systems for wideband neural recording have been previously

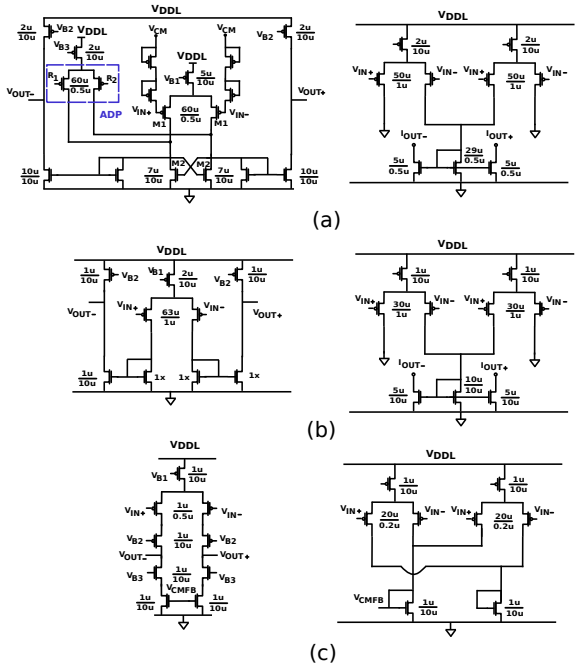

FIGURE 4.9: (a) OTA_1 and CMFB (b) OTA_2 and CMFB (c) OTA_3 and CMFB.

reported in [27] and [112]. However, these works are not optimal for closed-loop neuromodulators since they are designed for tolerance to environmental and power-supply interference that is much lower in magnitude than stimulation artefacts. For instance, the ac common mode range in [27] is limited to 220 mVpp while [112] exhibits a total harmonic distortion (THD) of 0.37 % for 4 mVpp differential input signals.

In this work we propose a capacitively-coupled chopper instrumentation amplifier (CCIA) as the basis for a high TCMRR recording system. The CCIA upmodulates the input signal to a chopping frequency before amplification. The input signal is then modulated back into the baseband frequency while $1/f$ noise and amplifier DC offset are upmodulated to the chopping frequency. An output low-pass filter then restores the input signal while filtering away the upmodulated noise and offset. More importantly, this technique has shown excellent common-mode rejection characteristics [113] [78] along with low-power consumption (¡ 5 μW). Besides, it is possible to obtain low distortion for differential signals by setting a moderate gain [95]. Input impedance is lowered in inverse proportion to the chopping frequency, however, this can be compensated by impedance boosting techniques [78] [95].

The proposed CCIA is shown in Fig. 4.8. The gain is set to 20 V/V by way of the ratio between input (C_{IN}=1 pF) and feedback (C_{FB}=50 fF) capacitors. In this way, V_S and V_{DMA} are amplified without risk of saturation. A current mirror amplifier with

partial positive feedback [114] has been chosen for OTA_1 (Fig. 4.9(a)). This OTA features rail-to-rail output and boosts bandwidth and open-loop gain so that a second OTA in the forward path can be obviated. Moreover, it offers high input common-mode range as its input stage requires only ~ 0.6 V to operate assuming weak inversion in all transistors [114]. The employed common-mode feedback (CMFB) monitors the output common-mode voltage of OTA_1 and compensates it by sinking currents from the very same output [83]. The bandwidth of the CCIA is set by a passive low-pass filter to about 600 Hz. The input impedance ($Z_{IN} = \frac{1}{2f_c C_{IN}}$) is controlled by setting a modest chopping clock frequency (f_c) of 2.5 kHz. In practice, this value is expected to be degraded due to pad parasitics, nevertheless, a positive feedback impedance boosting loop has been included to obtain higher input impedance [78].

The input chopping switches cancel the ac coupling, requiring the use of a DC servoloop (DCSL) to reject V_{EDO} and V_R. The DCSL introduces a high-pass frequency corner to the transfer function of the CCIA by feedbacking an integrator with a very large time constant. The high-pass frequency corner is defined as follows [115]:

$$f_{HP} = \frac{C_{HP}}{C_{FB}} \frac{1}{2\pi PRC_{INT}}, \tag{4.3}$$

where PR is a switched capacitor pseudoresistor [116] defined as:

$$PR = \frac{10}{Cf_s}. \tag{4.4}$$

where $f_s = f_c$ The maximum V_{EDO} and V_R that the DCSL can handle can be estimated according to:

$$V_{INDC} = \frac{C_{HP}}{C_{IN}} V_{DCSL}, \tag{4.5}$$

where V_{INDC}=V_{EDO}+V_R and V_{DCSL} is the maximum voltage at the DCSL output approximated to the supply voltage V_{DDL}. Thus, for a C_{HP}=100 fF, C_{FB}=50 fF and C_{IN}=1 pF, the high-pass frequency corner is f_{HP}=0.28 Hz while the maximum offset rejection is V_{INDC}=$\pm$180 mV. In this circuit we employed a current mirror amplifier for OTA_2 (Fig. 4.9(b)) due to its rail-to-rail output swing while implementing the same common-mode feedback strategy as in OTA_1.

Chopper modulation introduces an output ripple whose magnitude is proportional to the amplifier offset. This ripple can be attenuated by a ripple-reduction loop (RRL) that senses the ripple and compensates it in the input stage [117]. In this work we employ

the auto-zeroed switched capacitor integrator introduced in [78]. The RRL is driven by a clock at half of the chopping frequency. In phase ϕ_1, the circuit senses the output ripple voltage with capacitors C_S and produces and output voltage via C_I. This voltage is then converted into a proportional current by way of the auxiliary differential pair (ADP) in OTA_1 (Fig. 4.9(a). During phase ϕ_2, no ripple is sensed and the integrator samples and stores the offset voltage of OTA_3 in C_{az} while C_I holds the voltage of the previous phase. The RRL acts as a notch in the transfer function of the CCIA at the chopping frequency whose width is [117]:

$$f_{RRL} = \frac{G_{mA}C_S}{2\pi C_L C_I}, \tag{4.6}$$

where G_{mA} is the transconductance of the ADP. Assuming a G_{mA}=400μS, C_S=1pF, C_L=40pF and C_I=500fF, yields an f_{RRL}=795 Hz, which falls outside the CCIA bandwidth assuming f_c=2.5 kHz. The gain in the RRL is given by:

$$A_{RRL} = \frac{A_3 G_{mA}}{C_L f_c}, \tag{4.7}$$

where A_3 is the gain of OTA_3. A_{RRL} is directly related to ripple suppression which necessitates A_3 to be as high as possible. OTA_3 is therefore implemented with a telescopic topology as show in 4.9(c).

The input-referred noise in the CCIA can be expressed as follows:

$$\overline{IRN^2_{CCIA}} = v^2_{n,1}\left(\frac{C_{IN} + C_{FB} + C_{IB} + +C_{HP}}{C_{IN}}\right)^2 \Delta f, \tag{4.8}$$

where Δf is the bandwidth of the CCIA (defined by the output filter) and $v^2_{n,1}$ is the noise spectral density of OTA_1. Assuming negligible $1/f$ contribution due to chopper modulation, $v^2_{n,1}$ is approximated as follows [83]:

$$v^2_{n,1} = \frac{8kT\gamma}{G_{mM1}}\left(1 + \frac{2G_{mM2}}{G_{mM1}}\right). \tag{4.9}$$

where k is the Boltzmann constant, T is the temperature and γ is a process dependent parameter. The noise contribution by the RRL can be made negligible by making G_{mA} much smaller than G_{mM1} [78].

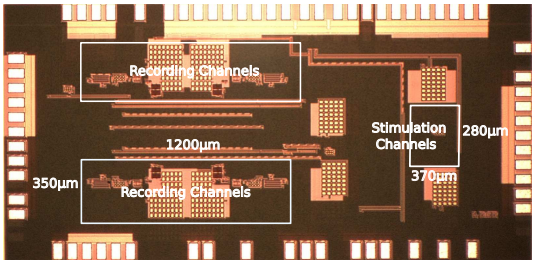

FIGURE 4.10: Die micrograph.

4.3 Measurement Results

Fig. 4.10 shows a photo of the fabricated prototype. The circuit was fabricated in a standard CMOS 0.18 μm process. The sub-blocks were spread out over the available area in order to ease routing for experimental testing. A single recording channel occupies 0.21 mm^2. The area can be reduced by placing the active circuits underneath capacitors. A single stimulation channel occupies 0.026 mm^2. The total effective area of the 8-channel front-end is calculated to be 0.94 mm^2.

4.3.1 Stimulation front-end characterization

Benchtop testing for the stimulator was carried out emulating and electrode load with a discrete capacitor and resistor included in the test board. DIP switches were used to control the DAC inputs. An off-chip variable resistor was used to set the less significant bit (via I_{REF}) such that the maximum current (DAC=1111) was 300 μA. The stimulator front-end was powered by a 3.3 V external supply. The stimulation waveforms were configured by a USB Logic Analyzer. Residual voltage was measured with a 6 1/2 digit resolution multimeter.

Fig. 4.11(a) shows a biphasic stimulation pulse of 600 μs per phase for a R=5 kΩ C=100 nF load. The DAC functionality was tested for a R=5 kΩ load, showing a maximum current of 300 μA (Fig. 4.11(b)). Charge balance was characterized by stimulating 10 biphasic pulses of 600 μs. The residual voltage was measured right after the last pulse. The final shorting phase was removed for this test. Fig. 4.12(a) shows the residual voltage for each stimulator after 10 biphasic pulses for each stimulator. The worst case residual charge is about 106 pC (Fig. 4.12(b)) while the total injected charge can be calculated from the stimulation current and the pulse width as follows: 300 μA $\times$ 600 μs = 180 nC. The worst case charge mismatch is therefore residual/injected $\times$ 100, which is 0.059%.

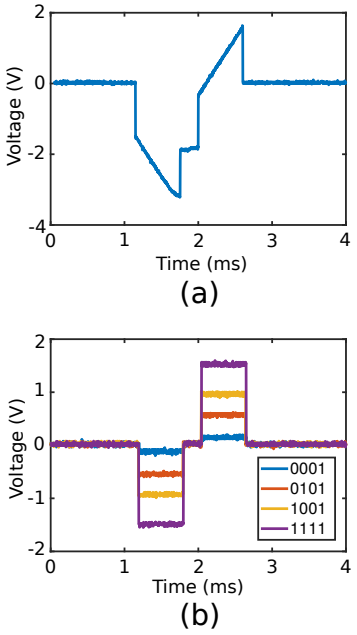

FIGURE 4.11: Stimulator front-end. (a) Waveform for an R+C load (b) Waveform for an R load.

DC current error is calculated by activating the shorting phase (via sw_s) after the anodic pulse. This creates a passive discharge described as follows:

$$q(t) = q(0) \cdot e^{(-t/RC)} \tag{4.10}$$

where $q(0)$ is the residual charge right after the anodic pulse, $q(t)$ is the residual charge after the shorting time t, R and C are the electrode time constant. Assuming time periods for cathodic, anodic and inter phases to be 1.4 ms and a total pulse interval of 3 ms, the available shorting time is t=1.6 ms. The electrode time constant for the test load is 5 kΩ $\times$ 100 nF = 500 μs. Thus, for a worst case $q(0)$=106 pC, the residual charge after shorting is $q(t)$=4.3 pC. The DC current error can then be calculated by dividing $q(t)$ over the pulse interval i.e., 4.3 pC / 3 ms = 1.4 nA, which complies with tissue and electrode safety specifications. It should be noted that this is not a fixed result and the DC current error can be made smaller by increasing the shorting phase.

4.3.2 Recording front-end characterization

The recording front-end was powered by an external 1.8 V supply. The 4-channel front-end draws 12.96 uW. The following tests were made on a single recording channel.

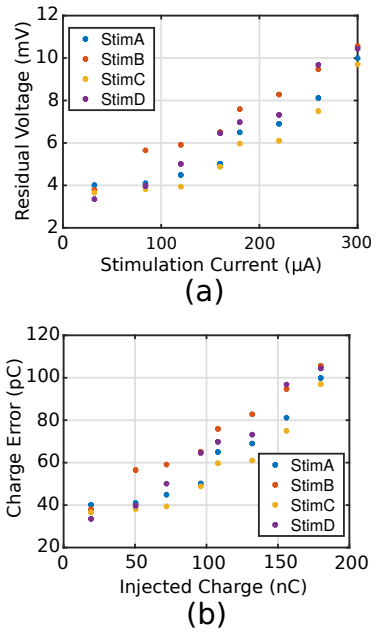

FIGURE 4.12: Stimulator front-end. (a) Residual voltage after 10 biphasic pulses (b) Charge error.

Fig. 4.13(a) shows the frequency response. The recording front-end shows a 600 Hz bandwidth and a $\sim$ 1 dB gain drop from the original target due to parasitics. This drop is within the expected variation. Fig. 4.13(b) shows the input-referred noise. The noise integrated from 1 - 600 Hz is 7.5 μVrms. The following tests are related to artefact tolerance for a single recording channel. THD is shown in Fig. 4.14(a). The recording front-end shows 2.85% THD for a 120 mVpp differential input. Fig. 4.14(b) shows the input ac common-mode range. The front-end exhibits a 5% gain drop for 1 Vpp common-mode inputs at 200 Hz. We should expect this variation to hold true for input signals within the recording bandwidth. ICMRR measured for 500 mVpp inputs is kept above 80 dB (Fig. 4.15(a)) in the recording bandwidth while PSRR hovers over 63 dB (Fig. 4.15(b))

Input impedance was measured by coupling a known external capacitor with the front-end's inputs. This creates a high-pass frequency corner where the time-constant is related to the input impedance [118]. This procedure was performed for each channel. ICMRR at 200 Hz for 500 mVpp was measured for each channel as well. These measurements are shown in Table 4.1. The calculated TCMRR assuming an electrode impedance = 100 kΩ [27] is above 66 dB for all channels.

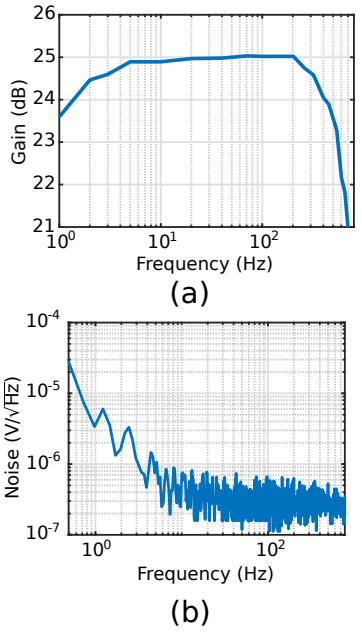

FIGURE 4.13: Recording front-end. (a) Noise (b) Gain.

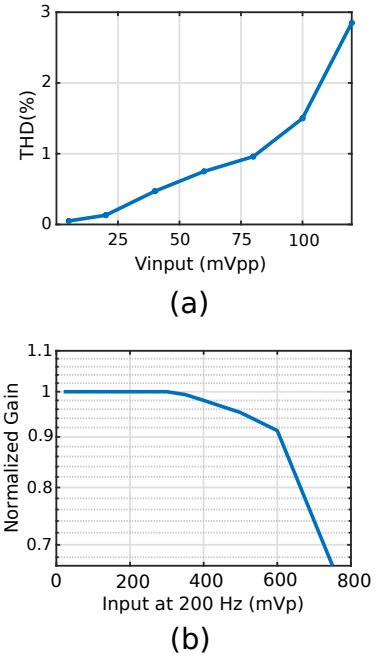

FIGURE 4.14: Recording front-end. (a) Total Harmonic Distortion (b) Input ac common-mode range.

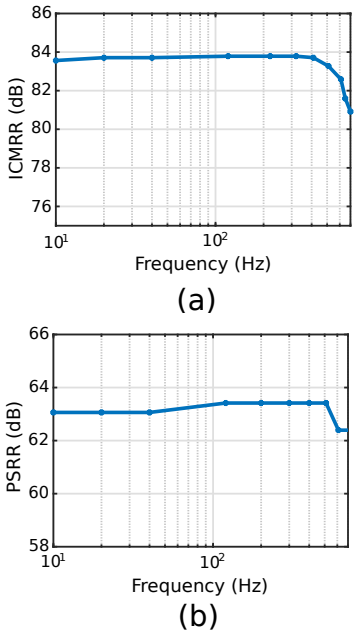

FIGURE 4.15: Recording front-end. (a) Intrinsic common-mode rejection ratio (b) Power-supply rejection ratio.

TABLE 4.1: Total common-mode rejection ratio at 200 Hz.

Recording channel	**Zin (MΩ)**	**ICMRR (dB)**	**TCMRR (dB)**
A	826	81	66.9
B	816	83	67.1
C	795	80	66.4
D	884	88	68.4

4.3.3 Self-interference characterization

Closed-loop experiments were performed in a beaker filled with saline solution. The stimulator outputs and recording inputs were connected to the same microelectrode array, which was then submerged in the solution. A diagram of the experimental setup is shown in Fig. 4.16. A multichannel array of surface microelectrodes was used for this test (FlexMEA36, Multichannel systems).

In the first test, every stimulator was set to $fstim$=200 Hz at their maximum current capability. Initially, only one stimulator was active while the others were progressively activated one by one. The measurements were taken after a few minutes to allow for some charge accumulation in the electrodes. Fig. 4.17 shows the output of a single recording

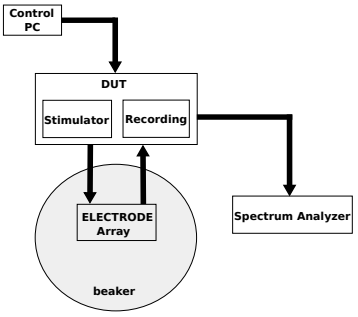

FIGURE 4.16: Test setup for closed-loop characterization.

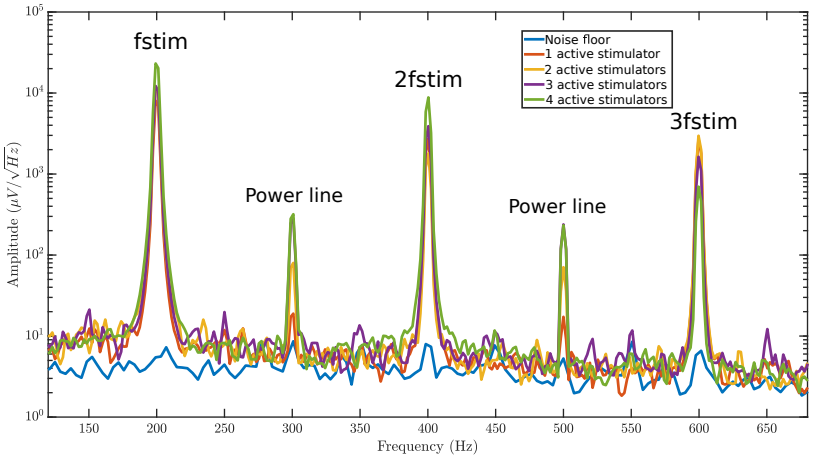

FIGURE 4.17: Artefact Magnitude.

channel. The results confirm the relationship between the number of active stimulators and the magnitude of the artefact. The magnitude of the first harmonic increases from 8 mV with a single active stimulator to 23 mV with four active stimulators. However, it should be noted that this relationship does not hold true for the 3rd harmonic. More importantly, the results show that the stimulator front-end generates non-saturating artefacts that fall within the lineal range of the recording front-end.

4.3.4 Comparison with the state of the art

The specifications are summarized and compared with previous art in Table 4.2. The comparison is made only with those works that have demonstrated simultaneous recording and stimulation. The proposed bidirectional front-end is the only one to account for electrode mismatch and its effect on the recorder. Expanding on this, [69] exhibits only ICMRR = 12 dB for 100 mVpp common-mode inputs. This would translate to about TCMRR = 11.7 dB per channel in the 64 channel recording system. Moreover,

TABLE 4.2: Comparison with closed-loop neuromodulators

	[69]	[70]	[68, 72]	This work
Process (nm)	65	40,180 HV	180 HV	180
Ch. Rec. / Stim.	[1)]64 / 16	64 / 8	64 / 4	4 / 4
Power (Rec.) (μW/Ch.)	[5)]2.7	[5)]8.2	[5)]8	3.24
BW (Hz)	8.3 k	250	500	600
Noise	8.2 μVrms	2.2 μVrms	68 nV/rtHz	7.5 μVrms
Offset Rejection	ac-coupled	-	± 200 mV	±180 mV
THD	[2)]-	[4)]-	0.012% at 100mVpp	2.85% at 120 mVpp
AC CMI Range	-	-	-	1 Vpp
ICMRR (dB)	12 for 100 mVpp	-	85 for unspecified input	¿ 80 for 500 mVpp
TCMRR (dB)	[3)]11.7	-	[6)]14.44	¿ 66
Charge Balance	-	-	¡ 1%	0.059%
DC error	-	-	-	1.4 nA

1) Only 8 out of the 64 channels are differential artefact tolerant. 2) Dynamic range = 77 dB for 200 mVpp inputs. 3) Calculated for 64 channels and Z_{IN}=1/(j2πfC_S), f= 200 Hz, C_S=1pF. 4) SFDR = 81 dB for 100 mVpp differential input. 5) Includes ADC. 6) Calculated for Z_{IN}= 30MΩ as estimated by [70].

this work does not demonstrate any particular preoccupation for artefact mitigation in the stimulator design. Similarly, [68, 72] features an estimated Z_{IN}= 30 MΩ [70], which in turn yields a TCMRR of only 14.44 dB.

Unfortunately, TCMRR cannot be estimated for [70] as this work does not publish ICMRR. However, a qualitative estimate can be made: the mismatch between the input high-pass filters degrades the CMRR substantially. An ICMRR = 66 dB was reported in [119] for a similar front-end, which in combination with the number of recording channels points to a degraded TCMRR.

4.4 Conclusions

This work presented an 8-channel bidirectional front-end for closed-loop neuromodulation. The proposed dual design strategy focuses on mitigating artefacts at their origin via stimulation charge balance and tolerating them at their end via TCMRR. As a result, the stimulation front-end produces programmable biphasic pulses that generate non-saturating artefacts while the recording front-end is able to reject large common-mode interference in the presence of degradation due to electrode mismatch. To the best of the authors knowledge, this is the first demonstration of such a design approach to implantable closed-loop neuromodulators.

Chapter 5

Conclusions and Future Directions

5.1 Conclusions

This thesis presented two different prototypes for implantable neural interfacing applications.

The first prototype is in many ways a proposal to escape the ever-present noise and power trade-off. Due to physical laws, the power consumption in optimally designed recording front-ends had settled to about 2 μW in the last few years. The only exit route to this conundrum was to re-evaluate the traditional noise specifications that had been set in stone for twenty years. This was made possible by recent research in neuroscience and materials. The result was a front-end that reduced by 2.5x the power consumption of conventional front-ends and 6.1x those with spectral selectivity.

The second prototype proposes a solution to the problem of simultaneous recording and stimulation in a bidirectional interface. The proposal involves, on one hand, the design of the stimulator front-end aimed at minimizing artefacts via charge balance. On the other hand, the recording front-end designed for tolerance to large common-mode interference and also acknowledgement of the electrode mismatch problem. The result was a stimulation front-end that generates non-saturating artefacts and a recording front-end that tolerates them.

Each front-end offers specifications not available in any other work. They are a step towards more advanced applications in the field of implantable neural interfaces. The underlying conclusion of this work is that electrodes significantly impact the performance

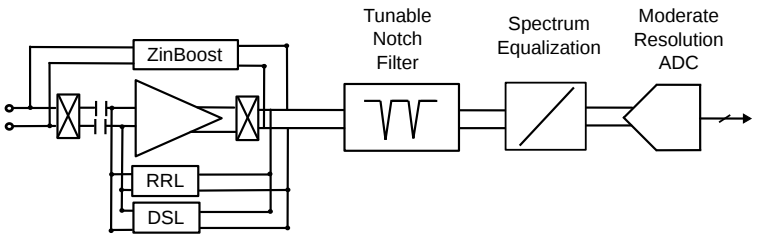

FIGURE 5.1: Artefact free recording channel.

of the interface which leads to the revelation of trade-offs in the front-end + amplifier system.

5.2 Future Directions

There is room for incremental improvement in both front-ends. For instance, further power reduction can be achieved in the first prototype by reducing the voltage supply. This would of course come with the trade-off of lower input and output swing, but a modest reduction to about 0.6 V would still yield significant savings (489 nW). Also, an additional ADC stage can be added in order to complete a neural recording channel. It is expected that power consumption would still be sub-μW since nanowatt ADCs for neural recording applications have been reported in the literature.

The second prototype can be benefited by additional experimental testing. Multichannel sensing in the presence of artefacts is a must to fully validate the aim of this work. The characteristics of this prototype also enable it as a sort of test chip in which artefact modeling (from design parameters) can be verified. For example, artefact modeling in a multichannel bidirectional array is missing in the literature.

The second prototype can be improved in a few significant ways. For instance, a higher voltage compliance and a full power management unit can be implemented on-chip. Fig. 5.1 shows a possible back-end for the recording front-end. It involves the addition of tunable notch filters to produce an artefact-free output and an equalization stage to reduce the requirements of the ADC stage.

Appendix A

Verification of noise model

The noise model for the prototype introduced in Chapter 3 is verified against the measured noise. Fig. A.1 shows the measured noise spectrum for the WB mode. This figure also plots the models for the individual noise contributions and the complete noise model. The modeled spectra plot stems from the noise analysis in Sections 3.3.1 and 3.4. The low-frequency slope in the noise spectral density is verified via (3.9). Afterwards, (3.7) was employed to calculate the total noise power spectral density as described by (3.10). The model plot used the following parameter values: A_2=25, T= 300 K, C_{OX}=9 fF/μm^2, K_n=10 x 10^{-25} J and K_p=5 x 10^{-25} J. Capacitor and transistor sizes were obtained from Table 3.1. For OTA_3 gm_3=60 pS was assumed and for OTA_1, gm_n=7 μS and gm_p=5.5 μS were assumed. This result confirms that the low-frequency slope is due to the thermal noise introduced by OTA_3. The LFP mode also shows this characteristic. The deviation in noise spectral density between model and measurements comes from a model overestimation of thermal noise sources.

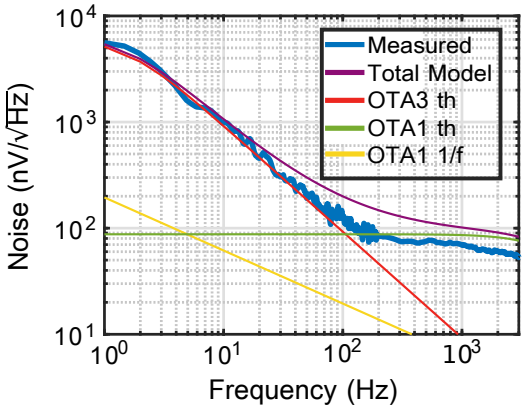

FIGURE A.1: Measured noise and model in the WB mode.

Bibliography

[1] ET McAdams, A Lackermeier, JA McLaughlin, D Macken, and J Jossinet. The linear and non-linear electrical properties of the electrode-electrolyte interface. *Biosensors and Bioelectronics*, 10(1-2):67–74, 1995.

[2] Craig T Nordhausen, Edwin M Maynard, and Richard A Normann. Single unit recording capabilities of a 100 microelectrode array. *Brain research*, 726(1-2): 129–140, 1996.

[3] Liang Guo. Perspectives on electrical neural recording: a revisit to the fundamental concepts. *Journal of Neural Engineering*, 2020.

[4] György Buzsáki, Costas A Anastassiou, and Christof Koch. The origin of extracellular fields and currents—EEG, ECoG, LFP and spikes. *Nature reviews neuroscience*, 13(6):407, 2012.

[5] Biyu J He. Scale-free brain activity: past, present, and future. *Trends in cognitive sciences*, 18(9):480–487, 2014.

[6] György Buzsáki and Andreas Draguhn. Neuronal oscillations in cortical networks. *science*, 304(5679):1926–1929, 2004.

[7] Wyeth Bair, Christof Koch, William Newsome, and Kenneth Britten. Power spectrum analysis of bursting cells in area mt in the behaving monkey. *Journal of Neuroscience*, 14(5):2870–2892, 1994.

[8] Kai J Miller, Larry B Sorensen, Jeffrey G Ojemann, and Marcel Den Nijs. Power-law scaling in the brain surface electric potential. *PLoS computational biology*, 5 (12):e1000609, 2009.

[9] Jozsef Csicsvari, Darrell A Henze, Brian Jamieson, Kenneth D Harris, Anton Sirota, Péter Barthó, Kensall D Wise, and Gyorgy Buzsaki. Massively parallel recording of unit and local field potentials with silicon-based electrodes. *Journal of neurophysiology*, 90(2):1314–1323, 2003.

[10] Arjun K Bansal, Carlos E Vargas-Irwin, Wilson Truccolo, and John P Donoghue. Relationships among low-frequency local field potentials, spiking activity, and three-dimensional reach and grasp kinematics in primary motor and ventral premotor cortices. *Journal of neurophysiology*, 105(4):1603–1619, 2011.

[11] Alain Destexhe, Diego Contreras, and Mircea Steriade. Spatiotemporal analysis of local field potentials and unit discharges in cat cerebral cortex during natural wake and sleep states. *Journal of Neuroscience*, 19(11):4595–4608, 1999.

[12] Spencer Kellis, Kai Miller, Kyle Thomson, Richard Brown, Paul House, and Bradley Greger. Decoding spoken words using local field potentials recorded from the cortical surface. *Journal of neural engineering*, 7(5):056007, 2010.

[13] Bradley Voytek, Mark A Kramer, John Case, Kyle Q Lepage, Zechari R Tempesta, Robert T Knight, and Adam Gazzaley. Age-related changes in 1/f neural electrophysiological noise. *Journal of Neuroscience*, 35(38):13257–13265, 2015.

[14] Tobias Loddenkemper, Andrew Pan, Silvia Neme, Kenneth B Baker, Ali R Rezai, Dudley S Dinner, Erwin B Montgomery Jr, and Hans O Lüders. Deep brain stimulation in epilepsy. *Journal of Clinical Neurophysiology*, 18(6):514–532, 2001.

[15] Alim Louis Benabid, Stephan Chabardes, John Mitrofanis, and Pierre Pollak. Deep brain stimulation of the subthalamic nucleus for the treatment of parkinson's disease. *The Lancet Neurology*, 8(1):67–81, 2009.

[16] Daniel R Cleary, Alp Ozpinar, Ahmed M Raslan, and Andrew L Ko. Deep brain stimulation for psychiatric disorders: where we are now. *Neurosurgical focus*, 38 (6):E2, 2015.

[17] Benjamin D Greenberg, Donald A Malone, Gerhard M Friehs, Ali R Rezai, Cynthia S Kubu, Paul F Malloy, Stephen P Salloway, Michael S Okun, Wayne K Goodman, and Steven A Rasmussen. Three-year outcomes in deep brain stimulation for highly resistant obsessive–compulsive disorder. *Neuropsychopharmacology*, 31(11):2384, 2006.

[18] Christof Koch, Marcello Massimini, Melanie Boly, and Giulio Tononi. Neural correlates of consciousness: progress and problems. *Nature Reviews Neuroscience*, 17(5):307, 2016.

[19] Avery Tye Gardner, Hunter S Stratham, David J Warren, and Ross M Walker. Impedance and noise characterizations of utah and microwire electrode arrays. *IEEE Journal of Electromagnetics, RF and Microwaves in Medicine and Biology*, 2018.

[20] Vijay Viswam, Marie Engelene J Obien, Felix Franke, Urs Frey, and Andreas Reinhold Hierlemann. Optimal electrode size for multi-scale extracellular-potential recording from neuronal assemblies. *Frontiers in neuroscience*, 13:385, 2019.

[21] Peng Cong. Neural interfaces for implantable medical devices: Circuit design considerations for sensing, stimulation, and safety. *IEEE Solid-State Circuits Magazine*, 8(4):48–56, 2016.

[22] Thomas Jochum, Timothy Denison, and Patrick Wolf. Integrated circuit amplifiers for multi-electrode intracortical recording. *Journal of neural engineering*, 6(1): 012001, 2009.

[23] Reid R Harrison. The design of integrated circuits to observe brain activity. *Proceedings of the IEEE*, 96(7):1203–1216, 2008.

[24] David Kleinfeld, Lan Luan, Partha P Mitra, Jacob T Robinson, Rahul Sarpeshkar, Kenneth Shepard, Chong Xie, and Timothy D Harris. Can one concurrently record electrical spikes from every neuron in a mammalian brain? *Neuron*, 103(6):1005–1015, 2019.

[25] Timothy M Seese, Hiroaki Harasaki, Gerald M Saidel, and Charles R Davies. Characterization of tissue morphology, angiogenesis, and temperature in the adaptive response of muscle tissue to chronic heating. *Laboratory investigation; a journal of technical methods and pathology*, 78(12):1553–1562, 1998.

[26] Hariprasad Chandrakumar and Dejan Marković. A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation. *IEEE Journal of Solid-State Circuits*, 52(3):645–656, 2017.

[27] Kian Ann Ng and Yong Ping Xu. A low-power, high CMRR neural amplifier system employing CMOS inverter-based OTAs with CMFB through supply rails. *IEEE Journal of Solid-State Circuits*, 51(3):724–737, 2016.

[28] Julián Oreggioni, Angel A Caputi, and Fernando Silveira. Current-efficient preamplifier architecture for CMRR sensitive neural recording applications. *IEEE Transactions on Biomedical Circuits and Systems*, 12(3):689–699, 2018.

[29] Daniel R Merrill, Marom Bikson, and John GR Jefferys. Electrical stimulation of excitable tissue: design of efficacious and safe protocols. *Journal of neuroscience methods*, 141(2):171–198, 2005.

[30] Stuart F Cogan. Neural stimulation and recording electrodes. *Annu. Rev. Biomed. Eng.*, 10:275–309, 2008.

[31] John C Lilly, John R Hughes, Ellsworth C Alvord Jr, and Thelma W Galkin. Brief, noninjurious electric waveform for stimulation of the brain. *Science*, 1955.

[32] Wen-Yang Hsu and Alexandre Schmid. Compact, energy-efficient high-frequency switched capacitor neural stimulator with active charge balancing. *IEEE transactions on biomedical circuits and systems*, 11(4):878–888, 2017.

[33] Mahboubeh Parastarfeizabadi, Abbas Z Kouzani, Jaclyn Beckinghausen, Tao Lin, and Roy V Sillitoe. A programmable multi-biomarker neural sensor for closed-loop dbs. *IEEE Access*, 7:230–244, 2018.

[34] Mikhail A Lebedev and Miguel AL Nicolelis. Brain–machine interfaces: past, present and future. *TRENDS in Neurosciences*, 29(9):536–546, 2006.

[35] Marco Capogrosso, Tomislav Milekovic, David Borton, Fabien Wagner, Eduardo Martin Moraud, Jean-Baptiste Mignardot, Nicolas Buse, Jerome Gandar, Quentin Barraud, David Xing, et al. A brain–spine interface alleviating gait deficits after spinal cord injury in primates. *Nature*, 539(7628):284, 2016.

[36] Jeffrey Lim, Po T Wang, Alireza K Bidhendi, Omid M Arasteh, Susan J Shaw, Michelle Armacost, Hui Gong, Charles Y Liu, Payam Heydari, An H Do, et al. Characterization of Stimulation Artifact Behavior in Simultaneous Electrocorticography Grid Stimulation and Recording. In *2018 40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 4748–4751. IEEE, 2018.

[37] Edgar A Brown, James D Ross, Richard A Blum, Yoonkey Nam, Bruce C Wheeler, and Stephen P DeWeerth. Stimulus-artifact elimination in a multi-electrode system. *IEEE transactions on biomedical circuits and systems*, 2(1):10–21, 2008.

[38] Peter Single and Jonathan Scott. Cause of Pulse Artefacts Inherent to the Electrodes of Neuromodulation Implants. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 26(10):2078–2083, 2018.

[39] Chung-Yu Wu, Cheng-Hsiang Cheng, and Zhi-Xin Chen. A 16-channel cmos chopper-stabilized analog front-end ecog acquisition circuit for a closed-loop epileptic seizure control system. *IEEE transactions on biomedical circuits and systems*, 12(3):543–553, 2018.

[40] Jian Xu, Tong Wu, Wentai Liu, and Zhi Yang. A frequency shaping neural recorder with 3 pF input capacitance and 11 plus 4.5 bits dynamic range. *IEEE Transactions on Biomedical Circuits and Systems*, 8(4):510–527, 2014.

[41] Hossein Kassiri, Arezu Bagheri, Nima Soltani, Karim Abdelhalim, Hamed Mazhab Jafari, M Tariqus Salam, Jose Luis Perez Velazquez, and Roman Genov. Battery-less tri-band-radio neuro-monitor and responsive neurostimulator for diagnostics and treatment of neurological disorders. *IEEE Journal of Solid-State Circuits*, 51 (5):1274–1289, 2016.

[42] Masoud Rezaei, Esmaeel Maghsoudloo, Cyril Bories, Yves De Koninck, and Benoit Gosselin. A low-power current-reuse analog front-end for high-density neural recording implants. *IEEE Transactions on Biomedical Circuits and Systems*, 12 (2):271–280, 2018.

[43] Dong Han, Yuanjin Zheng, Ramamoorthy Rajkumar, Gavin Stewart Dawe, and Minkyu Je. A 0.45 V 100-channel neural-recording IC with Sub-μW/Channel consumption in 0.18 μm CMOS. *IEEE Transactions on Biomedical Circuits and Systems*, 7(6):735–746, 2013.

[44] S Song, MJ Rooijakkers, P Harpe, C Rabotti, M Mischi, AHM Van Roermund, and E Cantatore. A 430nW 64nV/$\sqrt{}$ Hz current-reuse telescopic amplifier for neural recording applications. In *Biomedical Circuits and Systems Conference (BioCAS), 2013 IEEE*, pages 322–325. IEEE, 2013.

[45] Tzu-Yun Wang, Min-Rui Lai, Christopher M Twigg, and Sheng-Yu Peng. A fully reconfigurable low-noise biopotential sensing amplifier with 1.96 noise efficiency factor. *IEEE Transactions on Biomedical Circuits and Systems*, 8(3):411–422, 2014.

[46] Seong-Jin Kim, Su-Hyun Han, Ji-Hyoung Cha, Lei Liu, Lei Yao, Yuan Gao, and Minkyu Je. A Sub-μW/Ch analog front-end for Δ-neural recording with spike-driven data compression. *IEEE Transactions on Biomedical Circuits and Systems*, 2018.

[47] Fan Zhang, Jeremy Holleman, and Brian P Otis. Design of ultra-low power biopotential amplifiers for biosignal acquisition applications. *IEEE Transactions on Biomedical Circuits and Systems*, 6(4):344–355, 2012.

[48] Carolina Mora Lopez, Jan Putzeys, Bogdan Cristian Raducanu, Marco Ballini, Shiwei Wang, Alexandru Andrei, Veronique Rochus, Roeland Vandebriel, Simone Severi, Chris Van Hoof, et al. A neural probe with up to 966 electrodes and up to 384 configurable channels in 0.13μm SOI CMOS. *IEEE Transactions on Biomedical Circuits and Systems*, 11(3):510–522, 2017.

[49] Xilin Liu, Milin Zhang, Andrew G Richardson, Timothy H Lucas, and Jan Van der Spiegel. Design of a closed-loop, bidirectional brain machine interface system with

energy efficient neural feature extraction and PID control. *IEEE Transactions on Biomedical Circuits and Systems*, 11(4):729–742, 2017.

[50] Yan Liu, Song Luan, Ian Williams, Adrien Rapeaux, and Timothy G Constandinou. A 64-channel versatile neural recording SoC with activity-dependent data throughput. *IEEE Transactions on Biomedical Circuits and Systems*, 11(6):1344–1355, 2017.

[51] Byunghun Lee and Maysam Ghovanloo. An adaptive averaging low noise front-end for central and peripheral nerve recording. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 65(7), 2018.

[52] Rikky Muller, Simone Gambini, and Jan M Rabaey. A 0.013mm^2, 5μW, DC-Coupled neural signal acquisition IC with 0.5 V supply. *IEEE Journal of Solid-State Circuits*, 47(1):232–243, 2012.

[53] Michel SJ Steyaert and Willy MC Sansen. A micropower low-noise monolithic instrumentation amplifier for medical purposes. *IEEE Journal of Solid-State Circuits*, 22(6):1163–1168, 1987.

[54] Meysam Azin, David J Guggenmos, Scott Barbay, Randolph J Nudo, and Pedram Mohseni. A battery-powered activity-dependent intracortical microstimulation ic for brain-machine-brain interface. *IEEE Journal of Solid-State Circuits*, 46(4): 731–745, 2011.

[55] Hyo-Gyuem Rhew, Jaehun Jeong, Jeffrey A Fredenburg, Sunjay Dodani, Parag G Patil, and Michael P Flynn. A fully self-contained logarithmic closed-loop deep brain stimulation soc with wireless telemetry and wireless power management. *IEEE Journal of Solid-State Circuits*, 49(10):2213–2227, 2014.

[56] William Biederman, Daniel J Yeager, Nathan Narevsky, Jaclyn Leverett, Ryan Neely, Jose M Carmena, Elad Alon, and Jan M Rabaey. A 4.78 mm 2 fully-integrated neuromodulation soc combining 64 acquisition channels with digital compression and simultaneous dual stimulation. *IEEE Journal of Solid-State Circuits*, 50(4):1038–1047, 2015.

[57] Ruslana Shulyzki, Karim Abdelhalim, Arezu Bagheri, M Tariqus Salam, Carlos M Florez, Jose Luis Perez Velazquez, Peter L Carlen, and Roman Genov. 320-channel active probe for high-resolution neuromonitoring and responsive neurostimulation. *IEEE transactions on biomedical circuits and systems*, 9(1):34–49, 2014.

[58] Yu-Po Lin, Chun-Yi Yeh, Pin-Yang Huang, Zong-Ye Wang, Hsiang-Hui Cheng, Yi-Ting Li, Chi-Fen Chuang, Po-Chiun Huang, Kea-Tiong Tang, Hsi-Pin Ma, et al.

A battery-less, implantable neuro-electronic interface for studying the mechanisms of deep brain stimulation in rat models. *IEEE transactions on biomedical circuits and systems*, 10(1):98–112, 2015.

[59] Mahsa Shoaran, Masoud Shahshahani, Masoud Farivar, Joyel Almajano, Amirhossein Shahshahani, Alexandre Schmid, Anatol Bragin, Yusuf Leblebici, and Azita Emami. A 16-channel 1.1 mm 2 implantable seizure control soc with sub-μw/channel consumption and closed-loop stimulation in 0.18 μm cmos. In *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, pages 1–2. Ieee, 2016.

[60] Scott Stanslaski, Pedram Afshar, Peng Cong, Jon Giftakis, Paul Stypulkowski, Dave Carlson, Dave Linde, Dave Ullestad, Al-Thaddeus Avestruz, and Timothy Denison. Design and validation of a fully implantable, chronic, closed-loop neuromodulation device with concurrent sensing and stimulation. *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, 20(4):410–421, 2012.

[61] RNS. Neuropace User Manual, 2016. URL https://www.neuropace.dreamhosters.com/manuals/RNS_System/User/_Manual.pdf.

[62] NIH BRAIN Initiative. Public-private partnership program: devices and support specific manufacturers, 2018. URL https://braininitiative.nih.gov/sites/default/files/pdfs/ppp/_rns/_device/_info/_508c.pdf.

[63] Scott Stanslaski, Jeffrey Herron, Tom Chouinard, Duane Bourget, Ben Isaacson, Vaclav Kremen, Enrico Opri, William Drew, Benjamin H Brinkmann, Aysegul Gunduz, et al. A chronically implantable neural coprocessor for investigating the treatment of neurological disorders. *IEEE transactions on biomedical circuits and systems*, 12(6):1230–1245, 2018.

[64] Maeike Zijlmans, Premysl Jiruska, Rina Zelmann, Frans SS Leijten, John GR Jefferys, and Jean Gotman. High-frequency oscillations as a new biomarker in epilepsy. *Annals of neurology*, 71(2):169–178, 2012.

[65] Tolga Esat Özkurt, Markus Butz, Melanie Homburger, Saskia Elben, Jan Vesper, Lars Wojtecki, and Alfons Schnitzler. High frequency oscillations in the subthalamic nucleus: a neurophysiological marker of the motor state in parkinson's disease. *Experimental neurology*, 229(2):324–331, 2011.

[66] Wei-Ming Chen, Herming Chiueh, Tsan-Jieh Chen, Chia-Lun Ho, Chi Jeng, Ming-Dou Ker, Chun-Yu Lin, Ya-Chun Huang, Chia-Wei Chou, Tsun-Yuan Fan, et al. A fully integrated 8-channel closed-loop neural-prosthetic cmos soc for real-time epileptic seizure control. *IEEE Journal of Solid-State Circuits*, 49(1):232–247, 2013.

[67] Byunghun Lee, Yaoyao Jia, S Abdollah Mirbozorgi, Mark Connolly, Xingyuan Tong, Zhaoping Zeng, Babak Mahmoudi, and Maysam Ghovanloo. An inductively-powered wireless neural recording and stimulation system for freely-behaving animals. *IEEE transactions on biomedical circuits and systems*, 13(2):413–424, 2019.

[68] Benjamin C Johnson, Simone Gambini, Igor Izyumin, Ali Moin, Andy Zhou, George Alexandrov, Samantha R Santacruz, Jan M Rabaey, Jose M Carmena, and Rikky Muller. An implantable 700μW 64-channel neuromodulation IC for simultaneous recording and stimulation with rapid artifact recovery. In *2017 Symposium on VLSI Circuits*, pages C48–C49. IEEE, 2017.

[69] Seobin Jung, Paul Kwon, David Piech, Michel Maharbiz, Jan Rabaey, and Elad Alon. A 2.7-μW Neuromodulation AFE With 200 mVpp Differential-Mode Stimulus Artifact Canceler Including On-Chip LMS Adaptation. *IEEE Solid-State Circuits Letters*, 1(10):194–197, 2018.

[70] Dejan Rozgić, Vahagn Hokhikyan, Wenlong Jiang, Ippei Akita, Sina Basir-Kazeruni, Hariprasad Chandrakumar, and Dejan Marković. A 0.338 cm^3, Artifact-Free, 64-Contact Neuromodulation Platform for Simultaneous Stimulation and Sensing. *IEEE Transactions on Biomedical Circuits and Systems*, 13(1):38–55, 2018.

[71] Peng Cong, Piyush Karande, Jonathan Landes, Rob Corey, Scott Stanslaski, Wes Santa, Randy Jensen, Forrest Pape, Dan Moran, and Tim Denison. A 32-channel modular bi-directional neural interface system with embedded dsp for closed-loop operation. In *ESSCIRC 2014-40th European Solid State Circuits Conference (ESSCIRC)*, pages 99–102. IEEE, 2014.

[72] Andy Zhou, Samantha R Santacruz, Benjamin C Johnson, George Alexandrov, Ali Moin, Fred L Burghardt, Jan M Rabaey, Jose M Carmena, and Rikky Muller. A wireless and artefact-free 128-channel neuromodulation device for closed-loop stimulation and recording in non-human primates. *Nature biomedical engineering*, 3(1):15, 2019.

[73] Joshua Milstein, Florian Mormann, Itzhak Fried, and Christof Koch. Neuronal shot noise and brownian 1/f2 behavior in the local field potential. *PloS one*, 4(2): e4338, 2009.

[74] Agrita Dubey and Supratim Ray. Cortical Electrocorticogram (ECoG) is a local signal. *Journal of Neuroscience*, 39(22):4299–4311, 2019.

[75] William A Smith, Brian J Mogen, Eberhard E Fetz, Visvesh S Sathe, and Brian P Otis. Exploiting electrocorticographic spectral characteristics for optimized signal

chain design: A 1.08 μW analog front end with reduced ADC resolution requirements. *IEEE Transactions on Biomedical Circuits and Systems*, 10(6):1171–1180, 2016.

[76] Jose Luis Valtierra, Rafaella Fiorelli, Manuel Delgado-Restituto, and Angel Rodriguez-Vazquez. A sub-μW reconfigurable front-end for invasive neural recording. In *2019 IEEE 10th Latin American Symposium on Circuits & Systems (LASCAS)*, pages 85–88. IEEE, 2019.

[77] Greg A Worrell, Andrew B Gardner, S Matt Stead, Sanqing Hu, Steve Goerss, Gregory J Cascino, Fredric B Meyer, Richard Marsh, and Brian Litt. High-frequency oscillations in human temporal lobe: simultaneous microwire and clinical macroelectrode recordings. *Brain*, 131(4):928–937, 2008.

[78] Qinwen Fan, Fabio Sebastiano, Johan H Huijsing, and Kofi AA Makinwa. A 1.8 μW 60 nV/$\sqrt{Hz}$ capacitively-coupled chopper instrumentation amplifier in 65 nm CMOS for wireless sensor nodes. *IEEE Journal of Solid-State Circuits*, 46(7): 1534–1543, 2011.

[79] Matthias Kuhl and Yiannos Manoli. A 0.01 mm^2 fully-differential 2-stage amplifier with reference-free CMFB using an architecture-switching-scheme for bandwidth variation. In *European Solid-State Circuits Conference (ESSCIRC), ESSCIRC 2015-41st*, pages 287–290. IEEE, 2015.

[80] Pieter Harpe, Hao Gao, Rainier van Dommele, Eugenio Cantatore, and Arthur HM van Roermund. A 0.20 $mm^2$3 nw signal acquisition IC for miniature sensor nodes in 65 nm CMOS. *IEEE Journal of Solid-State Circuits*, 51(1):240–248, 2016.

[81] Jung-Chen Chung, Wei-Ming Chen, and Chung-Yu Wu. An 8-channel power-efficient time-constant-enhanced analog front-end amplifier for neural signal acquisition. In *Circuits and Systems (ISCAS), 2015 IEEE International Symposium on*, pages 1234–1237. IEEE, 2015.

[82] Rahul Sarpeshkar, Richard F Lyon, and Carver Mead. A low-power wide-linear-range transconductance amplifier. In *Neuromorphic systems engineering*, pages 267–313. Springer, 1998.

[83] Alireza Karimi-Bidhendi, Omid Malekzadeh-Arasteh, Mao-Cheng Lee, Colin M McCrimmon, Po T Wang, Akshay Mahajan, Charles Yu Liu, Zoran Nenadic, An H Do, and Payam Heydari. CMOS ultralow power brain signal acquisition front-ends: Design and human testing. *IEEE Transactions on Biomedical Circuits and Systems*, 11(5):1111–1122, 2017.

[84] Subramaniam Venkatraman, Craig Patten, and Jose M Carmena. Exploiting the 1/f structure of neural signals for the design of integrated neural amplifiers. In *Engineering in Medicine and Biology Society, 2009. EMBC 2009. Annual International Conference of the IEEE*, pages 2050–2053. IEEE, 2009.

[85] Sung-Yun Park, Jihyun Cho, Kyounghwan Na, and Euisik Yoon. Modular 128-channel Δ-Δ Σ analog front-end architecture using spectrum equalization scheme for 1024-channel 3-D neural recording microsystems. *IEEE Journal of Solid-State Circuits*, 53(2):501–514, 2018.

[86] M Reza Pazhouhandeh, Hossein Kassiri, Aly Shoukry, Iliya Wesspapir, Peter Carlen, and Roman Genov. Artifact-tolerant opamp-less delta-modulated bidirectional neuro-interface. In *2018 IEEE Symposium on VLSI Circuits*, pages 127–128. IEEE, 2018.

[87] A Tye Gardner, John Mize, David J Warren, and Ross M Walker. Comparative characterization of in vivo and in vitro noise of the SIROF Utah electrode array. In *SENSORS, 2017 IEEE*, pages 1–3. IEEE, 2017.

[88] Juan Martinez, Carlos Pedreira, Matias J Ison, and Rodrigo Quian Quiroga. Realistic simulation of extracellular recordings. *Journal of neuroscience methods*, 184 (2):285–293, 2009.

[89] Reid R Harrison and Cameron Charles. A low-power low-noise CMOS amplifier for neural recording applications. *IEEE Journal of Solid-State Circuits*, 38(6): 958–965, 2003.

[90] Chang Hao Chen, Elizabeth A McCullagh, Sio Hang Pun, Peng Un Mak, Mang I Vai, Pui In Mak, Achim Klug, and Tim C Lei. An integrated circuit for simultaneous extracellular electrophysiology recording and optogenetic neural manipulation. *IEEE Transactions on Biomedical Engineering*, 64(3):557–568, 2017.

[91] Hansjörg Scherberger, Murray R Jarvis, and Richard A Andersen. Cortical local field potential encodes movement intentions in the posterior parietal cortex. *Neuron*, 46(2):347–354, 2005.

[92] Vinay Shirhatti, Ayon Borthakur, and Supratim Ray. Effect of reference scheme on power and phase of the local field potential. *Neural computation*, 28(5):882–913, 2016.

[93] Rahul Sarpeshkar. Universal principles for ultra low power and energy efficient design. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 59(4): 193–198, 2012.

[94] Andy Zhou, Benjamin C Johnson, and Rikky Muller. Toward true closed-loop neuromodulation: artifact-free recording during stimulation. *Current opinion in neurobiology*, 50:119–127, 2018.

[95] Hariprasad Chandrakumar and Dejan Marković. An 80-mVpp Linear-Input Range, 1.6-GΩ Input Impedance, Low-Power Chopper Amplifier for Closed-Loop Neural Recording That Is Tolerant to 650-mVpp Common-Mode Interference. *IEEE Journal of Solid-State Circuits*, 52(11):2811–2828, 2017.

[96] Antonios Nikas, Sreenivas Jambunathan, Leonhard Klein, Matthias Voelker, and Maurits Ortmanns. A continuous-time delta-sigma modulator using a modified instrumentation amplifier and current reuse dac for neural recording. *IEEE Journal of Solid-State Circuits*, 2019.

[97] Ji-Jon Sit and Rahul Sarpeshkar. A low-power blocking-capacitor-free charge-balanced electrode-stimulator chip with less than 6 na dc error for 1-ma full-scale stimulation. *IEEE Transactions on Biomedical Circuits and Systems*, 1(3):172–183, 2007.

[98] Hosung Chun, Yuanyuan Yang, and Torsten Lehmann. Safety ensuring retinal prosthesis with precise charge balance and low power consumption. *IEEE transactions on biomedical circuits and systems*, 8(1):108–118, 2013.

[99] Natalie Butz, Armin Taschwer, Sebastian Nessler, Yiannos Manoli, and Matthias Kuhl. A 22 v compliant 56μw twin-track active charge balancing enabling 100% charge compensation even in monophasic and 36% amplitude correction in biphasic neural stimulators. *IEEE Journal of Solid-State Circuits*, 53(8):2298–2310, 2018.

[100] Zhicong Luo and Ming-Dou Ker. A high-voltage-tolerant and precise charge-balanced neuro-stimulator in low voltage cmos process. *IEEE transactions on biomedical circuits and systems*, 10(6):1087–1099, 2016.

[101] Elliot Greenwald, Christoph Maier, Qihong Wang, Robert Beaulieu, Ralph Etienne-Cummings, Gert Cauwenberghs, and Nitish Thakor. A cmos current steering neurostimulation array with integrated dac calibration and charge balancing. *IEEE transactions on biomedical circuits and systems*, 11(2):324–335, 2017.

[102] Konstantinos Petkos, Thomas Guiho, Patrick Degenaar, Andrew Jackson, Peter Brown, Timothy J Denison, and Emmanuel M Drakakis. A high-performance 4 nv/$\sqrt{Hz}$ analog front-end architecture for artefact suppression in local field potential recordings during deep brain stimulation. *Journal of neural engineering*, 2019.

[103] Sina Basir-Kazeruni, Stefan Vlaski, Hawraa Salami, Ali H Sayed, and Dejan Marković. A blind adaptive stimulation artifact rejection (asar) engine for closed-loop implantable neuromodulation systems. In *2017 8th International IEEE/EMBS Conference on Neural Engineering (NER)*, pages 186–189. IEEE, 2017.

[104] Stanislav Culaclii, Brian Kim, Yi-Kai Lo, Lin Li, and Wentai Liu. Online artifact cancelation in same-electrode neural stimulation and recording using a combined hardware and software architecture. *IEEE transactions on biomedical circuits and systems*, 12(3):601–613, 2018.

[105] Ian Williams and Timothy G Constandinou. An energy-efficient, dynamic voltage scaling neural stimulator for a proprioceptive prosthesis. *IEEE Transactions on Biomedical Circuits and Systems*, 7(2):129–139, 2013.

[106] Wannaya Ngamkham, Marijn N van Dongen, and Wouter A Serdijn. Biphasic stimulator circuit for a wide range of electrode-tissue impedance dedicated to cochlear implants. In *2012 IEEE International Symposium on Circuits and Systems*, pages 1083–1086. IEEE, 2012.

[107] Jayant Charthad, Ting Chia Chang, Zhaokai Liu, Ahmed Sawaby, Marcus J Weber, Sam Baker, Felicity Gore, Stephen A Felt, and Amin Arbabian. A mm-sized wireless implantable device for electrical stimulation of peripheral nerves. *IEEE transactions on biomedical circuits and systems*, 12(2):257–270, 2018.

[108] Eric Pepin, John Uehlin, Daniel Micheletti, Steve I Perlmutter, and Jacques C Rudell. A high-voltage compliant, electrode-invariant neural stimulator front-end in 65nm bulk-cmos. In *ESSCIRC Conference 2016: 42nd European Solid-State Circuits Conference*, pages 229–232. IEEE, 2016.

[109] Yong-Joon Jeon, Lei Yao, Yuan Gao, and Muthukumaraswamy Annamalai Arasu. A 0.034% charge-imbalanced neural stimulation front-end (sfe) ic with on-chip voltage compliance monitoring circuit and analysis on resting potential by utilizing the sfe ic. *IEEE Transactions on Circuits and Systems I: Regular Papers*, 2019.

[110] S Bourret, M Sawan, and R Plamondon. Programmable high-amplitude balanced stimulus current-source for implantable microstimulators. In *Proceedings of the 19th Annual International Conference of the IEEE Engineering in Medicine and Biology Society.'Magnificent Milestones and Emerging Opportunities in Medical Engineering'(Cat. No. 97CH36136)*, volume 5, pages 1938–1941. IEEE, 1997.

[111] Meysam Azin and Pedram Mohseni. A high-output-impedance current microstimulator for anatomical rewiring of cortical circuitry. In *2008 IEEE International Symposium on Circuits and Systems*, pages 2502–2505. IEEE, 2008.

[112] Sehwan Lee, Arup K George, Taeju Lee, Jun-Uk Chu, Sungmin Han, Ji-Hoon Kim, Minkyu Je, and Junghyup Lee. A 110db-cmrr 100db-psrr multi-channel neural-recording amplifier system using differentially regulated rejection ratio enhancement in 0.18 μm cmos. In *2018 IEEE International Solid-State Circuits Conference-(ISSCC)*, pages 472–474. IEEE, 2018.

[113] Tim Denison, Kelly Consoer, Wesley Santa, Al-Thaddeus Avestruz, John Cooley, and Andy Kelly. A 2μw 100 nv/rthz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials. *IEEE Journal of Solid-State Circuits*, 42(12):2934–2945, 2007.

[114] Rongtai Wang and Ramesh Harjani. Partial positive feedback for gain enhancement of low-power CMOS OTAs. In *Low-Voltage Low-Power Analog Integrated Circuits*, pages 21–35. Springer, 1995.

[115] Jiawei Zheng, Wing-Hung Ki, Langyu Hu, and Chi-Ying Tsui. Chopper capacitively coupled instrumentation amplifier capable of handling large electrode offset for biopotential recordings. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 64(12):1392–1396, 2017.

[116] Naveen Verma, Ali Shoeb, Jose Bohorquez, Joel Dawson, John Guttag, and Anantha P Chandrakasan. A Micro-Power EEG Acquisition SoC With Integrated Feature Extraction Processor for a Chronic Seizure Detection System. *IEEE Journal of Solid-State Circuits*, 45(4), 2010.

[117] Rong Wu, Kofi AA Makinwa, and Johan H Huijsing. A chopper current-feedback instrumentation amplifier with a 1 mHz $1/f$ noise corner and an AC-coupled ripple reduction loop. *IEEE Journal of Solid-State Circuits*, 44(12):3232–3243, 2009.

[118] Lieuwe B Leene and Timothy G Constandinou. A 0.006 mm^2 1.2μw analog-to-time converter for asynchronous bio-sensors. *IEEE Journal of Solid-State Circuits*, 53(9):2604–2613, 2018.

[119] Wenlong Jiang, Vahagn Hokhikyan, Hariprasad Chandrakumar, Vaibhav Karkare, and Dejan Marković. A$\pm$50-mv linear-input-range vco-based neural-recording front-end with digital nonlinearity correction. *IEEE Journal of Solid-State Circuits*, 52(1):173–184, 2016.