Programmable Resolution Imager for Imaging Applications

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ABSTRACT

In this paper a programmable imager with averaging capabilities will be described which is intended for averaging of different groups or sets of pixels formed by $n \times n$ kernels, $n \times m$ kernels or any group of randomly-selected pixels across the array. This imager is a 64×64 array which uses passive pixels with electronic shutter and anti-blooming structure that can be randomly accessed. The read-out stage includes a sole charge amplifier with programmable gain, a sample-and-hold structure and an analog buffer. This read-out structure is different from other existing imagers with variable resolution since it uses a sole charge amplifier, whereas the conventional structure employs an opamp per column plus another global opamp. This architecture allows a reduction of the fixed-pattern noise observed in standard imagers. The prototype also includes an analog to digital converter which provides the digital output of the images.

Keywords: CMOS imager, multi-resolution, averaging, binning.

1. INTRODUCTION

In the last years there has been a growing interest in the development of CMOS compatible imagers which can overcome the limitations of Charge Coupled Device (CCD) technology when small sizes, low power consumption and random access are required [1-3]. In particular this is the case where the spatial resolution of the imager is required to be variable. The concept of variable resolution imager is graphically illustrated in Figure 1 for an imager containing 32×32 optical sensors. Its maximum resolution is obtained when each of these sensors corresponds to a pixel of the image (Figure 1.a); however, in the variable resolution mode, each image pixel can be defined as the result of aggregating groups of sensors, thus resulting into an imager with smaller spatial resolution and uniform or non-uniform pixel size. Figure 1.b illustrates the case of a reduced image resolution, where sensors are uniformly aggregated into 4×4 kernels. On the other hand, Figure 1.c illustrates the case of non-uniform pixel size, where sensors are grouped in 4 different kernel sizes. This example shows a symmetrical variable resolution with a foveated distribution, however asymmetrical distributions are also possible. Fully programmable variable resolution imagers should enable random selection of the kernel size and kernel distribution, as well as random access to the averaged pixel output.

Variable resolution imagers can be used for different applications, such as image compression, target tracking or pattern recognition, where processing speed is increased by varying the image resolution. Variable resolution can also be used for image light-level adaptation, improving the sensitivity at the cost of a reduced resolution, or as an image pre-processing step, for example, as the image mean value calculation, or as a column/row mean value calculation, hence reducing the amount of information transferred to the image processor.

Multi-resolution or variable resolution can be achieved by two different methods: directly averaging the signals of the different pixels into a proportionally larger capacitor, or summing up ("binning") the signals in a unity size capacitor (especially intended for low light level applications). Selection of the different pixels to be read-out is normally done serially, although simultaneous selection is also possible when adding special circuitry.

Different chips have been reported with this capability, using charge integration amplifiers, both with active [4,5] and passive pixels [6,7], and innovative averaging techniques with active pixels [8]. The main characteristics of these imagers are summarized in Table 1. Those using charge integration amplifier actually do a binning of the signal charges, mainly intended to improve

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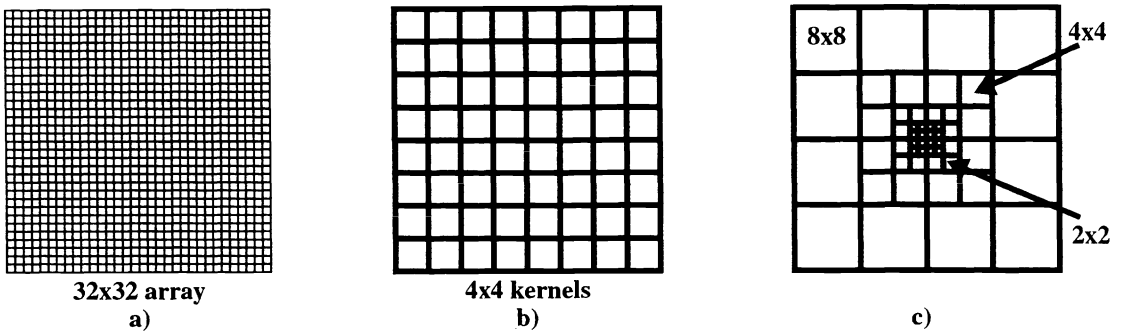


Figure 1. Variable resolution concept: a) full resolution image with 32x32 pixels; b) image resolution reduction where sensors are uniformly aggregated in 4x4 kernels; c) image resolution reduction with non-uniform kernel sizes (foveated distribution).

Table 1. Main characteristics of reported imagers with variable resolution.

imager	averaging circuitry	type of pixels	array size
Zhou et al. [4]	charge integration amplifier	active	32×32
Zhou et al. [5]	charge integration amplifier	active	128×128
CIVIS [6]	charge integration amplifier	passive	256×256
MAP2200 [7]	charge integration amplifier	passive	256×256
Kemeny et al. [8]	capacitor network	active	128×128

the sensitivity in low illumination applications, although it can also be used with normal illumination levels, reducing the integration time of the pixels proportionally to the number of pixels which are to be read-out [6]. The chip reported in Ref. 8 does not use charge integration amplifier but a passive switched capacitor network to averaging arbitrarily large neighborhoods of pixels which can be read-out by configuring a set of digital shift registers.

The first imagers incorporating variable resolution were those using passive pixels. The CIVIS chip [6], with a 256×256 array of pixels, has the typical architecture of this type of imagers. The pixel consists of a photodiode, which is also used for integrating the photo-generated signal, and a switch. Each column of photodiodes has its own read-out unit. This unit is used both for the read-out and the initialization of the photodiodes. For each column, signal summation of a number of photodiodes can be performed by serially addressing these rows without resetting the read-out unit in between. The chip has one common read-out circuit which is connected to all column read-out units and where a horizontal signal summation can be performed.

The MAPP2200 chip [7] is also a 256×256 array of passive pixels which are read-out by columns. The main difference with respect to the CIVIS chip is that the column signals are directly digitized by an on-chip analog-to-digital (A/D) converter, without going through a global charge integration amplifier.

The chip in reference [4] introduced the use of active pixels in variable resolution imagers. The chip includes a 32×32 array of pixels and a 32×32 array of memories for frame or image transfer in order to enhance the ability of the chip to perform image processing tasks. The memory read-out is charge integration amplifier-based, with a structure very similar to that of the CIVIS chip: column amplifiers plus a global amplifier. However, this implementation suffers from high-residual fixed-

pattern noise due to the use of single-ended column integrators. The design was modified eliminating the memory array and using fully-differential switched-capacitor integrators for the column and the global read-out circuitry [5]. This new imager has 128×128 pixels and is suited for light-level-adaptive imaging.

The imager mentioned in Ref. 8 uses a completely different read-out scheme. It includes three capacitor banks to store the pixel reset and signal levels. These capacitor banks have interconnecting switches among the capacitors which are controlled by shift registers that indicate the number of pixels that are averaged. Then the n column signals of the selected row are averaged out by letting the charge redistribute through the n capacitors. The averaged signal is then transferred to a capacitor of the row capacitor bank. This process is done for the n rows. Afterwards the n capacitors of the row bank are connected together to obtain the averaged value which is then read-out by a correlated double-sampling scheme.

All the imagers described above show one common disadvantage: a reduction in resolution implies an increase in the global read-out time, since pixels are serially read-out. A reduction in the integration time proportional to the number of pixels to be read-out is a possible solution which is proposed for the CIVIS chip, and that also implies the use of an electronic shutter function. This solution however will produce a reduction in the image contrast which cannot be acceptable in certain type of applications.

In this paper a programmable IMAGer with AVeraging capabilities (IMAGAV-I) will be presented which is intended for averaging of different groups or sets of pixels formed by $n \times n$ kernels, $n \times m$ kernels or any group of randomly-selected pixels across the array. This imager is a 64×64 array which uses passive pixels that can be randomly accessed. The signal read-out is done by a charge integration amplifier with programmable gain which can accessed the different pixels of the array. The read-out structure is different from other imagers reported in literature that use an operational amplifier per column plus a global output amplifier. Variable resolution is possible by simultaneously reading out the selected pixels. Pixel selection can be done following two different methods, depending on the distribution of the pixels.

First, in Section 2 the IMAGAV-I prototype will be described in detailed. Section 3 will be dedicated to explain the different averaging methods that can be used. In Section 4, experimental results obtained with the imager will be presented. Finally, a summary of concluding remarks is given in Section 5.

2. THE IMAGAV-I PROTOTYPE: DESIGN AND OPERATION

The IMAGAV-I prototype has been designed in a $0.5\mu m$, twin-well, CMOS technology, with three metal layers, double poly and high ohmic polysilicon resistors. Only two metal layers have been used for routing (metal1 and metal2); metal3 has been used as a light shield and also to supply the analog negative power to the whole circuit. The technology is designed for 3.3V power supply operation (V_{DD} = 3.3V, V_{SS} = 0.0V). Independent power supply pads are provided for analog, digital and electrostatic protection circuitry. The array size is $1.529 \times 1.529 mm^2$, and the chip size is approximately $3.3 \times 5 mm^2$.

The chip microphotograph can be seen in Figure 2 where the main building blocks of the IMAGAV-I prototype are indicated. The main area is occupied by the 64×64 array of pixels. The row and column decoders are placed left and down to the array. A row multiplexer to reduce the stray capacitance of the array and the read-out circuitry are located to the right side of the chip. The prototype includes an 8-bits flash A/D converter which can simultaneously provide a digital value of the output signal, and occupies the lower right part of the chip. The A/D converter has an independent power supply, being possible to switch it OFF completely if not used.

The array consists of a regular distribution of 64×64 identical pixels, where each pixel occupies $23.9 \times 23.9 \mu m^2$ with a fill factor of 16%. Passive pixels have been included that can be randomly selected and incorporate an electronic shutter. Figure 3 shows the schematic representation of the pixel circuitry. The diode, which is reversed biased, acts as a photodetector generating a reverse current which is proportional to the irradiance (flux density [W/m^2]) on the chip surface. This current is integrated in the capacitor during a certain period of time (exposition time), resulting in a stored charge proportional to the local illuminance on the pixel. Signal *SHT* controls the switch that acts as an electronic shutter, controlling the exposition time. When this switch is conducting, the photocurrent is integrated in the capacitor. Signals *R(i)* and *C(j)* are common to row "*i*" and column "*j*", respectively. Their function is to allow random selection of a pixel, connecting the capacitor to the data line *D(i)*, which is also common to row "*i*". When a pixel is selected, the charge stored in its capacitor is transferred through the data line and the row multiplexer to the negative input node of the read-out amplifier, that converts it into a proportional voltage signal. Precharging of all pixel capacitors is performed in parallel also through the data lines *D(i)*. The precharge period is previous to exposition and is done through a separate external power supply and a switch controlled by signal *PCH* (see Figure 4). The photodiode used in this design is a diffusion/well (p^+/n^-) junction which is isolated from the substrate,

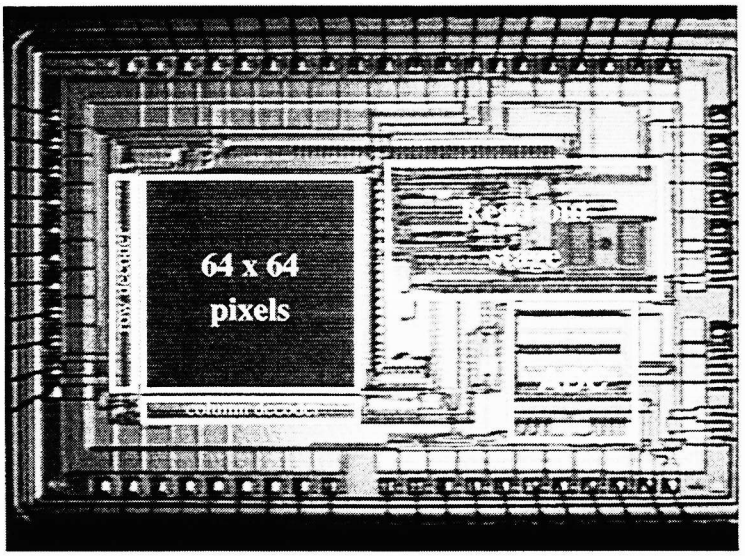


Figure 2. Chip microphotograph.

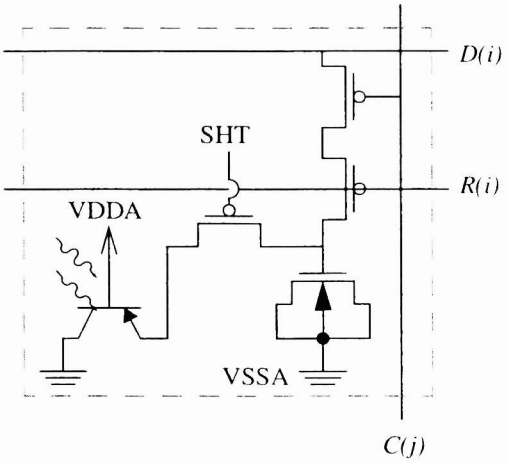


Figure 3. Schematic representation of the pixel circuitry.

therefore avoiding crosstalk between pixels, and at the same time provides an antiblooming structure through the well/substrate (n^-/p^-) junction [9]. Row and column selection switches and the shutter switch are implemented by p-type MOS transistors which have been included in an independent well to avoid influence of photo-generated carriers in the substrate. The integration capacitor is implemented by an n-type MOS transistor whose source and drain are short-circuited to VSSA.

The read-out structure includes a sole charge integration amplifier with programmable gain, which is designed to work at up to 5MHz read-out frequency. This read-out stage contributes to reduce the fixed-pattern noise observed in other imagers where the pixels are read-out using an amplifier per column. The chip can perform both averaging and binning of the signal charges depending on the selected feedback capacitor of the charge integration amplifier. The read-out process of the group of pixels can be done simultaneously and, up to a certain number of pixels, at the same read-out rate.

Figure 4 illustrates the read-out circuitry of the IMAGAV-I prototype, including the row multiplexer. The main elements are: the charge integration amplifier (called for simplicity output amplifier), a Sample-and-Hold (S/H) stage and an analog output buffer. The intermediate switch controlled by signal *MED* can be used for signal averaging in the array of pixel capacitors

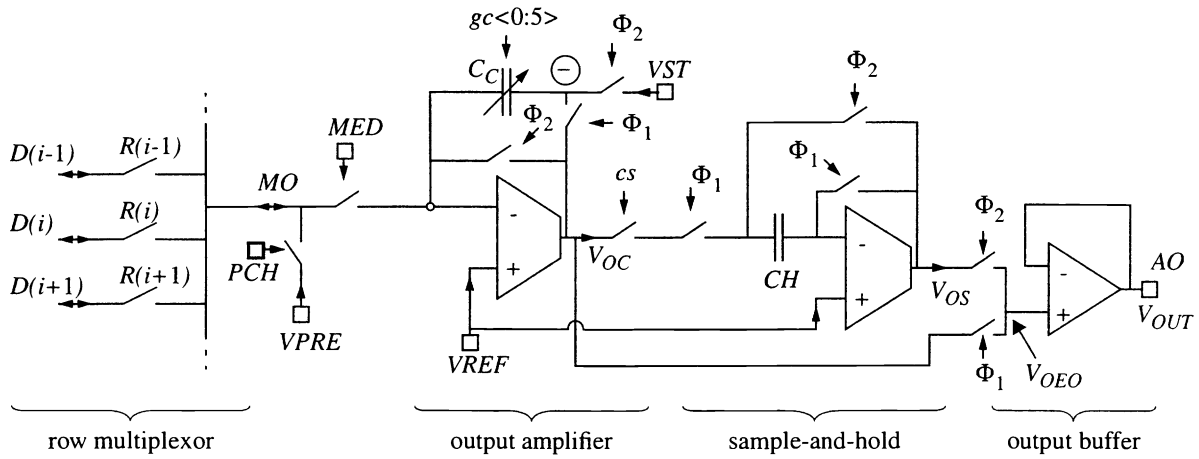


Figure 4. Symbolic representation of the read-out circuitry.

before reading out the pixels signals. The switch controlled by signal *PCH* is used for the "precharge" or reset of all the capacitors of the array of pixels. The voltage level of the precharge *VPRE* is transferred through the multiplexer and the row and column selection switches in each pixel, which are all activated for this purpose. Voltage *VPRE* determines the voltage range of the integrating capacitor in the pixel, which is given by $3.3\text{V} - VPRE$. The larger the *VPRE* value, the smaller the voltage range.

Switches controlled by signals Φ_1 and Φ_2, which are generated from an external clock signal, periodically commute to evaluate each pixel or set of pixels. Consider the output amplifier in Figure 4. Switches controlled by Φ_2 are used to reset the voltage levels of the feedback capacitor: on the one hand, the capacitor negative node (capacitor top plate) is directly set to *VST;* on the other hand, the OTA is connected in unity gain configuration so that its output node, and hence the capacitor positive node, are driven to *VREF.* The switch controlled by Φ_1 connects the output node of the OTA to the negative node of the feedback capacitor. Signal Φ_1 is in phase with the selection of rows and columns, and is during this period when the read-out process of one pixel or set of pixels is done. During the reading period, the OTA output voltage will decrease since all the charge stored in the integration capacitor of the pixel or set of pixels has been transferred to the feedback capacitor. Simultaneously, the OTA output voltage is transmitted to the output buffer in Figure 4, thereby yielding the following steady-state voltage level:

$$V_{OUT} = VST - \frac{\Delta Q}{C_C} = VST - \frac{C_{PIX}}{C_C}[VREF - (VPRE - \Delta V_{PIX})] \tag{1}$$

where ΔQ is the photo-generated charge, and ΔV_{PIX} represents the change in voltage level at the top plate of the integration capacitor due to photo-generated charge. As it can be seen, voltage *VST* is the reference level that determines the output range of the output amplifier, taking a maximum value of 3.3V. Normally, *VREF* and *VPRE* will take the same value and expression (1) can be written as

$$V_{OUT} = VST - \frac{C_{PIX}}{C_C}\Delta V_{PIX} \tag{2}$$

The sample-and-hold in Figure 4 is used to keep this level at the output during phase Φ_2.

The feedback capacitor C_C is formed by an array of capacitors which is binary programmable by a 6 bits word externally controlled by bus *gc*<0:5> (see Figure 4). The capacitor can take values from 1 to 63 times the unity capacitor *uc*, which has a value approximately equal to that of the integration capacitor in the pixel. This programmability allows to attenuate the output value when voltage saturation is observed. Whenever average is not employed, the feedback capacitor remains equal

to $1uc$. Pixel binning is also possible in low light illumination conditions by simply setting a unity capacitor as feedback capacitor and simultaneously or serially selecting the different pixels without resetting the amplifier.

The output value of the output amplifier is sampled at the end of each reading period and held by the Sample-and-Hold circuit during the reset period of the imager, in such a way that the analog output buffer transfers this voltage to a pad which can be accessed from the outside of the chip without being affected by the reset of the output amplifier. The Sample-and-Hold circuit that has been used presents the advantage of not being sensible to the offset of the OTA.

The main advantage of the IMAGAV-I prototype with respect to other imagers with variable resolution is that, when increasing the number of pixels to be read-out, the read-out rate is kept constant up to a large number of pixels. The maximum number of pixels that can be read is mainly determined by the programmable feedback capacitor of the output amplifier. In our case, and since the pixel array is of 64×64, we decided to limit this number to 64 pixels (8×8 kernels, or one column or row). However, this number could be increased by simply enlarging the capacitor array and adding a bit (or more) to the control bus *gc*<0:5>.

2.1 Pixels selection

The control of row and column selection signals is done by the row and column addressing circuits. The circuitry used to control signals *R(i)* and that used to control signals *C(j)* is identical. Therefore, we will describe them simultaneously, replacing letters "*R*" or "*C*" by letter "*X*" for the purpose of making the discussion general. These circuit blocks are called "decoders" because that is their basic functionality, although several other functions have been added to obtain the variable resolution.

Each decoder provides 64 output signals *X*<0:63>. The selection of all, none, or just one arbitrary signal can easily be done using a specific signal (e.g. ALL or NONE) and a 6 bits address bus (e.g. *SX*<0:5>). The definition of an arbitrary set of signals is not as simple.

Two methods of row- or column-set definition are provided in the prototype. First method (method A) is highly efficient in terms of hardware and speed, but is restricted to a certain type of sets which are thought to be the most commonly used. Second method (method B) is completely general, at the expense of a significant increase in the "decoder" hardware and a substantial speed reduction. Method A consists on defining the group of pixels using a 6 bits mask code. Method B is based in "accumulating" the definition of pixels or group of pixels in a serial mode. Both methods will be described in detailed in Section 3.

Figure 5 shows a logical representation of the decoding circuitry. The six blocks M introduce the masks for the definition of sets used in method A. Each block M receives one bit of the *SX*<0:5> selection bus and the corresponding bit of the *mx*<0:5> mask bus, giving two output variables BP<k> and BN<k> that take the values of the selection bit and its complementary value if *mx*<*k*> = "0", or both take the value "1" if *mx*<*k*>= "1". All six M blocks together give two buses of six bits *BP*<0:5> and *BN*<0:5>.

The signal *STRX* is a strobe and avoids possible hazards when changing the selecting address. The signal *ACCXN* activates the accumulation mode for averaging. When *ACCXN* is set to "1", the bistables SR are reset and the decoder acts in the mode A of averaging. When *ACCXN* is set to "0", the decoders are in the mode B of averaging, and the bistable SR is activated, if selected, keeping this state until a reset is done. The signal *ALLXN* simultaneously activates all the outputs of the decoder when set to "0", which is necessary for the precharge of pixels. If *ALLXN* is set to "1" the signal will not have any effect on the selection. Finally, the signal *EN* (ENABLE) enables (or disables) the outputs.

3. AVERAGING MODES

As already mentioned before, there are two methods of row- or column-set definition which determine the type of averaging operation that can be performed. Method A consists on defining the group of pixels using a 6 bits mask code. Method B is based in accumulating the definition of pixels or group of pixels in a serial mode.

3.1 Method A

Method A is based on a "normal decoder" like the one sketched in Figure 5, with signals *ALL*, *NONE*, and an address bus *SX*<0:5>. The type of sets that can be specified by method A are those obtainable by allowing some bits of the address bus to

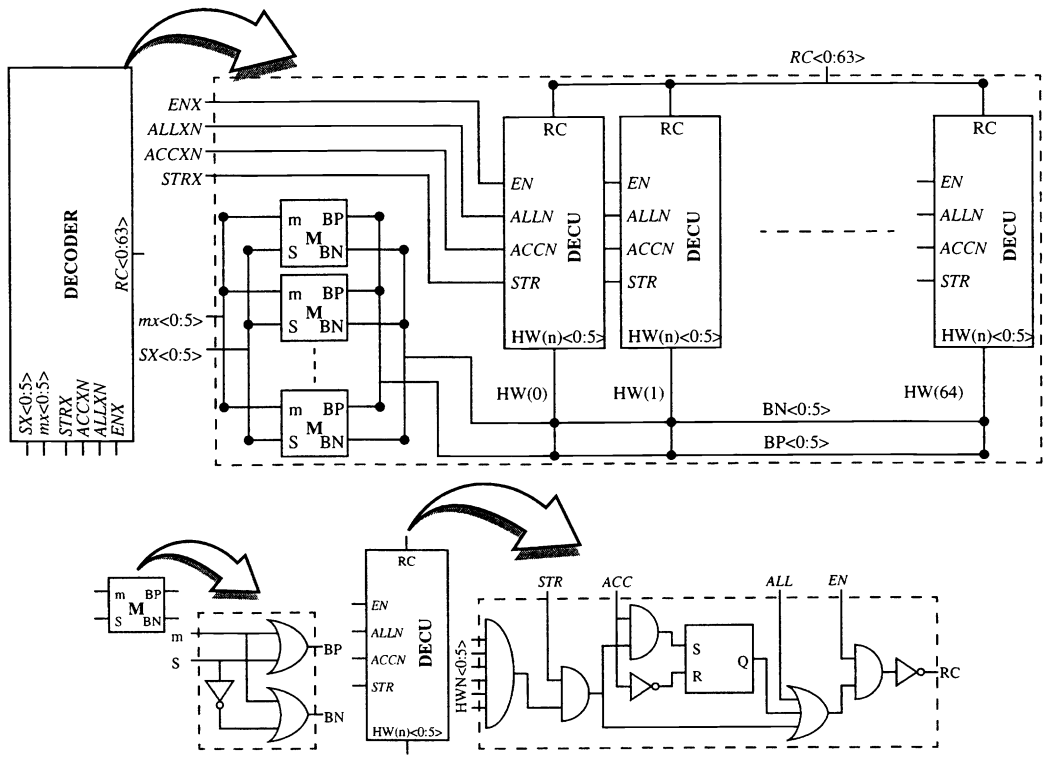


Figure 5. Logical representation of the row or column decoders. Signals *ACC* and *ALL* are the opposite to signals *ACCN* and *ALLN*.

be simultaneously "1" and "0", while the other bits have specific values ("1" or "0"). Because we need an additional mean of indicating which bits of *SX*<0:5> can be simultaneously "0" or "1", we use an additional bus called *mask bus mx*<0:5>. The set of selected rows or columns is defined by all the addresses obtained by combining the non-masked bit values of the address bus with all the possible combinations of values for the masked bits. Table 2 contains some examples of sets defined using this method.

Table 2. Examples of sets defined by method A. Letter "d" means 'do not care'.

SX<0:5>	*mx*<0:5>	DEFINED SET OF OUTPUTS		
dd.ddd1	11.1110	2n+1	n=0,1,...,31	All odd outputs: {1,3,...., 63}
dd.ddd0	11.1110	2n	n=0,1,...,31	All even outputs: {0,2,...., 62}
dd.dddd	11.1111	n	n=0,1,...,63	All outputs: {0,1,2,....,63}
00.00dd	00.0011	n	n=0,1,2,3	Only the first four outputs: {0,1,2,3}
dd.dd00	11.1100	4n	n=0,1...,15	One out of every four outputs, starting from output 0: {0,4,8,....,60}
dd.dd11	11.1100	4n+3	n=0,1...,15	One out of every four outputs, starting from output 3: {3,7,11,....,63}
dd.dd1d	11.1101	4n+m	n=0,1...,15, m=0,1	{2,3,6,7,....,58,59,62,63}
d0.1001	10.0000	32m+9	m=0,1	{9,41}

Method A is thus restricted to a certain class of sets. For example, you can define sets {0,1} and {2,3}, but not set {1,2}. On the other hand, this method has the advantage of allowing the set to be defined "in parallel", this is, in one single "clock cycle".

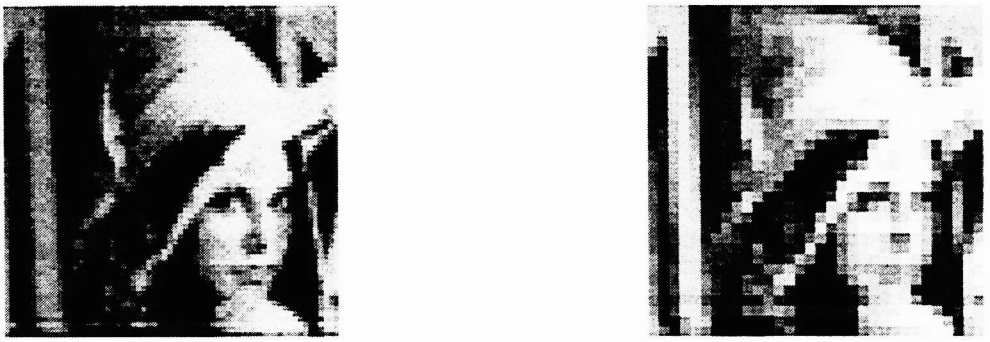
3.2 Method B

Method B is based on a sequential definition of the set. For this purpose, each output of the "decoder" contains a 1-bit memory. A typical set-definition process using method B starts with the activation of a specific external signal (*ACCXN*) which puts the decoder in accumulation mode. All output latches are initially set to "0" by the previous inactive state of the accumulation signal. One clock cycle after another, different elements (or subsets of elements) of the output set are defined using method A, which results in their corresponding latches being set to "1". An ENABLE signal allows all the outputs to be inactive during the sequential process. With the activation of the ENABLE signal, the (sequentially defined) output-signals set will be activated.

Note that the sets that can be defined with method B are always the union of subsets that can be defined using method A. Since method A includes the possibility of defining sets containing one single arbitrary pixel, method B is completely general.

4. EXPERIMENTAL RESULTS

As it has been mentioned above, the read-out stage is designed to operate at frequencies up to 5MHz when working at full resolution (reading out 1 pixel at a time). This read-out rate is not reduced when reducing the image resolution, as it can be observed in Figure 6, where an image obtained at 5MHz and at two different resolutions, 64×64 pixels and 32×32 pixels, is shown. In this case, the 32×32 pixels resolution image is obtained by averaging four pixels in a feedback capacitor which is four times larger to the unity size capacitor. In low light illumination conditions, a reduction in the resolution can



a) b)

Figure 6. (a) Full resolution (64×64) image taken at 5MHz read-out rate. (b) Same image taken at 32×32 pixels resolution. Integration time in both cases is 1.4ms

help to increase the image contrast when the feedback capacitor is set to its unity size (binning process) instead of to the number of averaged pixels (averaging process). This can clearly be observed in Figure 7, where an image taken in low light illumination conditions at full resolution (Figure 7.a) is afterwards taken at a reduced resolution, with both a proportionally larger feedback capacitor (Figure 7.b) and a unity size capacitor (Figure 7.c). The last image shows an improved contrast.

All the images included in Figure 6 and Figure 7 show a common characteristic: the very reduced fixed-pattern noise, as expected due to the use of a sole read-out stage for all the array.

Finally, Figure 8 illustrates the effectiveness of the anti-blooming structure included in the pixel design. A cable with a very bright background light is sharply imaged into the array.

a) b) c)

Figure 7. (a) Full resolution (64×64) image taken in low illumination conditions. (b) Same image taken at 32×32 pixels resolution with a four times larger feedback capacitor (averaging process). (c) Same image taken at 32×32 pixels resolution with a unity size feedback capacitor (binning process). Integration time in all cases is 15ms.

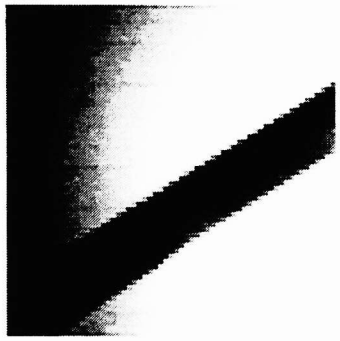


Figure 8. Image illustrating the effectiveness of the antiblooming structure.

5. CONCLUSIONS

A programmable imager with averaging capabilities has been presented which is intended for averaging of different groups or sets of pixels formed by $n \times n$ kernels, $n \times m$ kernels or independent pixels of the array. This imager is a 64×64 array which uses passive pixels with electronic shutter and anti-blooming structure that can be randomly accessed. A sole read-out stage with programmable gain is used which shows a strong reduction of the image fixed-pattern noise. Both averaging and binning of the images can be done by selecting the appropriate gain of the read-out stage. The prototype includes an analog to digital converter which provides the digital output of the images.

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REFERENCES

1. E. R. Fossum, "CMOS image sensors: Electronic camera on a chip," *Int. Electron Device Meetings*, pp. 17-25, 1995.
2. H.-S. Wong, "Technology and device scaling considerations for CMOS imagers," *IEEE Transactions on Electron Devices*, **43**, pp. 2131-2142, 1996.
3. G. Meynants, B. Dierickx and D. Scheffer, "CMOS active pixel image sensor with CCD performance," *Proceeding SPIE*, **3410**, pp. 68-76, 1998.
4. Z. Zhou, B. Pain and E.R. Fossum, "Frame-transfer CMOS active pixel sensor with pixel binning," *IEEE Transactions on Electron Devices*, **44**, pp. 1764-1768, 1997.
5. Z. Zhou, B. Pain and E.R. Fossum, "A CMOS imager with on-chip variable resolution for light-adaptive imaging," *Proceeding of the IEEE International Solid-State Circuits Conference*, pp. 174-175, 1998.
6. N. Ricquier, I. Debusschere, B. Dierickx, A. Alaerts, J. Vlummens and C. Claeys, "The CIVIS sensor: a flexible smart imager with programmable resolution," *Proceeding SPIE*, **2172**, p.2-10, 1994.
7. C. Jansson, P. Ingelhag, C. Svensson and R. Forchheimer, "An addressable 256x256 photodiode image sensor array with an 8-bit digital output," *Analog Integrated Circuits and Signal Processing*, **4**, pp. 37-49, 1993.
8. S.E. Kemeny, R.Panicacci, B. Pain, L. Matthies and E.R. Fossum, "Multiresolution image sensor," *IEEE Transactions on Circuits and Systems for Video Technology*, **7**, pp.575-583, 1997.
9. C.H. Aw and B.A. Wooley, "A 128x128-pixel standard -CMOS image sensor with electronic shutter," *IEEE Journal of Solid-State Circuits*, **31**, pp. 1922-1930, 1996.