Current-Mode Techniques for the Implementation of Continuous- and Discrete-Time Cellular Neural Networks

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***Abstract*— This paper presents a unified, comprehensive approach to the design of continuous-time (CT) and discrete-time (DT) cellular neural networks (CNN) using CMOS current-mode analog techniques. The net input signals are currents instead of voltages as presented in previous approaches, thus avoiding the need for current-to-voltage dedicated interfaces in image processing tasks with photosensor devices. Outputs may be either currents or voltages. Cell design relies on exploitation of current mirror properties for the efficient implementation of both linear and nonlinear analog operators. These cells are simpler and easier to design than those found in previously reported CT and DT-CNN devices. Basic design issues are covered, together with discussions on the influence of nonidealities and advanced circuit design issues as well as design for manufacturability considerations associated with statistical analysis. Three prototypes have been designed for 1.6-μm n-well CMOS technologies. One is discrete-time and can be reconfigured via local logic for noise removal, feature extraction (borders and edges), shadow detection, hole filling, and connected component detection (CCD) on a rectangular grid with unity neighborhood radius. The other two prototypes are continuous-time and fixed template: one for CCD and other for noise removal. Experimental results are given illustrating performance of these prototypes.**

I. Introduction

CELLULAR neural networks (CNN's) [1] consist of arrays of elementary processing units (*cells*), each one connected only to a set of adjacent cells (*neighbors*), and exhibiting potential application in different image processing tasks [2], pattern recognition [3], motion detection [4], etc. The local connectivity property makes CNN's routing easy, allowing increased cell density per silicon area and making these computation paradigms very suitable for VLSI implementation. This is more pertinent for the important class of *translationally invariant* CNN's, where all inner cells are identical, and layout is very regular. Also, since the number of different weights is very small for this CNN class, programmability issues can be easily incorporated without significant extra routing cost, by just adding several global control lines, one per weight.

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CNN properties and applications have been covered in different papers [1], [2], [4]–[9]. This paper focuses on CNN VLSI implementation, of which little literature is available [10]–[12]. For implementation purposes, analog CNN's can be classified into *continuous-time* (CT) [2] and *discrete-time* (DT) [12], [13] models. Each model type is described by a set of nonlinear dynamic equations, one per cell, whose associated equilibrium state distribution determines the network computational properties. Previously reported CT-CNN IC design approaches focused on the implementation of Chua–Yang's CNN cell circuit model [1] requiring capacitors, resistors, independent sources, and linear and nonlinear voltage controlled current sources. These implementations [10], [11] use g_m-C techniques [14] and differential-input CMOS transconductors, in a way compatible with standard CMOS technologies. Proposed discrete-time realizations focused on a very similar cell circuit model [12], where analog switches and corresponding clock controlling signals are required in addition to previous circuit elements. MOSFET-C techniques [15], [16] and fully differential high-output-impedance op-amps have been considered to implement this model [12].

There are some drawbacks to previously reported CNN implementation techniques. On one hand, input signals are voltages in all cases, while internal signals can either by voltages or currents. Since primary output of image sensor devices (*phototransistors* [17]) is current, the need arises to convert these outputs to voltage, thus complicating CNN interface design for image processing tasks. On the other hand, electrical cell design is not easy because different variation ranges for the internal voltages and currents must be considered to guarantee a reduced influence of the MOS transistor nonlinearities. Finally, operation speed is not optimum because the combination of internal voltage and current signals results in internal high-impedance nodes, and hence, large time constants.

In this paper, a unified approach is presented to implement both CT and DT CNN's using current-mode techniques, where all variables are in the form of currents. First, a new class of CNN cell models (*full range* models) is presented that allows reduced area and power consumption in VLSI implementation; then, the implementation of CNN's in current domain is discussed. Resulting cell complexity is much smaller than for previous approaches, for both the CT and the DT cases. Also, design is very simple and the speed/power figures are

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very good due to the nonexistence of internal high-impedance nodes. The full range models are covered in Section II, together with a brief summary of the CNN terminology, intended to make the paper somewhat self-contained. Section III presents the basic building blocks and the cell schematics for current mode CNN's; abstract circuit elements are used to achieve a technology independent presentation. In Section IV CMOS design issues are covered, including discussions on programmability, as well as on systematic and random error sources. Experimental results are given in Section V.

II. CNN Mathematical Models

CNN's are arrays of *locally* interconnected processing units (*cells*), arranged in the more general case on three-dimensional grids of arbitrary shape. Each generic CNN cell has three associated variables, namely:

- *Cell state:* $x^c(t)$, which conveys cell energy information as a function of time.
- *Cell output:* $y^c(t)$, obtained from the cell state via a soft-limiter nonlinear device. In the ideal model case [1] nonlinearity is *piecewise linear,*

$$y^c = f(x^c) \equiv \frac{1}{2}(|x^c + 1| - |x^c - 1|) \tag{1}$$

  though smoother *sigmoidal* approximations with unity slope at the origin are also valid.
- *Cell input:* u^c, representing external excitation.

Each cell in a CNN is excited by the outputs of a set of nearby cells located within a distance r in the grid: the cell r-*neighborhood,* $N_r(c)$, which includes cell c itself. Throughout the paper we will only consider *uniform* CNN's, where all inner cells are identical.

CNN's are signal processing units. Input signal information is conveyed by the initial state vector $\boldsymbol{x}(0) = \{x^c(0), \forall c \in \mathcal{GD}\}$ and the vector $\boldsymbol{u} = \{u^c, \forall c \in \mathcal{GD}\}$, where $\mathcal{GD}$ denotes the grid domain. Output signal information is conveyed by the output vector $\boldsymbol{y} = \{y^c, \forall c \in \mathcal{GD}\}$. Input–output mapping is determined by the net convergence to constant equilibrium states following the transient initialized by $\boldsymbol{x}(0)$ and driven by $\boldsymbol{u}$. In the rest of the paper, we will assume that internal net times are much smaller than the lowest input signal time constant, and, hence, will only consider the time variable in connection to the study of the internal network transient evolution. This evolution, as well as the equilibria encoding performed by the net, is related to the cell *dynamics,* given either in the form of a differential equation, for CT CNN's, or a finite difference equation, for DT CNN's.

Let us focus first on CT-CNN's. This paper proposes a model that differs from the Chua–Yang original one [1]. The new model is given by

$$\tau \frac{dx^c}{dt} = g[x^c(t)] + D^c + \sum_{d \in N_r(c)} \{A_d^c y^d(t) + B_d^c u^d\} \quad \forall c \in \mathcal{GD} \tag{2}$$

where summations extend over the cell neighborhood, $N_r(c)$, and $g(\cdot)$ is defined as follows:

$$g(x^c) = \lim_{m \to \infty} \begin{cases} -m(x^c + 1) + 1, & x^c < -1 \\ -x^c, & \text{otherwise.} \\ -m(x^c - 1) - 1, & x^c > 1 \end{cases} \tag{3}$$

Input (B_d^c) and output (A_d^c) weights in (2) are called *control* and *feedback* parameters, respectively, and D^c is the *offset* parameter. These parameters determine the input–output mapping performed by the net. Control and feedback parameters are, commonly, arranged into matrices (*templates*), which, for uniform CNN's, are the same for all cells. Templates for different processing tasks can be found elsewhere [2], [7]–[9]. The Appendix shows, on a table, the templates considered in this paper.

By making $m = 1$ in (3), (2) reduces to the Chua–Yang model [1]. A significant difference between both models concerns the variation range for the cell variables. For both models, output variables change inside the $[-1, 1]$ real axis interval. Value 1 corresponds to *black* in the pixel associated to the cell, while -1 corresponds to *white*.[1] On the other hand, the net input signals must fulfill, also for both models, the following normalized constraints:

$$|x^c(0)| \leq 1, \forall c \in \mathcal{GD}; \qquad |u^c| \leq 1, \forall c \in \mathcal{GD} \tag{4}$$

meaning that they have the same variation range that the outputs. Models differ in the range interval for the state variables. In the Chua–Yang model this range is larger, bounded by,

$$S = 1 + |D^c| + \sum_{d \in N_r(c)} \{|A_d^c| + |B_d^c|\} \tag{5}$$

which, for typical templates, is comprised between 5 and 10—much larger than 1. On the contrary, in the proposed model, which we call *full range* model, state variables have the same variation range than inputs and outputs, $[-1, 1]$. This is very convenient to simplify the design process and to reduce area and power consumption of CNN IC's.

As for the Chua–Yang model [1], the computational properties of the full range model rely on its ability to yield, for $A_c^c > 1$, two stable equilibrium points separated by an instability region, and in the possibility of modifying the attraction regions of the stable points by changing the cell state-variable independent term in (2),

$$I = D^c + B_c^c u^c + \sum_{\substack{d \in N_r(c) \\ d \neq c}} \{A_d^c y^d + B_d^c u^d\}. \tag{6}$$

Cell convergence is illustrated in Fig. 1, representing the $\tau(dx^c/dt)$ versus x^c characteristics, according to (2). Outer pieces have slope $m \to \infty$, while slope of the inner piece is $A_c^c - 1$. Parameter I is given by (6) and assumed constant for each trace in Fig. 1. Five different qualitative cases arise depending on the I values. As illustrated in Fig. 1, dynamic routes converge for all cases to the outer equilibria states, where $|y^c| = 1$. A detailed discussion on the proposed model

[1] These are normalized values which in actual circuits correspond to biasing signals.

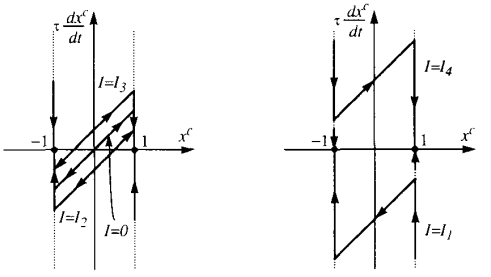


Fig. 1. Dynamic routes for the full range CT CNN model: $I_1 < I_2 < 0 < I_3 < I_4$.

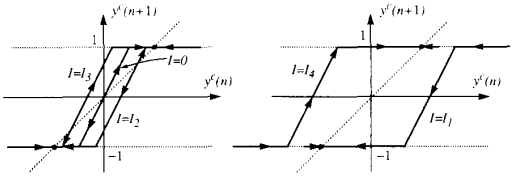


Fig. 2. Dynamic routes for the DT CNN model: $I_1 < I_2 < 0 < I_3 < I_4$.

stability properties is out of this paper's scope. However, the model has given correct results, qualitatively similar to those of the Chua–Yang model, for all the templates covered in this paper.

For sampled-data implementations, (2) must be emulated by some explicit integration algorithm. This involves a trade-off in choosing T/τ (where T denotes the sampling period): to increase speed, T/τ must be as large as possible; for stability, T/τ should be less than 2 [13]. We will use the heuristic guess of $T = \tau$, which produced correct steady states with all the templates we tried. Also, this choice allows writing the cell dynamic equation as follows:

$$y^c(n+1) = f\left[D^c + \sum_{d\in N_r(c)} \{A_d^c y^d(n) + B_d^c u^d\}\right] \quad \forall c \in \mathcal{GD} \tag{7}$$

where to ensure convergence, we require that $f(\cdot)$ be sigmoidal-like and that $A_c^c f'(0)$ be larger than 1. This can be achieved by using either a *soft nonlinearity* such as that in (1) and $A_c^c > 1$, or by using a *hard nonlinearity* (central slope infinitely large), and $A_c^c = 1$, as proposed in [12]. As for the full range CT model, all variables involved in the implementation of (7) have the same variation range, $[-1, 1]$. Fig. 2 illustrates convergence towards binary outputs for the DT-CNN model. Same qualitative cases as for Fig. 1 are considered, corresponding to different values of I in (6).

III. Basic Building Blocks for Current-Mode CNN's

Fig. 3(a) is an analog computer conceptual block diagram for a CT-CNN cell where circles indicate summation, triangles are used for signal scaling, and the other two blocks represent integration and nonlinear transformation. This diagram corresponds to the Chua–Yang model. For the full range model the

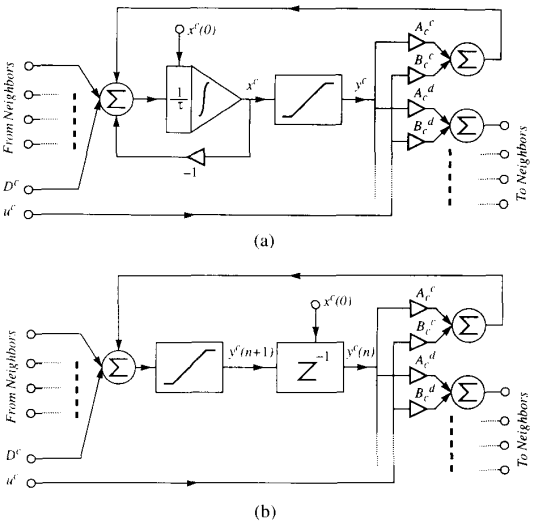


Fig. 3. (a) CT CNN conceptual cell diagram. (b) DT CNN conceptual cell diagram.

nonlinear block is eliminated and the function $g(\cdot)$ realized exploiting the output saturation of the integrator block. Fig. 3(b) shows a conceptual analog computation cell diagram for a full-range DT-CNN cell, which requires a delay instead of an integrator. Note that no weighting is performed on the neighbors' contributions at the cell input, as would correspond to (2) and (7). Instead, each cell produces different weighted output for each neighbor. To handle this, implementation templates must be obtained by interchanging entries along all radial lines in the original template matrices, as illustrated below,

$$\begin{bmatrix} a & b & c \\ d & e & f \\ g & h & i \end{bmatrix} \rightarrow \begin{bmatrix} i & h & g \\ f & e & d \\ c & b & a \end{bmatrix} \tag{8}$$

Signal *summation, scaled replication, integration, delay,* and *nonlinear transformation* are the analog operators required to implement CNN's. Summations are very easily performed in current-mode by routing currents to a common mode. Remaining operators are realized using a very simple analog building block: *the current mirror,* which yields linear currents scaling via the functional cancellation of nonlinearities between matched transconductors.

3.1. Background and Current-Mode CNN Static Operators

Current mirror concept and applications are discussed using a generic three terminal transconductor, represented by Fig. 4(a), which we assume characterized as follows:

$$\begin{aligned} i_2 &= Pu(v_1, v_2) \\ i_1 &\approx 0 \end{aligned} \tag{9}$$

where $u(\cdot)$ is assumed invertible, at least in v_1, and the characteristic is parameterized by a designer-controlled scale factor P.

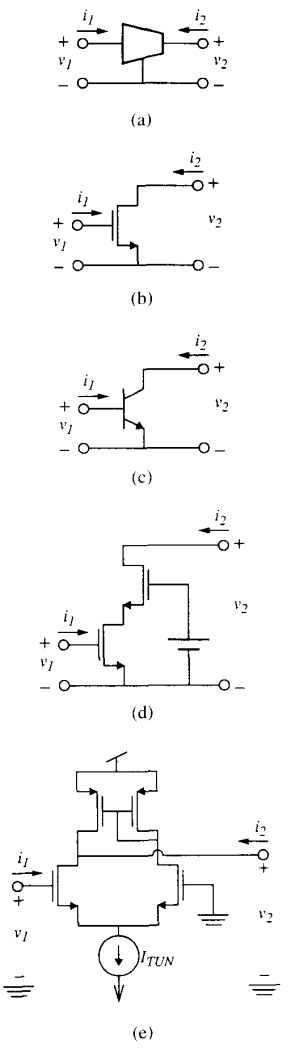


Fig. 4. (a) Generic transconductor. (b) Single MOST implementation. (c) Single BJT implementation. (d) Cascode MOS implementation. (e) Tunable implementation.

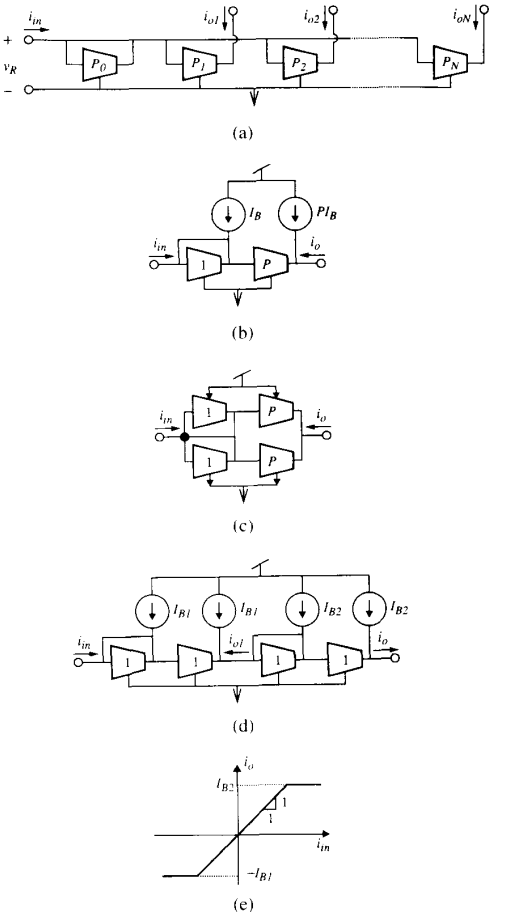


Fig. 5. Static current-mode analog operators. (a) Scaled replication. (b) Bilateral current mirror using bias shifting. (c) Bilateral current mirror using complementary devices. (d) Current reversing. (e) Nonlinear current transformation.

The generic transconductor of Fig. 4(a) may consist of either a single transistor or a more complex device containing several transistors. Fig. 4(b) and (c) shows the single MOS and BJT transconductors. Assuming operation after *pinch-off* in *strong inversion* for the MOS, and in active forward region for the BJT, (9) particularizes as

$$i_2|_{\text{MOS}} = \beta(v_1 - V_T)^2\left(1 + \frac{v^2}{V_A}\right)$$
$$i_2|_{\text{BJT}} = I_S e^{-(v_1/U_t)}\left(1 + \frac{v^2}{V_A}\right) \qquad (10)$$

where the designer controls $\beta = (K/2)(W/L)$, and $I_S = I_{SS}A_E$, by changing the channel width and length for the MOS, or the emitter area for the BJT.[2] Fig. 4(d) and (e) shows other MOS transconductor alternatives. We find convenient to use this abstract transconductor to make current mode analog operators development independent on both technology and transconductor topology.

Fig. 5(a), where each transconductor has a different parameter value, $P_i (0 \leq i \leq N)$. illustrates the basic current mirror function. Input device is feedback, while output devices are in open loop. Assuming that transconductors are matched, that their outputs are *equipotential,* and their input currents are negligible (the last holds exactly at DC for MOST), it is seen that output device nonlinearities cancel out (one by one) the nonlinearity of the input device, yielding

$$i_{ok} = \frac{P_k}{P_0} i_{\text{in}} \qquad 1 \leq k \leq N \qquad (11)$$

where P_k/P_0 can be controlled by the designer, yielding the *scaled replication* operation.

Most elementary transconductors enter a *cut-off* region, with $i_2 = 0$ in Fig. 4(a), when input voltages are below a *cut-in* value. This is the case for all devices in Fig. 4. It means that only positive currents are possible at the outputs in Fig. 5(a),

[2] $K \equiv \mu C_{ox}$ is the normalized MOS large signal transconductance and V_T is the MOS threshold voltage; U_t is the thermal voltage and V_A denotes the early voltage. V_A is controlled in MOS by the channel length [18], [19].

and, hence, that the implemented scaled replication operation is *unilateral*. For *bilateral* operation, either current shifting biasing at the input and output nodes or complementary devices must be used, as shown in Fig. 5(b) and (c), where an arrow has been added to the device symbols to differentiate complementary devices.

Circuits in Fig. 5(a)–(c) perform as *inverting* current amplifiers (assuming that input currents are positive when entering a node, while output currents are positive when leaving a node), allowing only negative weights. *Noninverting* amplification (this is, positive weights) are achieved by cascading two bilateral mirrors, as illustrated in Fig. 5(d) for unity weight. This circuit is also used to implement the *saturation nonlinearity* required for CNN's. It is achieved by using transconductor cut-off: in Fig. 5(d), for $i_{\rm in} < -I_{B1}$[3] the first mirror cuts off and current i_{o1} is supplied only by the rail, making $i_{o1} = -I_{B1}$; in a similar way, the cut-off of the second mirror makes $i_o = I_{B2}$ for $i_{\rm in} > I_{B2}$. In this manner the saturation characteristic of Fig. 5(e) is implemented.

3.2. Current Mode Dynamic Operators

Dynamic operators required for CNN's (both CT and DT) are also easily implemented by current mirrors. To understand these operators it is convenient to consider the simplified generic transconductor small-signal model shown in Fig. 6(a), where, commonly, it is $g_m \gg g_o \gg g_{\rm in}$. On the other hand, dominant reactive transconductor parasitic is typically capacitive and located at the input node, as assumed in the model of Fig. 6(a). Thus, the current mirror dynamic behavior is characterized by a finite time constant $\tau = 2C_{\rm in}/g_m$ what is used for the implementation of a current mode *lossy integrator*.

A schematic is shown in Fig. 6(b), where we have included the lossy integrator by itself (part enclosed in dashed lines) and the loading device consisting of the next mirror input. A capacitor has been added at the integrator input for more accurate control of the input time constant and to make it dominant as compared to the parasitic time constant at the output node. For analysis of Fig. 6(b) we assume a two pieces PL transconductor model (one piece for the cut-off region and the other for the conducting region), obtaining

$$\tau \frac{di_o}{dt} = i_{\rm in} + I_B g\left(\frac{i_o}{I_B}\right) \tag{12}$$

where $g(\cdot)$ is the nonlinearity proposed in the full range model, given in (3). By comparing (12) to (2) it is seen that the current mode lossy integrator saturation can be exploited for the implementation of the proposed full range CT CNN model, thereby greatly simplifying design. Nonidealities of the current-mode lossy integrator and their influence on the net operation will be discussed in Section 4.2.

Fig. 6(c) shows a circuit to achieve a *delay* in the propagation of a current, using a mirror and a clocked analog switch [20]. The parasitic input capacitor of the output transconductor is charged while the clock signal is high. When the clock signal becomes low, this charge is held at this capacitor and a *half* clock period delay is implemented:

$$i_o\left(n + \frac{1}{2}\right) = i_{\rm in}(n). \tag{13}$$

This concept is very well suited for technologies containing MOS transistors (NMOS, CMOS, BiCMOS), due to the availability of zero-offset low-leakage analog switches and high impedance transconductors. As for the lossy integrator, nonidealities of the delay block will be covered in Section 4.2.

Fig. 6(c) is a *half delay* block: sampled output currents are available during other clock phases than that during which input currents must be sampled. A *full delay* is achieved by cascading two identical half delay blocks and using nonoverlapping clock signals, as shown in Fig. 6(d). Taking into

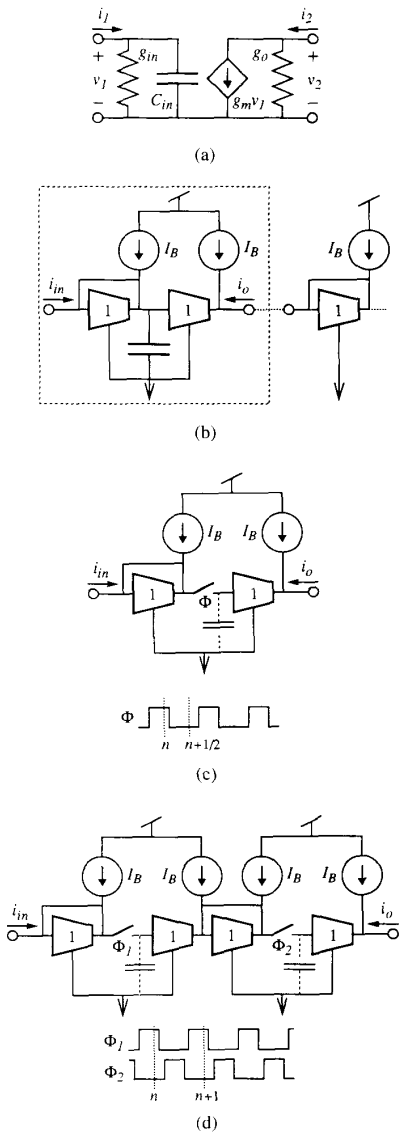


Fig. 6. Dynamic current mode CNN operators. (a) Small signal model of a generic transconductor. (b) Continuous time current mode lossy integrator. (c) Half-clock current mode delay. (d) Current mode full-clock delay.

[3] In actual circuits $i_{\rm in}$ cannot be smaller than $-I_B$, since it is limited by the device input bias current.

account transconductor cut-off, analysis of this circuit yields

$$i_o(n+1) = I_B f\left(\frac{i_o(n)}{I_B}\right). \tag{14}$$

Thus, since delay and saturation are achieved in the same device, the nonlinear block in Fig. 3(b) can be eliminated, similar to what occurs for the full range CT CNN model.

3.3. Current Mode CNN Conceptual Cell Architecture

The first step towards CNN IC design is to define the normalization factor for the output variables range. We assume the range is *symmetric* around the origin, and the rail is I_Q, so that $y^c \in [-I_Q, I_Q]$. For CT Chua–Yang CNN's, a different, wider range must be considered for the state variables, $x^c \in [-SI_Q, SI_Q]$, where S is given in (5).

Fig. 7(a) shows a generic current mode CNN cell which applies for all models in the paper. The dynamic part in this figure differs depending on the actual model considered (Fig. 7(b)–(d)). Fig. 7(a) shows only the part of the cell corresponding to the evaluation of the cell state (x^c) and the generation of output variable replicas for neighbors $(A_c^d y^c)$. Generation of scaled replicas of the input cell current (u^c) is straightforward using Fig. 5. Only two outputs per cell are included in Fig. 7(a): for positive and negative weights, respectively. Additional positive (alternatively negative) weighted outputs are obtained by using the mirror replication concept from voltage v_{RP} (alt. v_{RN}). Switches labelled S_t and $\overline{S}_t$ are used for cell initialization purposes.

Fig. 7(b) is a schematic of the cell's dynamic part for the Chua–Yang CT model. Corresponding schematic for the full range CT model is shown in Fig. 7(c). Switch R_c in both schematics is used for initialization purposes. It is seen that the full range model gives simpler circuits than the Chua–Yang model. Fig. 7(d) shows the schematic of the cell's dynamic part for the DT CNN model. Bias currents in Figs. 7(a)–(d) are obtained by replication of a master current using complementary devices, as shown in Fig. 7(e).

In the simplest case, a generic transconductor contains only one transistor. Besides, only one MOS transistor is required to implement an analog switch with zero ON offset and very low OFF leakage (about 10 pA). This infers that for this simplest case, and, for instance, for a CDD, the current-mode DT cell uses 20 transistors: this is an important advantage when compared to previous approaches for DT CNN's [12], where 106 transistors are required for a similar cell. For CT Chua–Yang CNN's, complexity (measured in number of transistors) of the current-mode circuit is similar to previous g_m-C implementations [10]. However, this complexity decreases in current mode implementations of the full range model (down to 18 for CCD).

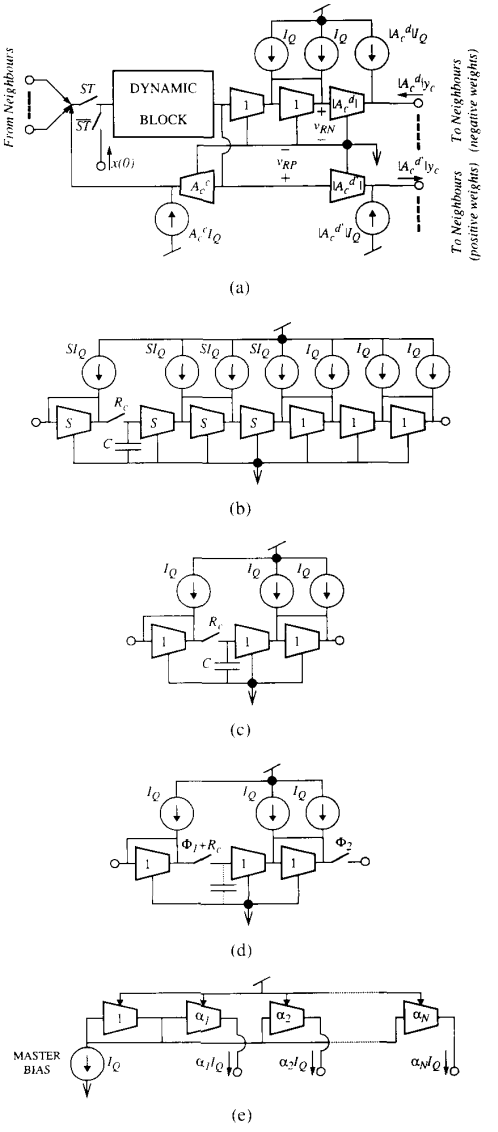


Fig. 7. (a) Generic current mode CNN cell. (b) Dynamic block for Chua–Yang CT CNN's. (c) Dynamic block for full range CT CNN's. (d) Dynamic block for DT CNN's. (e) Generating cell bias currents from a reference current.

IV. CMOS Current Mode CNN Design Issues

4.1. CMOS Mirror Schematics: Static Nonidealities and SizingEquations

Current mode CNN operation is degraded by both random and systematic sources of error. Random errors are due to statistical variations of the technological parameters across the die (mainly K and V_T in CMOS) and can be attenuated using large devices [21], careful layout [19], and proper bias generation and distribution. Systematic errors are, on the other hand, corrected by proper transconductor choice and transistor sizing.

Let us focus on systematic static current mirror errors. Fig. 8, consisting of a generic mirror and associated driving and loading devices is used to discuss these errors. We assume the device is nominally intended to yield output to input current scaling by a factor P_o/P_{in}. Two major error sources can be identified: a) Input–output voltage mismatching $(v_{\text{in}} \neq v_o)$ at the bias point, defined as the point where transconductors

TABLE I
SIZING EQUATIONS FOR CMOS MIRRORS

	Channel Widths ($W = W_n = W_p$)	Lengths	Bias Voltage
single device mirror	$W = \frac{4I_Q L_n}{V_{DD} - V_{SS} - V_{Tn})^2}\left[\sqrt{\frac{1}{K_n}} + \sqrt{\frac{\alpha_n}{2K_p\alpha_p}}\right]^2$	$L_p = \frac{\alpha_n}{\alpha_p}L_n$	
cascode mirror	$W = \frac{16I_Q}{K_n V_{Tn}^2}L_n$	$L_p = L_n$	$V_{CAS} \approx V_{SS} + 2V_{Tn}$

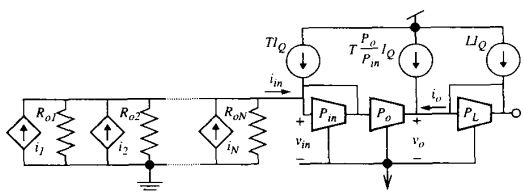


Fig. 8. Generic mirror and boundary circuitry.

sink only their bias currents, ($i_{\text{in}} = 0$); b) finite R_o/R_{in} ratios, where R_o and R_{in} represent the mirror output and input resistances.

Voltage mismatching produces current *offset* ($i_o \neq 0$ for $i_{\text{in}} = 0$), originated by the transconductor current dependence on the output terminal voltage (see (9)). For the MOS transconductors in the paper, this offset is eliminated by forcing the same current density in the mirror input transconductor and loading device, which in the case of Fig. 8 is achieved by specifying

$$\gamma = \frac{L}{P_L} = \frac{T}{P_{\text{in}}}. \tag{15}$$

This relation must hold for all transconductors (both input and output devices) in the net.

Finite R_o/R_{in} ratio causes current gain error due to spurious current division at the mirror input and output nodes. For simplicity, we shall assume the same output and input resistances for all mirrors in Fig. 8 (actually resistances depend on the current level) obtaining

$$\frac{i_0}{\sum_{j=1}^{N}} = \frac{P_0}{P_{\text{in}}}\frac{1}{\left[1 + \frac{NR_{\text{in}}}{R_0}\right]\left[1 + \frac{R_{\text{in}}}{R_0}\right]} \approx \frac{P_0}{P_{\text{in}}}1\frac{(N+1)R_{\text{in}}}{R_0} \tag{16}$$

where N is the number of mirrors driving node v_{in}. It is seen that the gain error is inversely proportional to R_o/R_{in}, and increases proportionally with N. A more precise evaluation taking into account R_{in} and R_o variations with current level also yields the same proportionality. Since N may be a large number (up to 11 for the corners and borders detection templates on a rectangular grid net with $r = 1$), the importance of the current gain error cannot be underestimated. The error is especially significant if small dimension single-transistor transconductors are used, due to the very low Early voltages associated to short channel transistors. This can be corrected by increasing device size (channel length), but this does not yield optimum area and speed for CNN implementations. For improved R_o/R_{in} figures with short channel devices, circuit strategies instead of transistor sizing should be used. In particular, the cascode transconductor of Fig. 4(d) provides optimum area and speed for given R_o/R_{in}.

Fig. 9(a) and (b) show the two CMOS mirror structures considered herein for CNN design, including the complementary devices used for biasing (separated by dashed lines). *Design parameters* are displayed in the figures: W, L_n, L_p for the simple mirror, and W, L, and V_{CAS} for the cascode mirror. Fig. 9(c) shows a circuit to provide the cascode voltage, V_{CAS}, for the cascode mirror. We assume that Early voltages are proportional to the channel length: $V_{An} = \alpha_n L_n, V_{ap} = \alpha_p L_p$. In Fig. 9(a) length of the NMOS's (L_n) is different to that of the PMOS's (L_p), which is intended to obtain equal nominal Early voltages, and, hence, optimize R_o/R_{in}. In the case of Fig. 9(b), R_o/R_{in} is intrinsically much larger and all lengths are made equal ($L_n = L_p$). For further simplicity, we have also assumed that all transistors have the same channel width, W.

Table I gives sizing equations for Fig. 9(a) and (b). These equations are intended to ensure that the mirrors handle the whole input current range with minimum distortion, and using the smallest possible devices. The W expressions given in the table correspond to a bias current I_Q; W values for larger currents are calculated taking into account the requirement for equal current density in all transconductors, given in (15).

Note that the sizing equations are parameterized by L_n, which is chosen by the designer to control R_o/R_{in} and the channel area. For Fig. 9(a), evaluation of these figures results in

$$\frac{R_o}{R_{\text{in}}} = 1 + \sqrt{\frac{K_n W L_n}{2I_Q}}\alpha_n; \qquad \text{Area} = 2WL_n\left[1 + \frac{\alpha_p}{\alpha_n}\right] \tag{17}$$

while, for the cascode mirror of Fig. 9(b), the following is obtained:

$$\frac{R_o}{R_{\text{in}}} = \frac{2WL_n}{I_Q}\left[\frac{\alpha_p^2\alpha_n^2 K_n\sqrt{K_p K_n}}{\alpha_n^2 K_n + \alpha_p^2\sqrt{K_p K_n}}\right]; \qquad \text{Area} = 8WL_n. \tag{18}$$

Fig. 10 shows the current gain error per *cell* versus the *total cell* area for a full range CT connected component detector CNN using single and cascode mirrors. Technology is a standard digital n-well 1.6-μm CMOS. Scale is logarithmic. Two families of curves are shown: the top family is for the single transistor mirror, and the bottom family for the cascode. Parameter for each family is the rail current I_Q, which varies

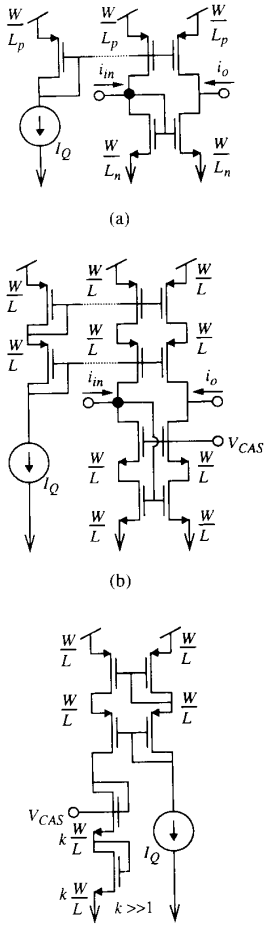


Fig. 9. CMOS bias shifted mirrors and biasing devices. (a) Simple mirror and reference circuitry. (b) Cascode mirror and reference circuitry. (c) Cascode voltage generation.

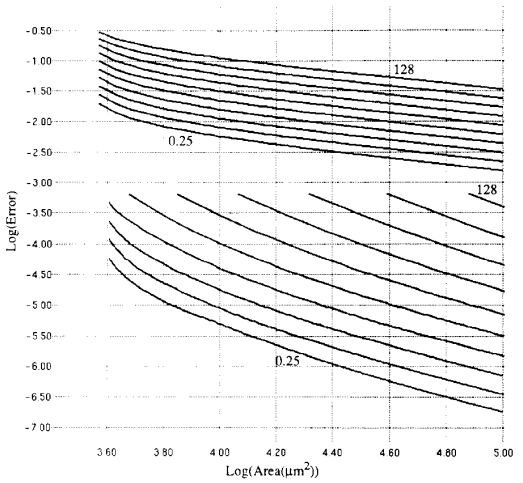


Fig. 10. Current gain relative error (per cell) versus cell area in a full range current mode CT CCD CNN cell, for different values of the rail bias current. $I_Q(\mu\mathrm{A})$ = 0.25, 0.5, 1, 2, 4, 8, 16, 32, 64, 128. Top family: Single mirror. Bottom family: Cascode mirror.

from 0.25 μA (bottom curve in each family) to 128 μA (top curves). As it can be seen, simple current mirror requires large area to achieve an acceptable error figure. On the other hand, cascode mirrors allow the use of short channel devices, and, thus result in much higher area efficiency and speed.

4.2. CMOS Current Mode Dynamic Operators Nonidealities

For illustration purposes, let us consider the current mode Chua–Yang model. Large signal analysis of Fig. 7(a) cell core (consisting of the dynamic block and self-feedback term) for MOS transconductors yields

$$\frac{dx^c}{dt} = \frac{\sqrt{2\beta(x^c + SI_Q)}}{C}\left[-x^c + A_c^c I_Q f\left(\frac{x^c}{I_Q}\right) + I\right] \quad (19)$$

which is valid for $-SI_Q < x^c < SI_Q$, for the simple and cascode mirrors, and where $\beta = K(W/L)$, and I denotes the part of the total cell input current which is not contributed by y^c (see (6)). It is seen that the time constant

$$\tau = \frac{C}{\sqrt{2\beta(x^c + SI_Q)}} \quad (20)$$

depends nonlinearly on the state variable value: transient is faster is the cell state is near the black pixel. However, the equilibrium points are exactly the same as for the nominal case, corresponding to the solution of the equation

$$h^c = -x^c + A_c^c I_Q f\left(\frac{x^c}{I_Q}\right) + I = 0. \quad (21)$$

Also, the sign of the state variable derivative (equivalently, the sign of h^c) for a given I has exactly the same dependence on x^c as for the nominal case, and, as a consequence, dynamic evolution can be expected to coincide to what is nominally expected.

Now let us consider nonidealities appearing in the CMOS current mode delay block of Fig. 6(c). Assume the analog switch consists of a single MOS transistor, as shown in Fig. 11(a), where the capacitor can consist only of parasitics. Correct operation of this circuit relies on the capacitor ability to hold the input when the analog switch turns off. Together with the unavoidable leakage current (negligible at usual clock frequencies), error arises mainly due to the necessity to evaluate the MOS channel charge during the switch turn-off process, giving

$$v_2\left(n + \frac{1}{2}\right) = v_1(n) + \frac{\Delta q}{C} \quad (22)$$

where Δq represents the part of the evacuated charge delivered to the capacitor node. This error, generically called *feedthrough error* [22], produces a large current error (up to 20% of the bias current, and more) if small geometries transconductors are used. This effect can be attenuated with several techniques. A simple choice is the inclusion of an additional capacitor at node v_2 in Fig. 11(a). Since neither linearity nor accuracy in the capacitance is required for this purpose, a shorted transistor can be used, represented by Q_1 in Fig. 11(b). This is feasible for standard digital CMOS technologies (having only one poly layer) and require less area

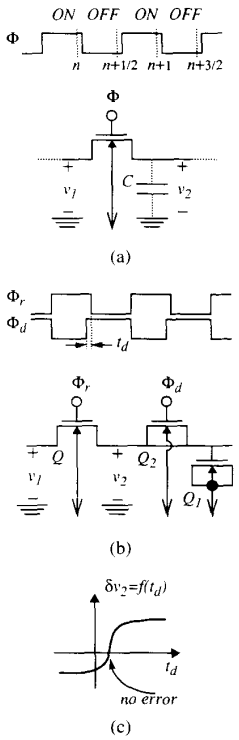


Fig. 11. (a) Storing a voltage via a simple switch. (b) Circuit strategy for feedthrough attenuation. (c) Feedthrough error versus real–dummy delay time.

than typical capacitors in two poly technologies (Poly1-SiO_2-Poly2), since channel oxide is usually thinner than interpoly oxide. The use of this technique can easily lower the error about one order of magnitude. Also, since only two of these devices are required in each CNN cell, area penalization is not severe. Much lower feedthrough error is achieved using a dummy transistor, represented by Q_2 in Fig. 11(b), and automatically tuning the delay between the switching device (transistor Q) clock signal and the dummy device clock signal [23]. In this manner errors as little as 0.3% have been measured on silicon prototypes. Also, the extra monitoring and control circuitry can be shared for all cells in the network, so that area penalty is not severe at the network level.

Note that feedthrough is also important in the CNN initialization process. Thus, this effect must also be considered for the design of CT CNN models.

4.3. Bias Current Selection: Area, Power and Reliability

A crucial issue that has not been discussed yet is the election of the bias current I_Q. Since the transistor geometry factors (see Table I), the static gain error due to finite R_o/R_{in} values, and the power dissipation, increase with I_Q, a bias current as small as possible should be chosen. The issue is to identify the minimum feasible rail current value. Lowest limit is certainly established by leakage (about 10 pA in standard CMOS). However, a more restrictive bound exists due to MOS transistor mismatch [21], [24] and Early voltage (V_A) degradation with channel length.

Mismatch is mainly produced by variations of the threshold voltages (V_T) and large signal transconductance ($\beta = KW/L$) of equally designed transistors in the same chip. Standard deviations for these parameters have two major components: one inversely proportional to the square root of the channel area, and other proportional to the device distance. Results in [21] demonstrate that the distance-dependent component is negligible for devices with a channel area less than about 100 μm^2. Since for bias currents below about 50 μA and cascode mirrors, device area calculated from Table I is well below this bound, the distance dependent component need not to be considered for current mode CNN's.

Another important consideration, for a given $\sigma(V_T)$ and $\sigma(\beta)/\beta$, the ratio $\sigma(I)/I$ in MOS transistors is inversely proportional to the gate-source voltage $v_{gs}(v_1)$ in (10)). This means that, once W/L factors have been set to achieve acceptable mismatch levels, bias current can not be decreased too far below the upper bound given by equations in Table I, since this would produce a low v_{gs} voltage at the bias point, with the corresponding high $\sigma(I)/I$. Hence, mismatch considerations establish bounds for both minimum area and power trends.

For example, we have obtained 100% success (out of 30 trials) for a Monte Carlo simulation of a connected component detector (CCD) current mode full range CT CNN with 16 cells in a row[4] (CCD template is one-dimensional, and hence there is no need to simulate a two-dimensional system). Unitary transistor geometries of $W/L = 4\,\mu\text{m}/3.2\,\mu\text{m}$ for both n and p-channel devices, and a bias current $I_Q = 2\,\mu$A were used. Further geometry reduction has not been considered, since minimum contact size (4 μm with surrounding diffusion in the 1.6 μm n-well technology used) does not allow a significant area reduction anyway.

Similar simulations performed on a Chua–Yang model counterpart using devices with the same geometries resulted in lower yield figures. This may be clarified by Fig. 12, where the nonlinear characteristics seen by the integrating capacitor are shown for different Monte Carlo trials. It is seen that normalized dispersion value of the equilibrium points (normalization factor is the distance between nominal equilibrium state positions) is much smaller for Fig. 12(a), corresponding to the full range model, than for Fig. 12(b), corresponding to the Chua–Yang model. Hence, larger geometries should be used for increased yield with this last model.

In the previous Monte Carlo simulations, global biasing voltages (bias stage is also simulated) are used for current reference generation. Dispersion due to mismatch among transistors of different current sources did not produce critical results. Thus, global biasing is a fair approach. Nevertheless, when high noise levels are expected at bias voltages, as may be the case in DT implementations, an independent current reference [25], shown in Fig. 13, can be included in each cell. Monte Carlo simulation of an entire CCD system in which

[4] All simulation results referred to in the paper correspond to full device level simulation on schematics extracted from the net layout and using level 2 transistor models with parameters provided by the foundry. The technology used is a standard direct wafer writing 5 V 1.6 μm n-well 2-metal 1-poly CMOS.

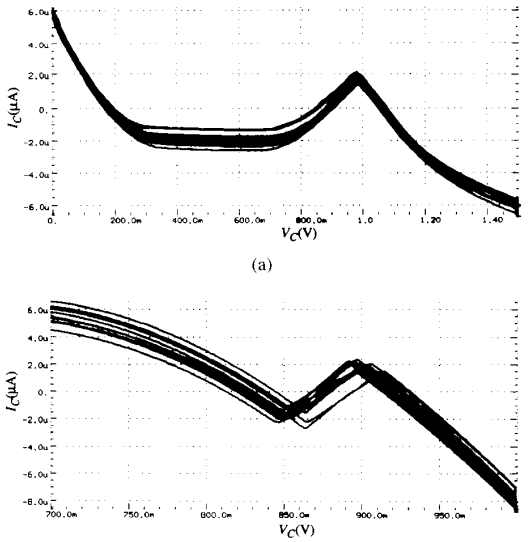


Fig. 12. Different Monte Carlo trials for the I–V characteristic at the capacitor of a CT current mode integrator in a CCD CNN cell. (a) Full range model. (b) Chua–Yang model.

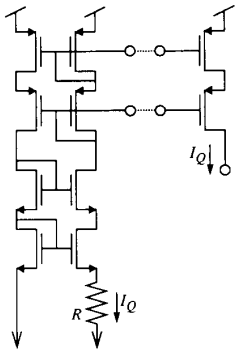


Fig. 13. Bias and threshold voltage independent current reference [Greg86].

cell current references have a standard deviation larger than 5% have shown 100% success.

4.4. Input–Output Strategy

Efficient input–output (I/O) interfacing is the strongest obstacle limiting usability and testability of CNN chips. To make design feasible for medium complexity circuits, I/O strategies other than parallel cell loading and/or downloading through bonding pads must be considered.

When input data is in optical form, using CMOS compatible *photosensor devices* [17] allows full parallel cell loading with no pinage cost. Output signals provided by photosensors are in the form of current, and thus easily connected with the proposed current-mode cells. Also, since in most application cases either $x^c(0)$ or u^c do not convey signal information, only one photosensor per cell is required.

Regardless of whether the initialization process is parallel or serial, some control circuitry must be included inside each cell to isolate this process from the net computation process. In the fully parallel input case this is handled very easily by using one global signal, St. to control the switches in Fig. 7. The switch labelled Rc in the CT dynamic blocks (Fig. 7(b) and (c)) is not required in this parallel case (switch must be shorted). For the DT cell (Fig. 7(c)), clock signals must be disabled, and kept at a high state, while St is high.

Serial cell loading requires more involved control circuitry: local logic must be included in each cell, and additional control signals must be employed. Local logic can be implemented by serial/parallel switches, to avoid noise coupling from switching digital gates. Serial loading confronts also the designer with important electrical issues related to the need to maintain each cell state and input, while remaining cells are initialized. To reduce errors due to MOS channel charge injection, the attenuation techniques discussed in Section 4.2 can be used.

Net downloading processes must be performed serially in the more general case, and hence, local logic and control signals are also required. However, this additional circuitry can be basically the same as that used for initialization. Since downloading can be performed while the network remains in operation (with the help of an additional output replication branch), leakage and charge injection errors are not of concern in this case.

For instance, Fig. 14(a) and (b) show the cell schematic and layout of a CT full range CCD cell for parallel loading and downloading, including I/O circuitry. As way of example, Fig. 15 depicts a high level diagram of a CNN chip with a cell-by-cell loading and downloading strategy. Only 8 external pins are required (6 if digital and analog supplies share the same pin).

If input signals are binary, current mode CNN chips can be tested with digital equipment. For this purpose, input and output signals must be voltages. Fig. 16(a) shows a simple binary V-to-I converter, which is used to interface test equipment with network input. This circuit is also used for offset terms and border cell contributions. Output I-to-V transformation can be done either using a simple CMOS inverter, or the faster current comparator of Fig. 16(b) [26].

4.5. Area Evaluation for Current Mode CNN's

Table II gives the transistor count and total cell area for the different templates in Appendix A, and for both CT models. Cascode mirrors with $W = 4\,\mu$m and $L3.2\,\mu$m are used (bear in mind that for these dimensions yield of the implementations based on the Chua–Yang model is lower than that for the full range model). For DT implementations area is slightly larger than those for the full range CT model, due to the switches. Network layout is simplified by including in each cell the global lines for power supplies, biasing, control and data path. These lines may use metal-2 over the cell area, which allows a significant increase in pixel density. Connections with neighbor cells can also be laid-out in such a way that cells interconnect by abutment. This eliminates tedious routing at the network layout level.

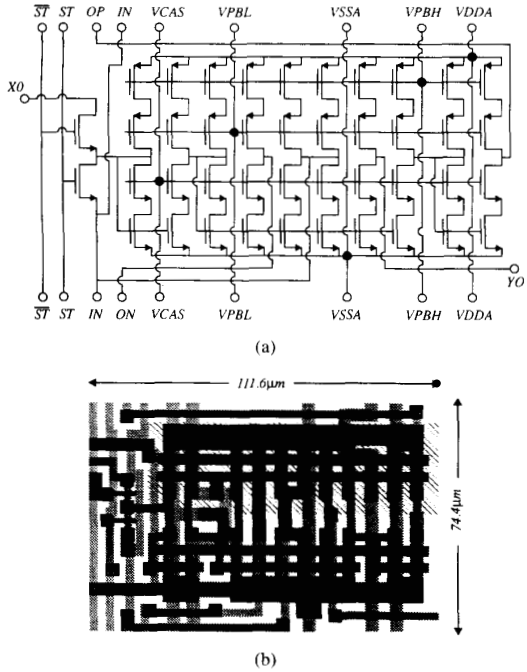


Fig. 14. (a) Complete schematic of a CT FR CCD cell for parallel loading/unloading. (b) Layout of the cell.

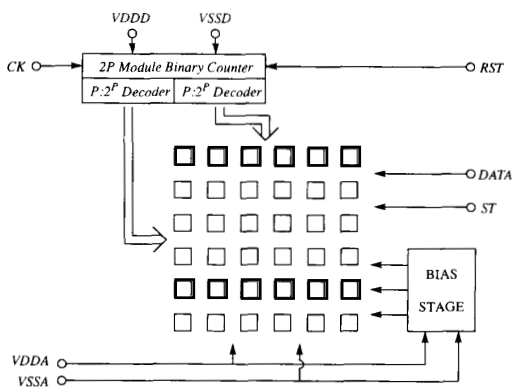


Fig. 15. Architecture of a serial I/O CNN chip with required external connections.

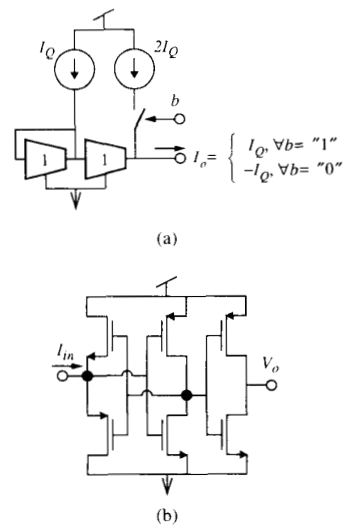


Fig. 16. (a) One bit voltage to current converter with $\pm I_Q$ output. (b) High resolution current comparator [Domi92].

TABLE II
CELL AREA AND TRANSISTOR COUNT FOR DIFFERENT TEMPLATES AND CNN MODELS

	Full Dynamic Range Area (μm^2)	Chua–Yang Model Area (μm^2)	Full Dynamic Range Ttor. Count	Chua–Yang Model Ttor. Count
C.C. Detec.	5916	12691	40	56
Shadow Detec.	7736	16533	52	68
Borders Extrac.	15471	26291	112	128
Corners Extrac.	16381	28212	120	136
Hole Filling	10921	24774	76	92
Noise Filtering	5460	14258	40	56

Although data in Table II do not include the area occupied by the initialization circuitry, approximate pixel-densities ranging from 60 to more than 160 cells/mm^2 can be easily achieved (depending on the particular template) if the full range model is used.

4.6. Programmability Issues for Current-Mode Blocks

Although fixed weight CNN chips can be useful as standalone units for dedicated image processing tasks, programmability is an important system level feature for general purpose CNN IC's. In current-mode domain two different approaches to programmability can be considered depending on the nature of the associated controlling signals: discrete programmability, where controlling signals are digital, and continuous programmability, where controlling signals are analog. Discrete programmability can be incorporated in a very simple way, by analog multiplexing of current contributions from different mirrors. These mirrors can either implement fixed templates (with application, for instance, in cases where well-defined tasks must be sequentially performed, as in [27] and [28]), or be binary-weighted (for more general application). Discrete programmability provides ease of controllability and accurate results, at the cost of strong area penalty.

For reduced area and continuous weight adjustment, analog programmability should be considered. A simple way to achieve analog programmability is using tunable transconductors, as the one shown in Fig. 4(e). Fig. 17 shows a programmable current mirror using this transconductor. Two different situations arise depending on whether transistors operate in weak or in strong inversion. Analysis for both

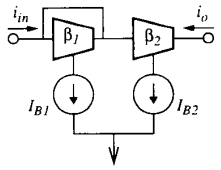


Fig. 17. Programmable current mirror using tunable transconductors.

operating conditions shows the following:

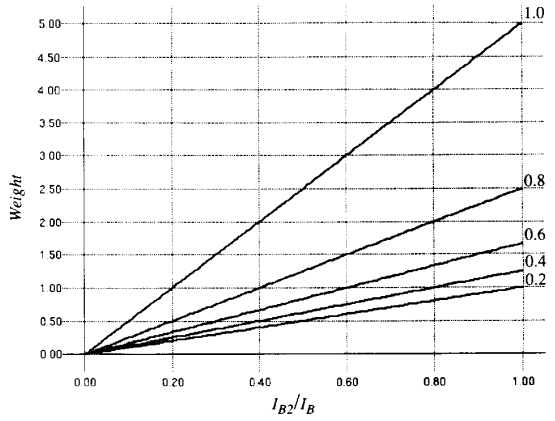
$$\left.\frac{i_o}{i_{\text{in}}}\right|_{\text{strong}} = \sqrt{\frac{\beta_2 I_{B2}}{\beta_1 I_{B1}}} \qquad \left.\frac{i_o}{i_{\text{in}}}\right|_{\text{weak}} = \frac{I_{B2}}{I_{B1}}. \tag{23}$$

As can be seen, the dependence is linear for weak inversion; hence, this latter case provides larger weight adjustment ranges. It is illustrated in Fig. 18, showing the current weight as a function of I_{B2}/I_B for different values of I_{B1}/I_B, where I_B is a normalization factor of value 10 nA for weak inversion (Fig. 18(a)) and 50 μA for strong inversion. Also, nonlinearity cancellation is exact in weak inversion due to the exponential nature of current to voltage characteristics, while it is only approximate for strong inversion: nonlinearity in the weak inversion case is less than 1% up to i_o/I_{B2}, while the corresponding value for strong inversion is $i_o = 0.13 I_{B2}$. Drawbacks of weak inversion are low accuracy, due to mismatch, and reduced speed. These can be overcome by using CMOS compatible lateral BJT's [29], which exhibit exponential feature for larger current ranges, and with excellent matching properties [30]. Other alternatives for tunable CMOS current mirrors are found elsewhere [31], [32].

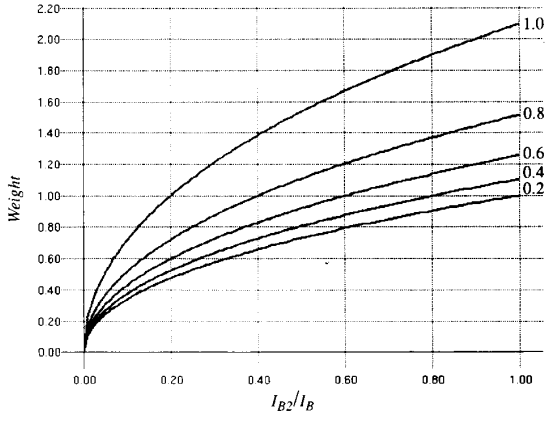
V. Practical Results

Several prototypes have been designed in a 1.6 μm 2-metal 1-poly n-well CMOS technology (within the EUROCHIP framework). One corresponds to a reconfigurable 9×9 DT CNN prototype which is conceived as a general purpose vehicle for CNN chip demonstration and test. Reconfigurability is achieved via local logic, allowing the circuit to implement the templates for noise removal, feature extraction (borders and edges), shadow detection, hole filling, and CCD, on a rectangular grid with $r = 1$. Rail current used in the prototype is 10 μA. Switches are implemented using minimum dimension n-channel transistors. Dummy transistors, also with minimum dimension, are used for adaptive feedthrough cancellation [23]. No feedthrough cancellation capacitor is used. Clock frequency is 5 Mhz. Serial loading/downloading process on a cell by cell basis is used. Due to the incorporation of programmability and reconfigurability issues, as well as other issues related to manufacturability evaluation (for instance, biasing currents can be generated either locally, using a bias circuit per cell, or globally, using a master bias), cell dimension for this prototype is very large: $500\,\mu\text{m} \times 500\,\mu\text{m}$.

Fig. 19 shows a measurement of the cell nonlinearity for this prototype. Inversion in the measured characteristics is due to the sign convention for the measurement system (HP4145B semiconductor parameter analyzer). Linearity is excellent (less than 1% deviation) over the whole input current range, and



(a)



(b)

Fig. 18. Weight (i_o/i_{in}) variation with I_{B2}/I_B for different values of I_{B1}/I_B in Fig. 17. (a) Transconductors operating in weak inversion, $I_B = 10$ nA. (b) Transconductors operating in strong inversion, $I_B = 50\,\mu$A.

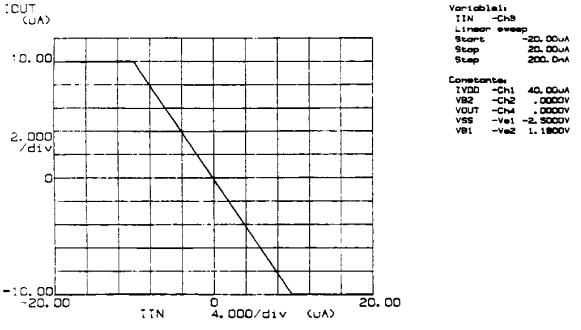


Fig. 19. Cell nonlinearity measured from a silicon prototype.

nonlinearity is quite abrupt. Measured R_o/R_{in} is 44×10^3. On the other hand, measurements of the delay block shows that the proposed feedthrough cancellation technique yields errors below 0.3% of the rail current, much better than needed for CNN.

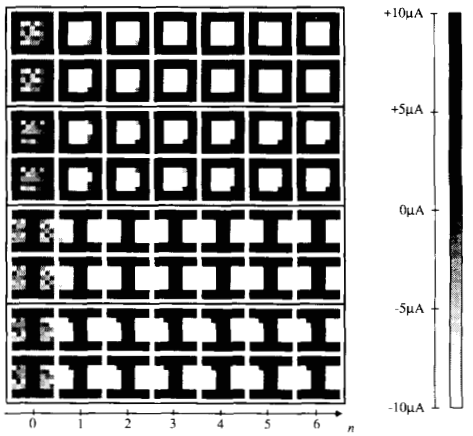


Fig. 20. Empirical results for the DT prototype configured for noise removal: Four cases with different input images (a, b, c, d). In each case, top row corresponds to numerical simulation, and bottom row to device level 2 electrical simulation.

Fig. 20 shows experimental results obtained if the DT prototype is configured for noise removal. These are HSPICE simulations of layout extracted netlists using level-2 MOST models. Four different images are considered. For each image, Fig. 20 shows the corresponding ideal and experimental result. In this figure different gray levels are assigned to the different current levels, according to the scale included on the right in the figure. It is seen that results provided by the circuit coincide with that anticipated by the ideal model. Each column in the figure corresponds to a discrete time instant, starting from the instant $n = 0$, on the left, in which the net is initialized. Noise-to-signal power ratio for all input images was 1/3. Convergence is achieved in about four clock cycles, which corresponds to about 1 μs computation time. Similar results are obtained for the different templates provided by the DT reconfigurable prototype.

The other two prototypes are continuous-time and fixed template: one for CCD (1×16) and other for noise removal (9×9). Noise removal prototype uses the full range CT model with $I_Q = 2\,\mu$A, cascode transistors, and $L = 3.2\,\mu$m. Experimental results look very similar to that in Fig. 20, convergence time being about 0.25 μs. Here we include results only for the CT CCD prototype. This actually consists of two prototypes: one made according to the Chua–Yang model and other using the full range CT model. Parallel loading/downloading processes through bonding pads are used. Internal current replicators are used to achieve simultaneous initialization of both prototypes from the same input bonding pads. A control signal is used to connect output bonding pads to either the outputs of one prototype or the other. Rail current is 2 μA in both cases, and $S = 5$ (see Fig. 7(b)) for the Chua–Yang model prototype. Although Monte Carlo analysis gives lower yield for the Chua–Yang model prototype in case $L = 3.2\,\mu$m is used, we decided to use this geometry for both prototypes, to obtain experimental evidence of the yield reduction. Minimum dimension n-channel switches are used for cell initialization. Cell areas are close to those

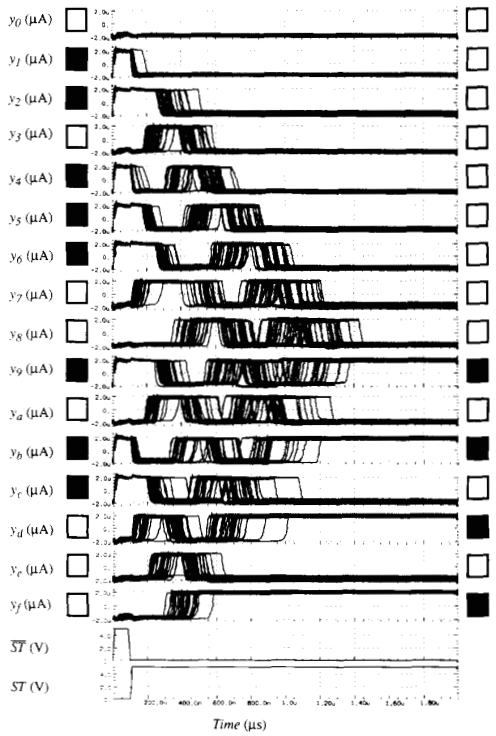


Fig. 21. Monte Carlo results for the CT full range CCD prototype.

given in Table II. No feedthrough cancellation technique is required.

Fig. 21 illustrates the transient evolution of the full range prototype for the input state shown on the left. The correct final state, shown on the right, is obtained for 30 different Monte Carlo trials corresponding to random variations of the technological parameters in the full device level layout simulations performed. The superposition of signals obtained at each cell output for the different trials are shown in the middle figures. The last two signals in this set are the net initialization signals. It is seen that convergence at the final state is achieved in 1.5 μs for the worst case (nominal value is 1.1 μs).

VI. Conclusions

Current mode provides powerful tools for the analog implementation of CT and DT CNN's. Large cell densities with good yield are achieved by using proper models and circuits.

- Full range CNN models, allowing all cell variables to have the same variation ranges and, hence, better area and power consumption figures.
- Intrinsic functional nonlinearity cancellation, giving technology independent circuits and architectures, and allowing the simplification of the IC design process.
- Cascode transistors, to reduce static error terms without area and speed penalization.
- Careful consideration of electrical issues related to net architecture and input/output interfacing.

TABLE III
CNN TEMPLATES

Function	$[A_d^c]$	$[B_d^c]$	D	Input State	Border Cells
Noise Removal	$\begin{bmatrix}0&1&0\\1&2&1\\0&1&0\end{bmatrix}$	$\begin{bmatrix}0&0&0\\0&0&0\\0&0&0\end{bmatrix}$	0	$x^c(0)$ = image u^c = do not care	$x^c = 0$ u^c = do not care
Hole Filler		$\begin{bmatrix}0&0&0\\0&4&0\\0&0&0\end{bmatrix}$	-1	$x^c(0) = +1$ u^c = image	
Corners Extraction			-2.8		
Borders Extraction	$\begin{bmatrix}0&0&0\\0&2&0\\0&0&0\end{bmatrix}$	$\begin{bmatrix}-0.25&-0.25&-0.25\\-0.25&2&-0.25\\-0.25&-0.25&-0.25\end{bmatrix}$	-1.8	$x^c(0)$ = image u^c = image	x^c = do not care $u^c = -1$
Shadow Detector	$\begin{bmatrix}0&0&0\\0&2&2\\0&0&0\end{bmatrix}$	$\begin{bmatrix}0&0&0\\0&2&0\\0&0&0\end{bmatrix}$	0	$x^c(0) = +1$ u^c = image	$x^c = 0$ u^c = do not care
Connected Component Detector	$\begin{bmatrix}0&0&0\\1&2&-1\\0&0&0\end{bmatrix}$	$\begin{bmatrix}0&0&0\\0&0&0\\0&0&0\end{bmatrix}$	0	$x^c(0)$ = image u^c = image	$x^c = \pm 1$ x^c = do not care

For CMOS technology, current as low as 2 μA can be used with reasonable yield, if strong inversion is used. Speed for these low current levels is optimum (about 1 μs for 16 cells CCD) due to the small device dimensions and the low impedance of internal nodes. Electrical tunability can be easily incorporated using electrically parameterized transconductors, for instance, differential amplifiers. Digital tunability is direct by switching lines rooted to common nodes. Delay templates are in this way easily incorporated. Summarizing, results in this paper demonstrate the feasibility of high density, high-speed CNN's in standard digital technologies; also, the new CNN mathematical model provided opens new vistas for the development of CNN IC's.

APPENDIX

See Table III.

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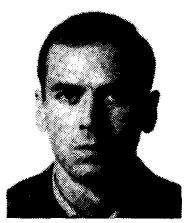

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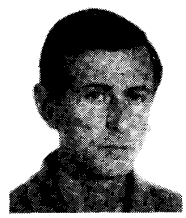

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