An Ultralow-Power Mixed-Signal Back End for Passive Sensor UHF RFID Transponders

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***Abstract*—This paper describes the design of mixed-signal back end for an ultrahigh-frequency sensor-enabled radio-frequency identification transponder in full compliance with the Electronic Product Code Class-1 Generation-2 protocol, defined in the standard ISO 18000-6C. The chip, implemented in a low-cost 0.35-μm CMOS technology process, includes a baseband processor, an analog-to-digital converter (ADC) to digitize the signal acquired from the external sensor, and some auxiliary circuitry for voltage regulation and reference generation. The proposed solution uses two different supply voltages, one for the processor and the other for the mixed-signal circuitry, and defines a novel communication protocol between both blocks so that analog readouts are minimally affected by the digital activity of the tag. The whole system was first functionally validated by exhaustively testing with external dc power supplies ten prototype samples, and then, the two main blocks, processor, and ADC were individually tested to assess their performance limits. Regarding the baseband processor, experiments were performed toward the calculation of its packet error rate (PER) under two typical biasing configurations of passive tags, using either crude clamps or regulators. It was found that the regulated biasing outperforms the clamping solution and obtains a PER of 3×10^{-3} with a supply voltage of 0.75 V. The current consumption of the processor during the reception and response to a *Read* command at maximum backward rate is only 2.2 μA from a 0.9-V supply. Regarding the ADC, it is a 10-b successive approximation register converter which obtains 9.41 b of effective resolution at 2-kS/s sampling frequency with a power consumption of 250 nW, including the dissipation of a current generation cell and the clock generation circuitry, from 1-V supply.**

***Index Terms*—Baseband processing, Electronic Product Code (EPC) Class-1 Generation-2 (Gen2) protocol, ISO 18000-6C, low-power design, passive transponder, radio-frequency (RF) identification (RFID), sensor interface, successive approximation register (SAR) analog-to-digital converter (ADC) (SAR-ADC).**

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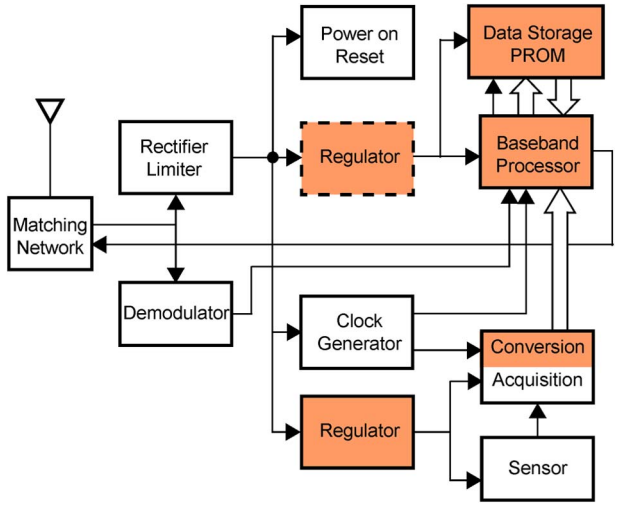

Fig. 1. Block diagram of a sensory tag.

I. Introduction

THE abilities of sensor-enabled radio-frequency (RF) identification (RFID) transponders (sensor tags, in short) to monitor, record, and even react to ambient conditions are expected to promote a new world of applications far beyond a simple barcode system replacement [1]–[3]. In these tags, the information delivered to the reader may not only consist of identification data [4], [5] but also contain environmental readouts (e.g., temperature, pressure, and optical or chemical variables) obtained from an accompanying sensor.

Nowadays, there are not many manufacturers who offer tags with sensor functionality, and most often, solutions are active or semipassive [6], [7]. However, to take full advantage of the RFID technology in terms of device autonomy, small form factor, and low price, passive tags have to be targeted. Contrary to their active counterparts, passive tags have no internal power source available, but they are remotely biased by the reader by means of an on-chip RF-to-dc conversion stage [8]–[13].

Fig. 1 shows the basic block diagram of a passive sensor tag [8]–[13]. The RF-to-dc converter is implemented by a set of rectifiers and limiters which, together with voltage regulators, provide stable supplies for all the blocks of the tag, including the attached sensor. A power-on reset (POR) circuit monitors the voltage at the RF-to-dc converter and determines if its output has reached a suitably high voltage level to reliably power the tag. In such a case, the POR circuit provides the

initial logic signal to enable the baseband processor. Otherwise, it stops the entire digital system to prevent unpredictable behavior or transmission of erroneous data. In the signal path, the demodulator extracts the binary instructions to be handled by the baseband processor from the incoming RF signal. A self-oscillating clock generator, enabled by the POR circuit, defines the master frequency of the tag. Backward communication to the reader is accomplished by modulating the amplitude and/or the phase of the RF carrier by means of a switchable antenna matching network driven by the baseband circuitry. Specific to sensor tags, a signal conditioning circuit, including an analog-to-digital converter (ADC), is used to acquire the physical variable measured by the sensor. The conditioning circuit and the sensor itself are supplied by a dedicated regulated voltage to avoid perturbations from the digital activity of the processor.

Because of the scarce supplying conditions, power consumption minimization is a priority for passive tags in general and sensor ones in particular as of the additional resources required by the sensor circuitry. Another important challenge of passive sensor tags is to define a reliable protocol between the signal conditioning circuitry and the baseband processor of the tag, so that sensor readouts can be robustly transferred and processed.

This paper addresses both challenges and presents the design of the baseband processor, data-conversion stage, and other auxiliary blocks (shaded elements in Fig. 1) of a passive ultrahigh frequency (UHF) sensor tag for half-duplex communications in the 860–960-MHz range. The design has been conceived as a multipurpose platform not tied to a particular sensor device. Hence, any eventual signal transduction required by the sensor to provide its output in voltage form is assumed to be realized off-chip. Despite this limitation, which must be anyhow balanced with the multipurpose feature of the solution, the proposed procedures and techniques can be likewise applied to any arbitrary sensor-enabled tag with on-chip sensors.

The proposed design, implemented in a low-cost 0.35-μm CMOS technology, targets the Electronic Product Code (EPC) Class-1 Generation-2 (Gen2) protocol [14], included in the standard ISO 18000-6C [15], which is briefly reviewed in Section II. The architecture of the baseband processor is presented in Section III, and Section IV describes its timing control unit which supports many of the low-power design strategies implemented in the chip. Section V presents the protocol used for the communication between the processor and the data-conversion stage. It also briefly describes the design of the converter, a rail-to-rail 2-kS/s 10-b successive approximation register (SAR) ADC (SAR-ADC). Next, Section VI shows the experimental results which confirm that the processor is fully functional, meets the packet error rate (PER) specifications of the available regulations, and is able to tolerate master clock frequency deviations as high as 15% from the nominal. This is demonstrated for two different biasing circuits, either using a dedicated voltage regulator or a programmable supply capacitor, for comparison purposes. The baseband processor only consumes 2.2 μA at 0.9-V supply using a supply voltage regulator, and the SAR-ADC obtains 9.4 b of effective resolution [effective number of bits (ENOB)] for 1-V supply with only 250 nW of power consumption. Finally, Section VII gives some concluding remarks.

TABLE I
EPC Gen2 COMMANDS

Category	Command	EPC Code	*cmd_ID*
Inventory	*QueryRep*	00	0001
	ACK	01	0010
	Query	1000	0011
	QueryAdjust	1001	0100
	NAK	11000000	0101
Select	*Select*	1010	0110
Access	*ReqRN*	11000001	0111
	Read	11000010	1000
	Write	11000011	1001
	Kill	11000100	1010
	Lock	11000101	1011
	Access	11000110	1100

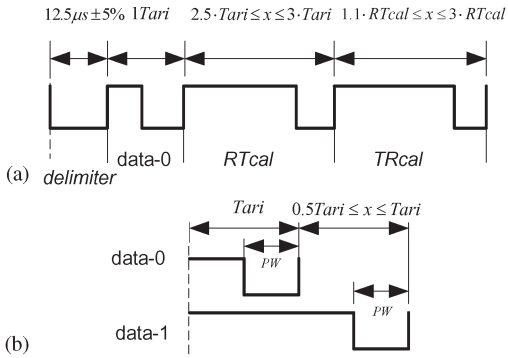

Fig. 2. (a) Preamble used in reader-to-tag signaling during a *Query* command. (b) Data encoding in PIE format.

II. EPC Gen2 REVIEW

The EPC Class-1 Gen2 protocol [14] is a highly flexible RFID protocol which allows for the transmission of simple commands between reader and tags. These instructions are listed in Table I together with their identification codes. They are grouped into three categories (*Select*, *Inventory*, and *Access*) related to the different phases along an RFID communication. All these commands have been fully implemented in the proposed baseband processor.

Reader-to-tag communications are always preceded by a preamble. Fig. 2(a) shows an example, corresponding to a *Query* instruction. The preamble comprises a fixed-length *delimiter*, a *data*-0 symbol, a reader-to-tag calibration symbol (*RTcal*), and a tag-to-reader calibration symbol ($TRcal$). These two latter symbols are used to define the forward (reader-to-tag) and backward (tag-to-reader) data rates, respectively. The duration of $RTcal$ is equal to the length of a *data*-0 symbol plus the length of a *data*-1 symbol, both shown in Fig. 2(b). These symbols define the pulse-interval encoding (PIE) format used for reader-to-tag signaling.

The data rates of the backward link (which may amount from 5 to 640 kb/s) are obtained by dividing the master clock

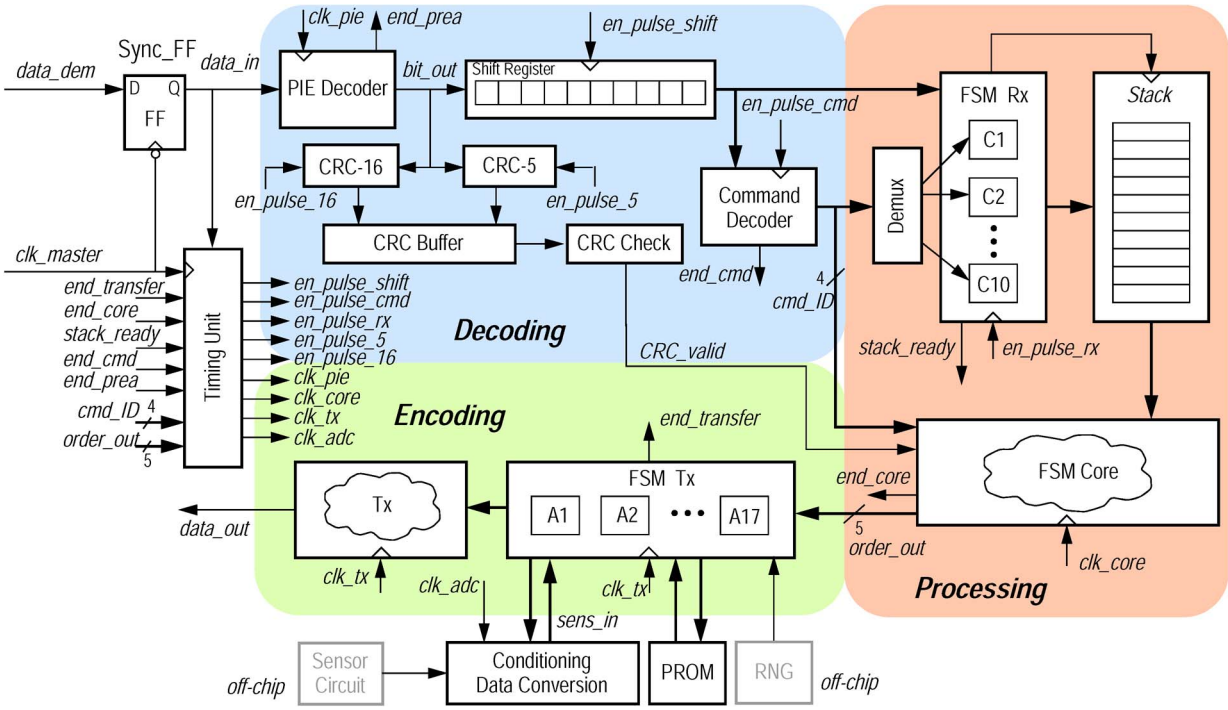

Fig. 3. Architecture of the proposed baseband processor.

frequency by integer values. The number of clock cycles per bit in the backward link N_{BLF} is therefore computed as

$$N_{\mathrm{BLF}} = round\left\{\frac{\mathrm{int}(TRcal \cdot f_m)}{DR}\right\} \tag{1}$$

where the divide ratio DR specified in the *Query* command can be 8 or 64/3, f_m is the master clock frequency, and $\mathrm{int}(\cdot)$ is an operator whose output may take on two possible integer values which are obtained by either rounding up or down its argument. This depends on the *a priori* unknown phase relation between the local oscillator and the demodulated RF signal. The Gen2 protocol defines tolerance margins for the different backward frequencies which can be synthesized from (1). Taking into account these tolerances and the timing resolution requirements of the forward link, as well as the need for reducing the dynamic power consumption of the processor, it can be theoretically found that the minimum master clock frequency imposed by Gen2 requirements is 1.92 MHz [16], [17].

III. Baseband Processor Architecture

The baseband processor of a sensory RFID tag decodes the demodulated signal, checks consistency, performs the operations requested by the reader, manages the access to the memory blocks (and, eventually, to the data acquired from the sensor), and generates the information to be backscattered to the interrogator.

Fig. 3 shows the block diagram of the proposed processor. Its operation is enabled by the baseband POR signal through a flip-flop synchronized to the system master clock *clk_master*. When enabled, the processor provides a single output streaming response to the demodulated signal coming from the analog front end of the RFID *data_dem* and, eventually, from the voltage acquired from the sensory plane *sens_in*.

Aside from the *Timing Unit*, to be discussed in Section IV, the processor consists in three major blocks which implement decoding, encoding, and processing operations, respectively.

In the decoding section, a falling-edge triggered flip-flop *Sync_FF* is used to synchronize *data_dem* to the master clock signal. Then, a *PIE Decoder* block is used to convert the resulting digitized forward link from PIE to binary format. This is simply accomplished by a time-to-digital conversion. The number of clock cycles comprised during the symbol *RTCal* is computed and divided by two to define a *pivot*. If a symbol has less number of cycles than the *pivot*, then it is a *data*-0 symbol; otherwise, it is a *data*-1 symbol. The output of the *PIE Decoder* block *bit_out* is sequentially stored in a 16-b *Shift Register* block to be evaluated by the *Command Decoder* block.

The purpose of the *Command Decoder* is to identify which instruction has been sent by the reader. This is a simple task because commands in the Gen2 protocol include a code which unequivocally addresses the instruction received by the tag (third column of Table I). Command identification is accomplished when the last bit of this code is received. Then, the *Command Decoder* codifies the instruction in a 4-b vector *cmd_ID* (fourth column of Table I).

Aside from filling *Shift Register*, the output of the *PIE Decoder* block is also transferred to a cyclic redundancy check (CRC) unit for transmission error detection. The results of the CRC computations are stored in buffers and used by a *CRC Check* block to assess their validity.

After command identification, the *Command Decoder* passes *cmd_ID* to the *FSM Rx* block inside the processing section. This block is formed by a set of finite-state machines (FSMs), one per Gen2 command. Only that FSM addressed by the *Command*

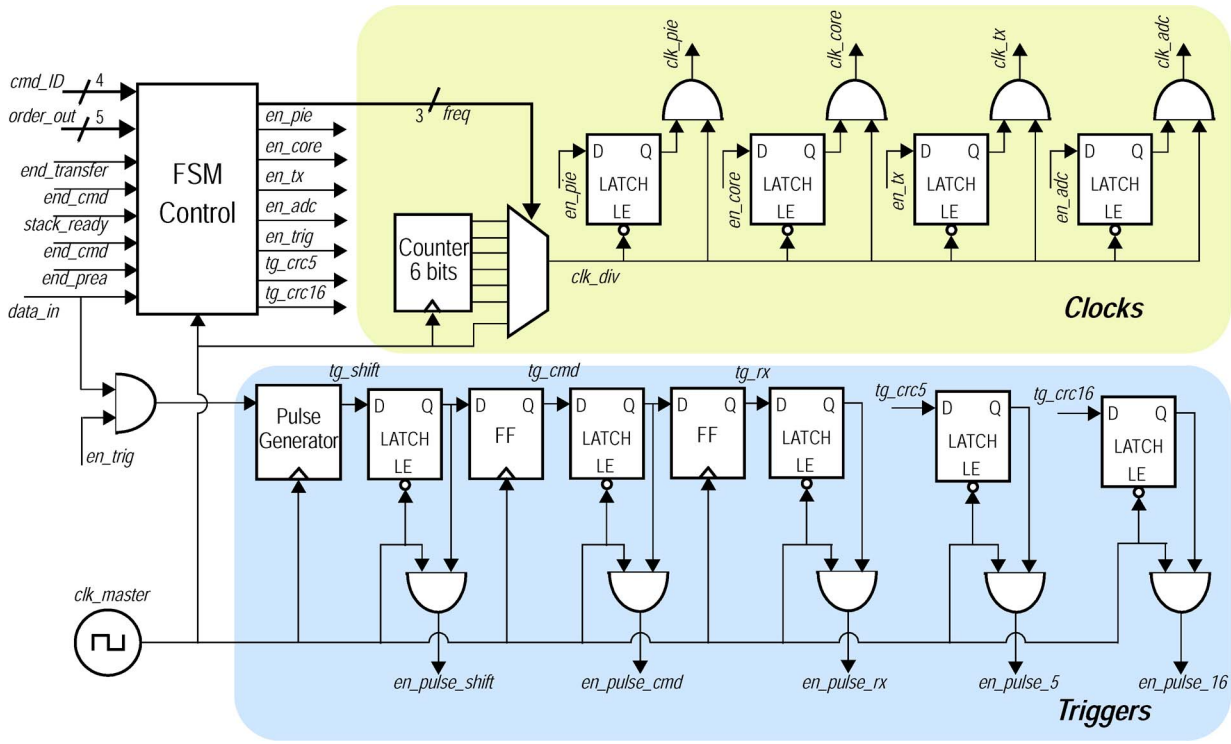

Fig. 4. Structure of the *Timing Unit* block.

Decoder is active; the others are disabled. The active FSM sequentially stores the command parameters in the registers of the *Stack* block. Only that register which is being addressed by the *FSM Rx* block is active; the others remain off.

The *FSM Core* block decides the tag's state, performs the required state transitions, reads the parameters stored in the *Stack* by the *FSM Rx*, and triggers the *FSM Tx* block according to the command that has been received. When operations at *FSM Core* are concluded, a nonzero 5-b vector *order_out* is transmitted to the *FSM Tx* block.

At the encoding section, the *FSM Tx* block performs the actions requested by the reader, such as to read the nonvolatile memory of the tag (represented in Fig. 3 by the *PROM* block), gather parameters or information to send (including data from the sensor interface), or control the transmitter for the backward link. Depending on the handled command, the *FSM Tx* block also uses a 16-b random number generator for authentication, data encryption, and key administration.

The *FSM Tx* is formed by a set of FSMs. There is one FSM for each possible action, and as before, only one FSM is enabled at a time. The *FSM Tx* block calculates the number of master clock cycles required for the synthesis of the backscattering link frequency (BLF) using the DR and the $TRcal$ information. This counting number is later transferred to the *Tx* block which encodes the data at the bit rate requested by the reader. When the requested action has been finished or the transmission is completed, *FSM Tx* and *Tx* (if required) are disabled, and *FSM Core* is activated again to check if the processor must change the state or remain in the same configuration.

The *PROM* is a 128-b one-time-programmable memory array based on Zener Zap diodes acting as antifuses [31]. The memory and its driving circuitry use standard cells available in the technology. The *EPC Number* for the identification of the tag is stored in the first 96 b of the memory, and the remaining 32 b is reserved for user data, for instance, sensor calibration data.

IV. Timing Unit

The *Timing Unit* generates the control signals required by the decoding, encoding, and processing operations described in Section III. Two basic power saving design strategies have been considered in its implementation, namely, the clock-gating (CG) and clock-management (CM) approaches [13].

The former is a well-known approach which builds on the idea of disabling blocks when they are dispensable, thus reducing the overall power consumption of the system [18], [19]. For instance, if the processor has not completely interpreted a received command, there is no need to activate those blocks involved in the backward link communication. CG can be simply realized by combining the input clock with an enable flag in accordance to the command that the processor is currently handling. If the enable flag is only active during a single clock period, the gated signal is a simple pulse, herein denoted as a trigger.

In other respects, not all the blocks of the processor need to run at full speed. Rather, some of them can be clocked at a fraction of the master frequency to save power. Moreover, there are blocks that can be driven at different frequencies, depending on the particular processor state. This is the design principle of the CM approach, i.e., to define dedicated clocks per block and state in order to reduce the overall dynamic power consumption of the processor. The lower limit of the dedicated clock frequencies is determined by the time interval between two rising edges of the demodulated input signal.

TABLE II
DEDICATED CLOCKS OBTAINED BY APPLYING CM STRATEGIES

Clock Signal	Driven Block	Enabling Signal	Disabling Signal	Frequency	Commands
clk_pie	*PIE Decoder*	*en_pie*	*stack_ready*	f_m	All
clk_core	*FSM Core*	*en_core*	*order_out / end_core*	f_m	*Query, Write, Read, Lock & Access*
				$f_m/2$	*QueryRep & ACK*
				$f_m/4$	*ReqRN*
				$f_m/64$	*Select*
clk_tx	*FSM Tx*	*en_tx*	*end_transfer*	f_m	All but the *Write* command
	Tx			$f_m/64$	*Write*
clk_adc	*ADC*	*en_adc*	*end_transfer*	$f_m/64$	*Write*

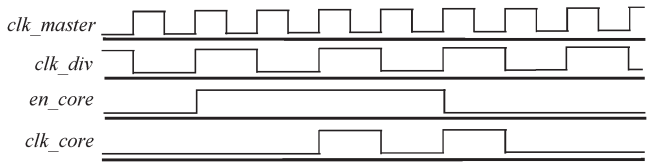

Fig. 5. Timing diagram of *clk_core*.

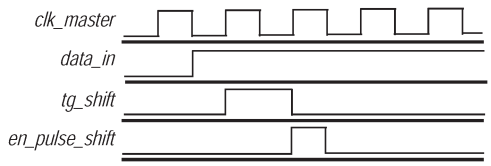

Fig. 6. Timing diagram of *en_pulse_shift*.

TABLE III
TRIGGER SIGNALS

Trigger	Driven Block	Enabling Pulse	Disabling Flag
en_pulse_shift	*Shift Register*	*tg_shift*	*stack_ready*
en_pulse_cmd	*Command Decoder*	*tg_cmd*	*end_cmd*
en_pulse_rx	*FSM Rx*	*tg_rx*	*stack_ready*
en_pulse_5	*CRC-5*	*tg_crc5*	*end_core*
en_pulse_16	*CRC-16*	*tg_crc16*	*end_core*

The schematic of the *Timing Unit* block is shown in Fig. 4. It consists of three main sections: *FSM Control*, dedicated clocks synthesis, and trigger signals generation.

The *FSM Control* handles the state of the baseband processor and decides the clocks and triggers which are active along the circuit operation. It is driven by a set of input signals and vectors and clocked by *clk_master*.

Dedicated clocks are obtained by means of a 6-b counter driven by the *clk_master*. Accordingly, clocks with frequencies $f_m = f_m/2^n$, $n = 0, \ldots, 6$, can be synthesized. Table II summarizes the different dedicated clocks synthesized by the *Timing Unit*, along with the baseband blocks that they drive, the signals used to enable and disable the clock, their output frequencies, and the associated commands. As an example, Fig. 5 shows a timing diagram for the synthesis of *clk_core* which runs at half the frequency of the master clock. Following CG strategies, *clk_core* is only active in response to a delayed version of the enabling signal *en_core*.

Table III shows the different trigger pulses generated by the *Timing Unit*, along with the baseband blocks that they drive and the signals used to enable and disable them. The first three triggers in Table III are related to changes in the input data signal *data_in*, whereas the other two triggers are related to CRC operations. As an example, Fig. 6 shows the timing diagram of the signals involved in the generation of the *en_pulse_shift* trigger signal, which is used to enable the *Shift Register* block.

It is worth observing that triggers *en_pulse_cmd* and *en_pulse_rx* are delayed versions of *en_pulse_shift*, by one or two master clock cycles, respectively. This favors the correct synchronization of the *Shift Register*, *Command Decoder*, and *FSM RX* blocks and also allows for a more uniform distribution of current consumption over time.

V. SENSORY INTERFACE AND DATA TRANSFER

Specific to sensory-type RFIDs, the architecture in Fig. 3 also includes an ADC which converts the quasi-static voltage signal generated by the external sensor.

Data transfer from the converter to the reader implies two mandatory Gen2 commands: *Write* and *Read*. The procedure is shown in Fig. 7. The interface circuitry is enabled when the *Write* command addresses the *User Bank* of the tag.[1] When this occurs, the processor turns down a *powerdown* flag, and the ADC starts converting the analog input signal acquired by the voltage buffer after a 50-μs delay to guarantee a quite supply—the digital activity of the processor considerably decreases after such a delay. The conversion process is repeated five times. The first one $D0$ is discarded because of possible sampling errors during ADC power on, and the remaining four

[1]Data storage in the Gen2 standard is divided into four different banks, internally divided in 16-b length words, denoted as Reserved, EPC, Tag Identification (TID), and User banks [14]. The optional Reserved bank contains the kill and/or access passwords of the tag in case such a feature is implemented. The EPC bank stores the variable-length EPC together with a 16-b protocol control word. It also contains a 16-b CRC code which is calculated upon each power-up. The TID bank stores the manufacturer's code which allows for an interrogator to identify the custom commands and/or optional features that the transponder supports. Finally, the User bank is optional and can be exploited in sensory tags to read/write sensor measurements.

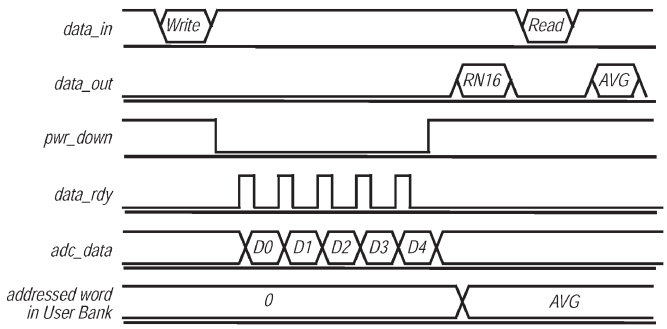

Fig. 7. Communication diagram for the processor/ADC interface.

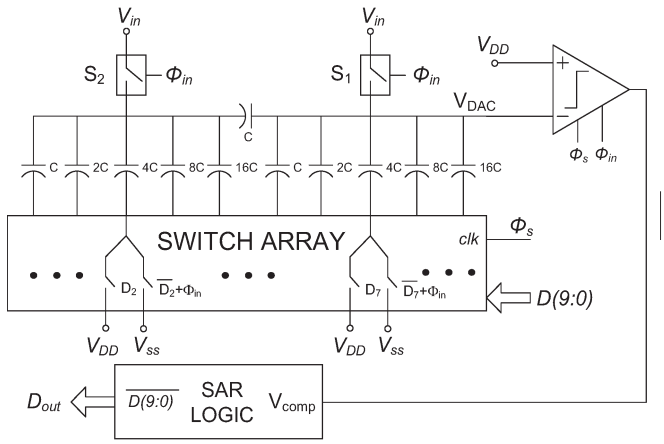

Fig. 8. Simplified schematic of the 10-b charge-redistribution SAR-ADC.

conversions $D1, \ldots, D4$ are averaged in digital domain and stored in the *User Bank* position specified in the *Write* command. Afterward, the tag informs the reader that the conversion has been successfully completed (otherwise, an error command is returned). Finally, the interrogator sends a *Read* command addressing the memory position where the ADC conversion has been stored, and the information is retrieved.

The interface circuitry uses the gated clock *clk_adc* (running at a frequency of $f_m/64$) during the conversions $D0, \ldots, D4$. This frequency is internally divided by two by means of level-shifted flip-flops which also adapt the logic levels to the regulated reference. Altogether, the ADC operates at a frequency 128 times slower than the master clock. As the ADC requires 12 clock cycles to complete a conversion, its nominal throughput rate is 1.25 kS/s.

Fig. 8 shows the schematic of the ADC. It is a charge-redistribution SAR converter which consists of a capacitive digital-to-analog converter (DAC), a comparator, and some control logic (itself called the SAR). Circuit operation is as follows. The input signal is first sampled and stored in the capacitive DAC and then added to the analog equivalent of the first SAR code [the most significant bit (MSB) is set to "1" while the remaining bits are "0"] to give

$$V_{\mathrm{DAC}} = V_{\mathrm{in}} + V_{\mathrm{DDA}}/2 \tag{2}$$

where V_{DDA} is the regulated power supply of the whole interface circuitry. The value (2) is compared to V_{DDA}, and

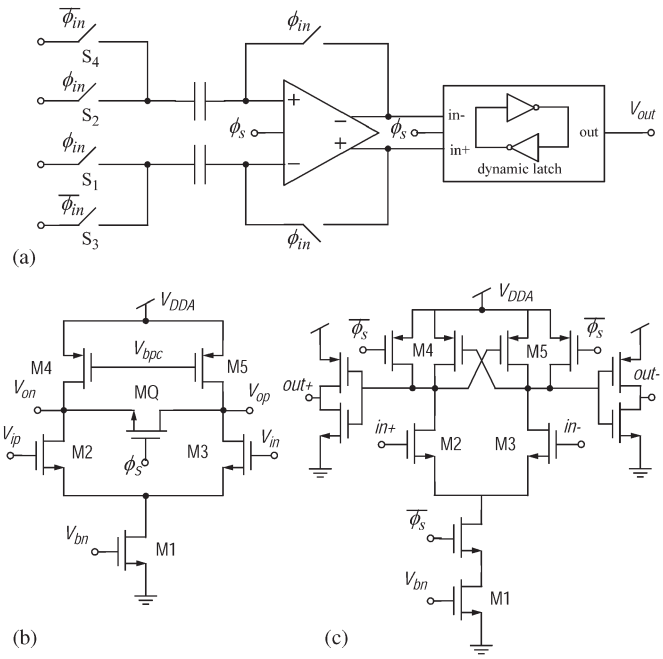

Fig. 9. Schematics of the (a) autozeroed comparator, (b) preamplifier, and (c) dynamic latch.

depending on the output of the comparator, the MSB of the ADC output is definitively set to "1" if $V_{\mathrm{in}} > V_{\mathrm{DDA}}/2$ or "0" if otherwise. Correspondingly, the MSB capacitor is tied to V_{SS} or V_{DDA} (the SAR and ADC outputs are complementary). Afterward, the next bit of the SAR register is activated for an additional comparison, and the procedure is repeated until the N-bit conversion is completed. At the end of the conversion phase, the output of the DAC is given by

$$V_{\mathrm{DAC}} = V_{\mathrm{in}} + \sum_{n=1}^{N} V_{\mathrm{comp}}(n) \cdot \frac{V_{\mathrm{DDA}}}{2^n} \tag{3}$$

where $V_{\mathrm{comp}}(n) = [0, 1]$ is the nth comparison result.

The capacitive DAC uses two 5-b binary-weighted subarrays connected by a unitary capacitor to obtain the required 10-b resolution [20]. Switches in the array are pMOS or nMOS, depending on whether the bottom plate of capacitors is connected to the negative or positive rails (V_{SS} or V_{DDA}, respectively). Sampling switches S1 and S2 are bootstrapped to allow for rail-to-rail operation of the converter [21].

The comparator uses an input offset-compensated architecture so that the static resolution of the circuit remains below the converter quantization step. The schematic of the comparator is shown in Fig. 9(a) and consists of an autozeroed preamplifier [Fig. 9(b)] followed by a dynamic latch [Fig. 9(c)]. As V_{DAC} swings from $V_{\mathrm{DDA}}/2$ to $3_{\mathrm{VDD}}A/2$, a simple pMOS switch S2 is used to reliably sample this voltage. On the contrary, S1 is a bootstrapped switch, and S3 and S4 are CMOS switches.

Finally, the SAR logic block has been implemented using the custom architecture presented in [22], which provides nearly 40% less power than conventional library cell solutions.

Both the voltage buffer and the ADC are supplied by the bias current generator in Fig. 10. It is based on the circuit presented in [23] and provides a nominal current reference I_{ref} of 30 nA.

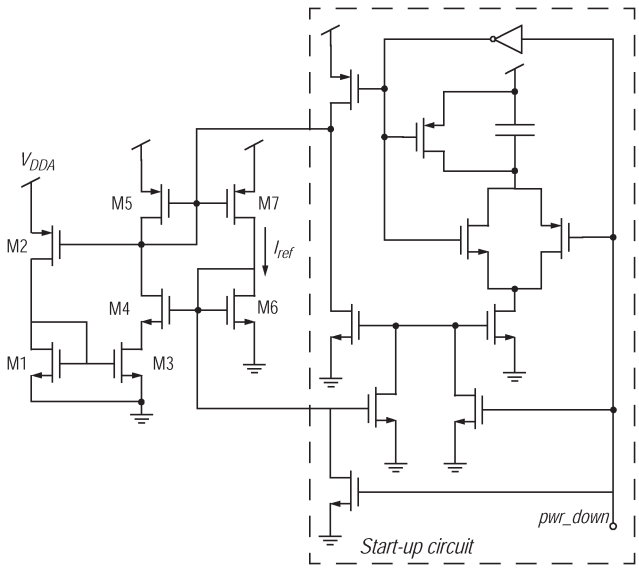

Fig. 10. Bias current generator for the signal conditioning circuit.

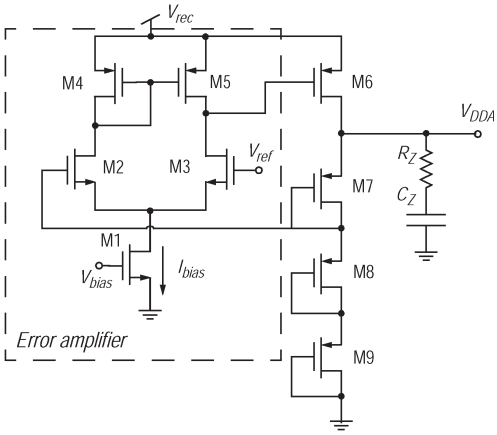

Fig. 11. Schematic of the regulator employed to supply the signal conditioning circuit and the external sensor.

The current generator includes a start-up circuit which avoids the reference circuit to get trapped in a parasitic zero current state [24]. Circuit operation is enabled when signal *pwr_down* is in its high state. Otherwise, the generator is switched off with a negligible power consumption and the driven blocks turn unbiased.

As shown in Fig. 1, the complete mixed-signal sensor interface is powered by a dedicated low-dropout regulator (LDO). Its schematic is shown in Fig. 11 and provides a stable output supply voltage $V_{\rm DDA}$ of 1 V. The unregulated input voltage $V_{\rm rec}$ can range from 1.1 to 3 V. The output voltage $V_{\rm DDA}$ is stabilized by means of a left half-plane zero compensation technique implemented by R_Z and C_Z [25]. The load of the regulator is defined by the on-chip signal conditioning circuitry and the external sensor. The maximum output load current and maximum load capacitance tolerated by the regulator are 50 μA and 30 pF, respectively. The quiescent current of the regulator is 700 nA, 50 nA of which is consumed by the error amplifier, and it obtains a line regulation of 17 μV/V, a load regulation of 10 mV/mA, and a peak dropout voltage of 160 mV.

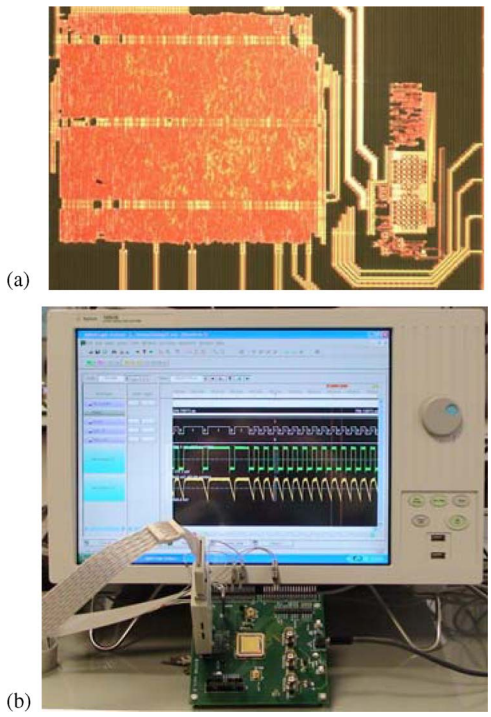

Fig. 12. (a) Die micrograph of the passive UHF RFID baseband processor and the data-conversion stage. (b) Evaluation setup.

VI. Experimental Results

The architecture of Fig. 3 has been implemented in a 0.35-μm CMOS technology. Fig. 12(a) shows a microphotograph of the chip, in which the signal acquisition circuitry and the digital baseband processor can be easily identified. The baseband processor occupies 1.0 mm^2. Fig. 12(b) shows a photograph of the setup employed for testing.

Test has been realized by using an Agilent 16902B logic analyzer and a Tektronix AFG3102 for master clock frequency generation. Measurements have addressed the functional validation of the processor, its PER and power consumption performances under different supply conditions, and the characterization of the mixed-signal sensor interface. They are separately discussed next.

A. Functional Verification

Ten samples of the prototype have been exhaustively tested to validate their functionality. Our measurements confirmed that the system works properly in all the samples and for all the instructions defined by the EPC standard. In the experiments, we used a supply voltage $V_{\rm DDD} = 0.9$ V for the baseband processor and $V_{\rm DDA} = 1.0$ V for the sensory interface circuitry (the $V_{\rm ref}$ and $V_{\rm rec}$ in Fig. 11 were 650 mV and 1.5 V, respectively). Voltages $V_{\rm DDD}$, $V_{\rm ref}$, and $V_{\rm rec}$ were externally provided by dc power supplies.

As an illustration, Fig. 13 shows the system response to a sequence of commands which conclude with a data acquisition from the sensor. The inset of Fig. 13 shows the details of some of the signals involved in the *Read* operation. Signals *clk_pie* and *en_pulse_shift* are only active when the processor

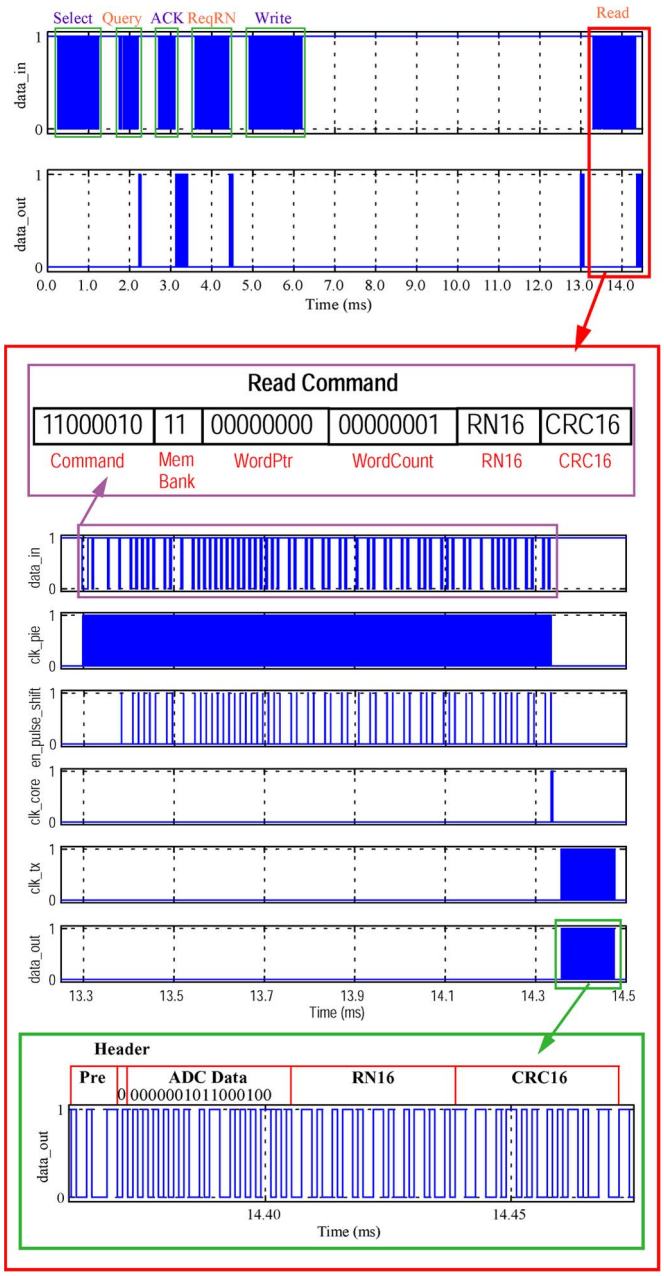

Fig. 13. Example of tag-reader communication, including a sensor information flow using FM0 encoding for the backward link.

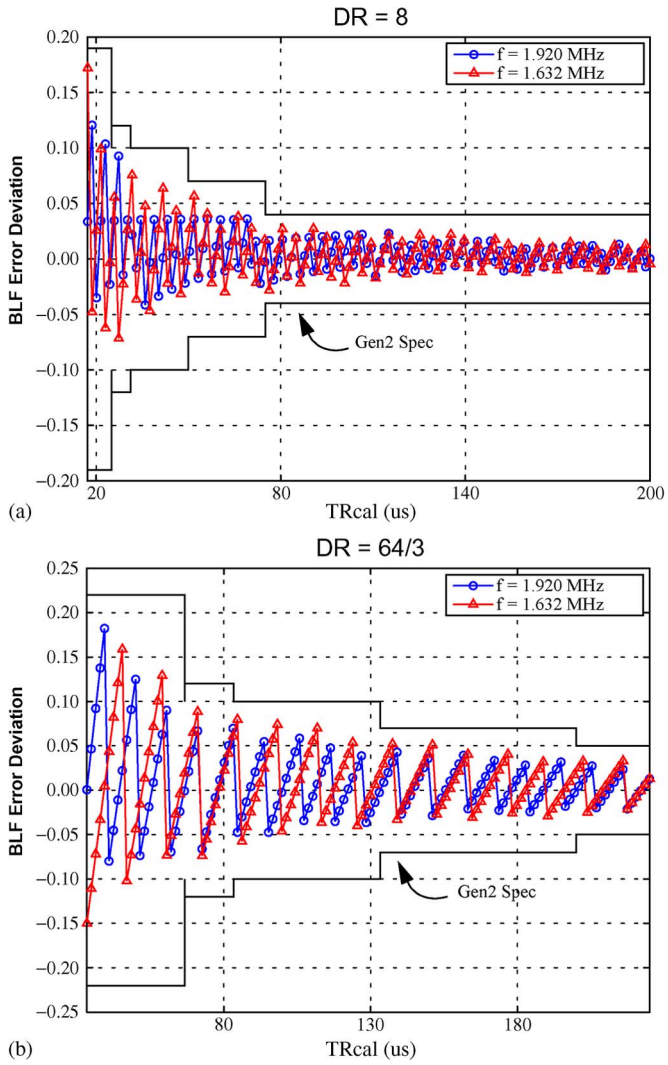

Fig. 14. BLF error deviation. (a) $DR = 8$. (b) $DR = 64/3$.

is decoding the input signal *data_in*. At the end of the *Read* command, *clk_core* is enabled to process the received information. Once the processing finishes, *clk_core* is disabled, and *clk_tx* turns on for transmitting the requested data *data_out*. It is a digital sequence which contains the averaged data conversion generated during the previous *Write* command, together with other parameters imposed by the communication protocol. It is worth observing that only the ten less-significant bits of the *User Bank* are occupied by the data-conversion outcome, in accordance to the resolution of the ADC. Once the information is transmitted, *clk_tx* stops.

Another test concerned the robustness of the processor against deviations of the master frequency. Fig. 14 shows the backscatter frequency error of the system measured at 1.92 and 1.632 MHz, i.e., using a master clock frequency 15% slower than the nominal. Divide ratios of 8 and 64/3 have been considered in Fig. 14(a) and (b), respectively. In both cases, the boundary lines are per the Gen2 specification requirements. The obtained sawtooth characteristics are a direct consequence of the rounding errors inherent to (1). Fig. 14 shows that, even with a 15% frequency deviation, the system meets the Gen2 requirements with margin.

B. PER

In order to assess the performance limits of the presented baseband processor alone[2] under realistic operation conditions, two different experimental setups have been considered. They are aimed to reproduce, without resorting to RF signaling, the two types of baseband biasing configurations that can be found in passive tags, those using crude clamps [12], [26] or using regulators [8]–[11], [27], [28]. It is worth insisting that no external clean supply has been used in the measurements

[2]The performance of the mixed-signal sensor interface is presented in Section VI-D.

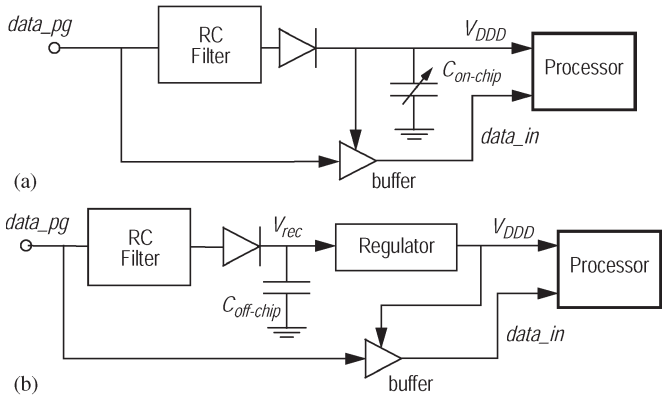

Fig. 15. Test setups to evaluate the PER performance of the baseband processor. (a) Nonregulated and (b) regulated supply voltages.

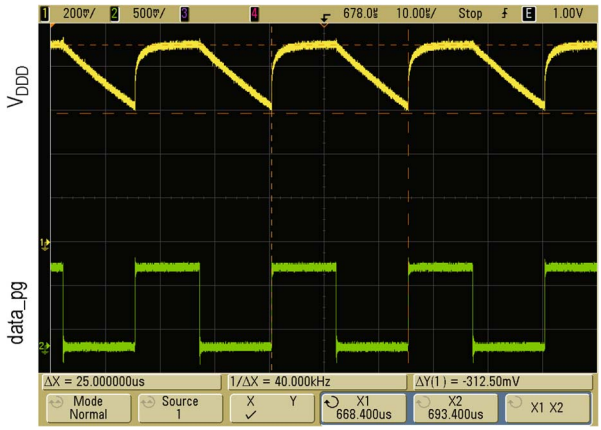

Fig. 16. Measured signals in the experimental setup of Fig. 15(a). Input signal *data_pg* is a 40-kHz pulse train with 1-V amplitude and 47.5% duty cycle. The peak amplitude of the rectified signal $V_{\rm DDD}$ is 0.9 V, and the voltage drop is 312.5 mV.

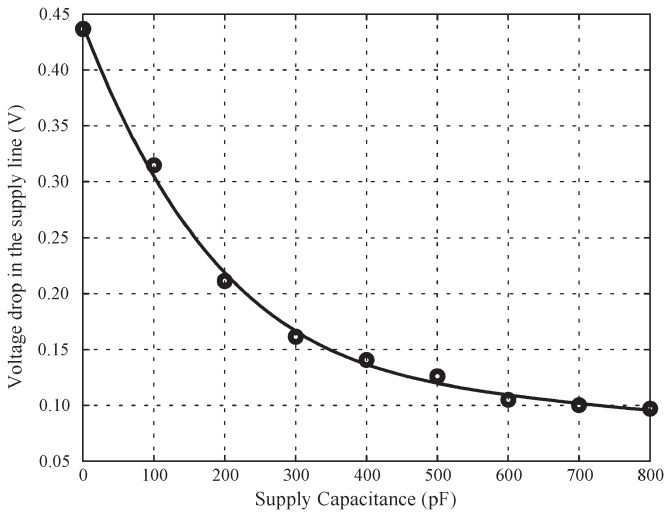

Fig. 17. Peak voltage drop in the supply line of the processor, with a $V_{\rm DDD}$ amplitude of 0.9 V. The circles correspond to the measured results, and the continuous trace is a fitting curve.

which otherwise would unrealistically ameliorate the true performance of the processor.

In one scenario [denoted as the nonregulated case and shown in Fig. 15(a)], the system is directly powered by the rectified average of the incoming binary data *data_pg*. This bit stream, generated by an Agilent 16702A pattern generator, can be interpreted as an amplitude-adjustable version of the amplitude shift keying (ASK) modulating signal used by the reader. Rectification is simply implemented by a programmable on-chip supply capacitor $C_{\rm on-chip}$ and an external Schottky diode (Agilent HSM S-2850), together with some passive filtering circuitry. The different capacitance values for $C_{\rm on-chip}$, nominally ranging from 0 to 800 pF, are externally programmed through dedicated control pins. The filter, which is a simple RC section, has been added to model the forward time constant of the rectifier and, hence, to better emulate the voltage ripples which can be observed at the output of the rectifier/limiter block in monolithic RFID tags [28], [29]. Note that, due to the PIE encoding format used in the forward link [see Fig. 2(b)], the amplitude of the received ASK signal remains at maximum value (no matter if data-0 or data-1 has been transmitted) except during the RF notches of duration PW, in which the amplitude drastically drops with a nominal modulation index of 90%. As the duration of the interval PW, which may amount from 2 to 13.125 μs [14], is much larger than the period of the carrier signal, the ripple at the output of the rectifier/limiter in Fig. 1 is essentially dominated by the RF notches [28], the effect that can be easily reproduced with the setup of Fig. 15(a) with no need for RF signals. As an illustration, Fig. 16 shows a snapshot of the generated supply signal $V_{\rm DDD}$, for a 1-V amplitude *data_pg* signal, assuming that $PW = 13.125$ μs and a load capacitance $C_{\rm on-chip} = 100$ pF. As the forward voltage of the Schottky diode is 150 mV, the peak value of $V_{\rm DDD}$ is 900 mV. In this scenario, the voltage drop (312.5 mV in the example) due to the ASK modulation depends inversely on the supply capacitor [29]. This is illustrated in Fig. 17, which shows the experimentally observed peak ripple voltage in terms of the on-chip supply capacitance for a $V_{\rm DDD}$ amplitude of 0.9 V. Note that, for low supply capacitances, the voltage drop can be as high as 0.44 V.

In the second scenario [denoted as the regulated case and shown in Fig. 15(b)], the system is powered by an LDO preceded by a rectification circuit, similar to that shown in Fig. 15(a), but using an external capacitor $C_{\rm off-chip} = 300$ pF. The baseband regulator follows a structure similar to that in Fig. 11, but instead of left half-plane zero compensation (R_Z is replaced by a short), it uses Miller compensation (a 1-pF capacitor is connected between the gate and drain of the pass transistor M6) [25]. Capacitor C_Z amounts 200 pF, and it is implemented by properly programming the on-chip capacitor $C_{\rm on-chip}$. Similar to the LDO for the signal acquisition section, the unregulated input voltage $V_{\rm rec}$ can range from 1.1 to 3 V ($V_{\rm rec} = 1.5$ V was used in the experiments). The maximum output load current is 100 μA, and the quiescent current is only 125 nA, 25 nA of which is used by the error amplifier. The regulator obtains a line regulation within 25 μV, a load regulation of 8 μV/μA, and a peak dropout voltage of 150 mV.

In both powering strategies, the processor data input *data_in* is contaminated by the supply variations (similar to that occurs in fully integrated transponders) by means of voltage buffers biased by the synthesized $V_{\rm DDD}$.

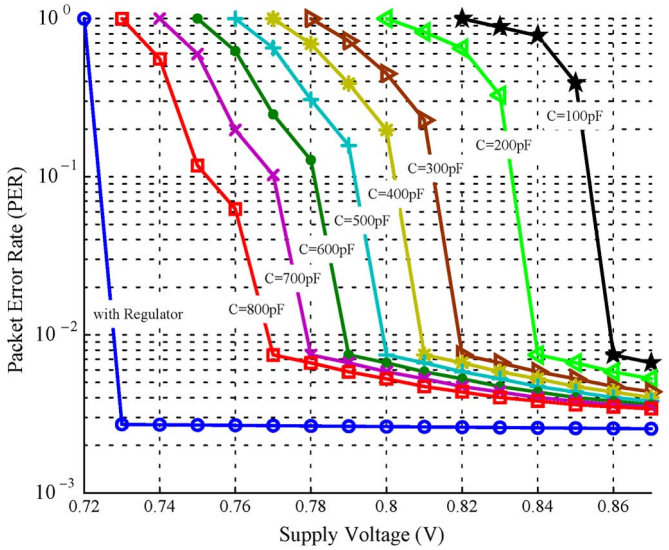

Fig. 18. PER in terms of the supply voltage.

Obviously, degradation of the biasing conditions affects the performance of the processor. This aspect has been studied by evaluating the PER performance for the two scenarios in Fig. 15. The experimental results are shown in Fig. 18, where the PER value in terms of the V_{DDD} amplitude is represented. In the nonregulated case, measurements were done for different values of the supply capacitance (from 0 to 800 pF at steps of 100 pF). The evaluation procedure was as follows. For each configuration, the supply amplitude V_{DDD} was decreased, starting from 0.9 V, in steps of 10 mV until the PER value reaches 1, meaning complete malfunction. The PER was calculated by counting the number of failed responses to 12 000 *Query* commands, each preceded by a system reset. The ratio between the number of fails and the total number of generated commands gives the PER of the processor.

As can be seen in Fig. 18, the plots settle to a PER value of about 3×10^{-3} beyond a certain threshold value, which varies from one configuration to another. The 3×10^{-3} PER value is far below the transponder sensitivity level of 2×10^{-1} PER imposed by the regulations in Europe [30]. In the nonregulated case, the V_{DDD} thresholds are located at lower amplitudes as long as the supply capacitor increases. Therefore, there exists a tradeoff between area and power consumptions in this scenario. In the regulated case in Fig. 15(b), the threshold is located even at a lower V_{DDD} value than any nonregulated configuration, at the expense of some increment on power consumption due to the additional LDO block. Namely, the threshold V_{DDD} value of the PER curve is at 740 mV at which the processor obtains a PER slightly lower than 3×10^{-3}. This confirms the superior performance of regulated solutions in terms of error rate performance as compared to nonregulated ones, besides the larger tolerance against process and temperature variations demonstrated in [28].

C. Power Consumption of the Digital Baseband Processor

The power consumption of the baseband processor has been evaluated for a V_{DDD} amplitude of 0.9 V, employing the regulated power supply configuration in Fig. 15(b). Note that a 160-mV voltage margin has been added to the minimum required V_{DDD} value measured in Fig. 18 to guarantee correct operation against wafer-to-wafer process variations.[3] The average current consumption during the reception and response of a *Read* command at maximum bit rate both for the backward and forward links was about 2.2 μA, with current peaks below 3 μA.

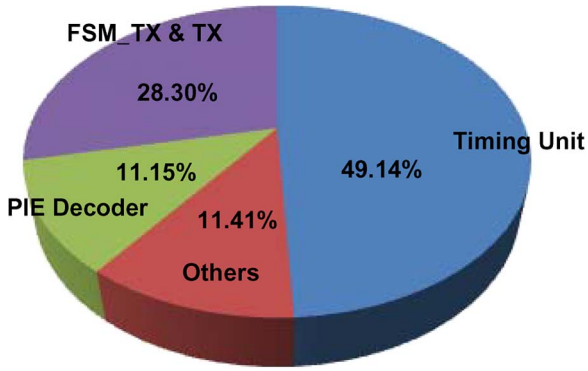

Fig. 19. Current consumption distribution of the baseband processor for a 0.9-V supply voltage.

TABLE IV
COMPARISON WITH PREVIOUSLY PUBLISHED BASEBAND PROCESSORS FOR THE STANDARD ISO 18000-6C

Reference	Supply Voltage	Master Frequency	Current Consumption	CMOS Technology
[13][(a)]	1.2 V	480 kHz	1.47 µA	0.35 µm
[18]	1.0 V	2.56 MHz	6.40 µA	0.18 µm
[31]	0.8 V	2.30 MHz	6 µA	0.18 µm
[32][(b)]	0.7 V	3.00 MHz	6 µA	0.13 µm
[33]	3.3V	1.28 MHz	5.10 µA	0.35 µm
[34]	1.1 V	1.28 MHz	22.72 µA	0.18 µm
This work	0.9 V	1.92 MHz	2.2 µA	0.35 µm

a. It only implements mandatory commands. Because of the low master frequency, not all the backward rates are possible.
b. It only implements the *Query*, *ReqRN*, *ACK* and *Read* commands.

Fig. 19 shows how this current consumption distributes among the different blocks of the architecture in Fig. 3. Note that the *Timing Unit*, *FSM Tx*, *Tx*, and *PIE Decoder* blocks are the most current-demanding elements of the processor because they are clocked at the master frequency.

Table IV compares the performance of the presented processor with other implementations in the literature and shows how the power/current consumptions were measured. Unfortunately, there is not a unified criterion to report the performance of the processors, and in some cases, it is not even clear if the circuit is fully compliant with the targeted standard. Only [13] clearly specifies that power consumption was measured during the reception and response to an ReqRN command. Anyhow, it can be observed that the proposed prototype achieves much lower current consumption than other circuits with similar

[3]According to the information provided by the foundry, the tested wafer is close to the typical technology corner, where the nMOS and pMOS have threshold voltages of about 0.48 and −0.51 V, respectively.

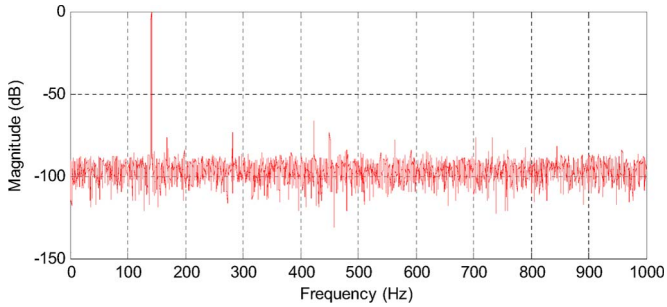

Fig. 20. Fast Fourier transform spectrum of the signal conditioning output for a 140-Hz input tone sampled at 2 kS/s.

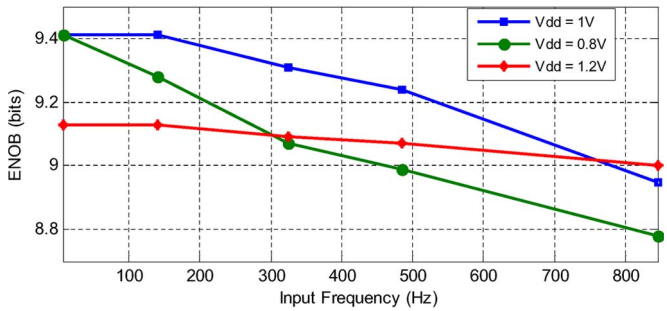

Fig. 21. ENOB performance of the mixed-signal interface under different supply voltages at 2 kS/s.

feature size, even when measured during one of the most power demanding commands, such as the *Read* instruction, and assuming maximum signaling speed.

D. Mixed-Signal Interface

Fig. 20 shows the output spectrum of the ADC circuitry for a 1-V-amplitude 140-Hz input tone. The throughput rate of the ADC has been set to 2 kS/s (well beyond the nominal rate of 1.25 kS/s) and the supply voltage is 1 V, so that the rail-to-rail feature of the interface is fully exploited. As can be seen, the measured signal-to-noise and distortion ratio is 58.39 dB, which results in 9.41 ENOB.

Fig. 21 shows the comparison of the performances of the interface for different input frequencies and supply voltages assuming again a 2-kS/s conversion rate for the ADC. As shown, the interface obtains effective resolutions above 8.75 b under all testing conditions. The power consumption of the mixed-signal interface including the current generation cell and the clock generation circuitry is 250 nW for 1-V supply and 2-kS/s sampling mode, while the consumption of the ADC alone is 130 nW.

VII. Conclusion

In this paper, the mixed-signal back end of a sensor-enabled RFID tag targeting the EPC Gen2 protocol has been designed and implemented in a 0.35-μm CMOS process. Because of the sensor interface, the prototype not only serves the purposes of identification but also can be used to monitor an environmental variable of interest. The design includes a fully EPC-compliant baseband processor, a data-conversion stage, and other auxiliary blocks, such as regulators and reference generators. The baseband processor is fully functional, meets the PER specifications of the standard, and is able to tolerate master clock frequency deviations as high as 15% from the nominal. This has been demonstrated for two different biasing circuits, either using a dedicated voltage regulator or a programmable supply capacitor. The current consumption of the baseband processor during a *Read* command, which is one of the most power demanding EPC instructions, is only 2.2 μA from a 0.9-V-amplitude biasing voltage provided by a voltage regulator. In other respects, the power dissipation of the sensor ADC, which is a 1-V 10-b charge-redistribution SAR converter, is 250 nW and obtains 9.41-b effective resolution at 2 kS/s. A simple protocol for the data transfer between the processor and the data-conversion stage has been also introduced.

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