Trabajo Fin de Máster

Máster en Ingeniería Aeronáutica

Design and Modelling of a Bidirectional DC-DC Converter based on Full Bridge Current Doubler Topology for Aeronautical Applications

Autor: Álvaro de Jesús Ojeda Rodríguez

Tutor: María Ángeles Martín Prats

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This project would not exist without the encouragement from a lot of people.

I would like to thank my parents, and also my whole family, for their constant support. They always help me to take the best decision. They always help me to be a better person.

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Abstract

This project falls within the framework of the research about More Electric Aircraft (MEA) concept, which is the target of the current designs. In this context, electrical system is being reinforced as one of the main power systems. Electrical power level and voltage level transmission are increasing –the last one is tending to High Voltage Direct Current (HVDC) level– and requirements of generation, distribution, management and control of this kind of power are becoming more and more challenging.

Within electrical system, power converters are responsible for electrical power transmission. Moreover, they must fulfil aeronautical standards in respect of on-board electrical and electronic systems. The precise aim of this project is to study suitable topologies for DC-DC bidirectional and isolated power converters within defined framework. Many industries, as aeronautical or automotive, request them with better features –for instance, power density and efficiency are critical KPI in aeronautical industry–. After a review of main power circuits that could fulfil specifications for these applications, a promising topology will be analysed from a numerical point of view.

Particularly, Bidirectional Current Doubler is the topology subject of study. Its working principle will be analysed under certain operating range domain. Simulation models will be developed to asses topology performance in such operating domain. By knowing currents and voltages on ideal elements, a more realistic components selection will be carried out, particularly as far as MOSFETs concerns. Finally, regarding a more little bit accurate model, efficiency will be calculated in terms of input and output power.

Contents

Acronyms

AC Alternating Current.

ATM Air Traffic Management.

ATRU Autotransformer Rectifier Unit.

ATU Autotransformer Unit.

BDC Bidirectional Converter.

CDR Current Doubler Rectifier.

DAB Dual Active Bridge.

DC Direct Current.

EMI Electromagnetic Interference.

HF High Frequency.

HV High voltage.

HVDC High Voltage Direct Current.

KPI Key Performance Indicator.

LF Low frequency.

LV Low voltage.

LVDC Low Voltage Direct Current.

MEA More Electric Aircraft.

PDS Power Distribution System.

PSM Phase Shift Modulation.

PSPICE Personal Simulation Program with Integrated Circuits Emphasis.

R&D Research and Development.

RMS Root Mean Square.

SESAR Single European Sky ATM Research.

SJU SESAR Joint Undertakinhg.

SPRC Series-Parallel Resonant Converter.

SR Synchronous Rectification.

TRU Transformer Rectifier Unit.

VDC Volts Direct Current.

ZCS Zero Current Switching.

ZVS Zero Voltage Switching.

Symbols

$\Delta \mathbf{I_{LDC2a+2b}}$ Peak-to-peak total current through LV side inductors.

$\mathbf{C_{oss}}$ Mosfet output parasitic capacitance.

$\mathbf{C_{snb}}$ Snubber capacitance.

$\mathbf{D}$ Duty cycle.

$\mathbf{f_s}$ Switching frequency.

$\mathbf{I_{AC1}}$ Transformer current at HV side.

$\mathbf{I_{AC2}}$ Transformer current at LV side.

$\mathbf{I_{L_{DC2a}}}$ DC inductor current.

$\mathbf{L}$ Leakage inductance.

$\mathbf{L_{DC}}$ DC inductor.

$\mathbf{L_m}$ Magnetizing inductance.

$\mathbf{n}$ Transformer turn ratio.

$\mathbf{P_2}$ Nominal power at low voltage side.

$\mathbf{R_{d_{clamped}}}$ Ohmic resistance clamped diode.

$\mathbf{R_{DSon}}$ Ohmic switch resistance when it is conducting.

$\mathbf{R_{LDC}}$ Ohmic resistance DC inductor.

$\mathbf{R_m}$ Magnetizing resistance.

$\mathbf{R_{snb}}$ Snubber resistance.

T1 Semiconductor HV side 1.

T2 Semiconductor HV side 2.

T3 Semiconductor HV side 3.

T4 Semiconductor HV side 4.

T5 Semiconductor LV side 5.

T6 Semiconductor LV side 6.

$\mathbf{T_C}$ Switching time.

$\mathbf{T_{dead}}$ Dead time.

$\mathbf{T_{free}}$ Freewheeling time.

$\mathbf{T_S}$ Switching period.

$\mathbf{V_1}$ High voltage.

$\mathbf{V_2}$ Low voltage.

$\mathbf{V_{AC1}}$ Transformer voltage at HV side before leakage inductance.

$\mathbf{V_{AC2}}$ Transformer voltage at LV side.

$\mathbf{V_{aux}}$ Auxiliary voltage source.

$\mathbf{V_{d_{clamped}}}$ Forward voltage drop clamped diode.

$\mathbf{V_{d_{switch}}}$ Voltage drop across switch antiparallel diode.

$\mathbf{V_{DS}}$ Mosfet drain to source voltage drop.

$\mathbf{V_L}$ Voltage drop through leakage inductor.

Chapter 1

Introduction

1.1 General presentation of the study

Currently, it is a fact that *More Electric Aircraft* (MEA) is not the future but the present. So R&D tends to aircraft designs that involve higher power level, [1]. This affects to power generation, transmission, management and control. A good example could be aircraft Airbus A350 and Boeing B787 *Dreamliner*. The first one comes with four independent variable frequency generators, each one of 100 kVA, [2]. The second one is fitted with four variable frequency generators, each one of 250 kVA, [3], [4]. From the electrical power generated on-board point of view, Boeing *Dreamliner* is closer to MEA concept than Airbus A350, since the first one generates more than twice the electrical power than the last one.

As far as safety, reliability and technological advances concerned, aeronautics is perhaps one of the most challenging industries. Issues related to weight and size reduction, power density and efficiency are also especially important. Because of this, electrical systems and electrical/electronics devices are required to be:

- Very efficient.
- With high power density.

Increasing efficiency will help to reduce environmental impact, and also decrease operating cost. International organisations, like SESAR Joint Undertaking (SJU), consider this R&D tasks seriously and therefore they support many research projects

in this field –and in many others that could be relation with improving efficiency, safety, and so on–like Clean Sky programs.

Power Electronics is the subject that faces such a challenging task. A good definition of Power Electronics is given by [5] :

> "Power electronics involves the study of electronics circuit intended to control digitally the flow of electrical energy. These circuits handle power flow at levels much higher than the individual device ratings".

Power electronics basic module is power converter. This electronic circuit contains switches (e.g. semiconductors), energy storage elements (e.g. inductors, capacitors) and transformers. An external control function commands the switches according to the input received from the load and power converter state.

Regarding the type of electrical power at input and output of power converter, a number of different kinds of converters exists:

- AC to DC converter, also called *rectifier*.
- DC to AC converter, also called *inverter*.
- AC to AC converter.
- DC to DC converter.

In order to improve reliability and safety, electrical power generation has been moved from DC to AC, [1]. This change in topology increased the power density due to the benefits of AC generators, with the consequent size and weight reduction. However, power distribution in new aircraft designs tends to include a hybrid PDS with DC and AC buses, in order to supply power to all type of loads, [3]. Figure 1.1 shows an example of MEA electrical power system architecture.

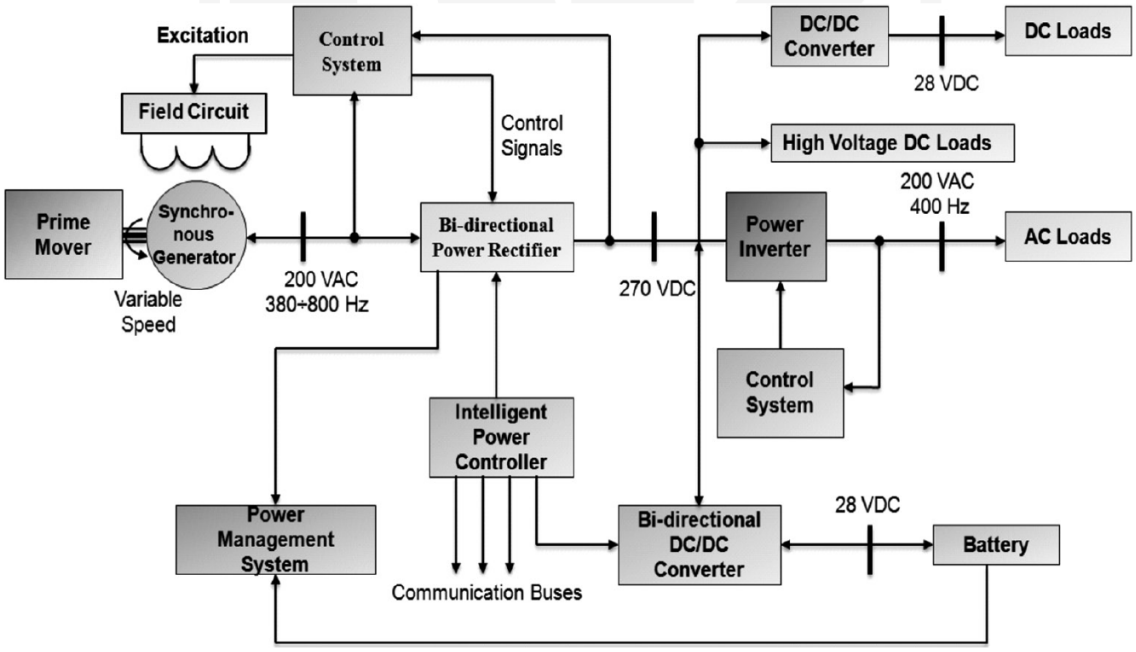

Figure 1.1: Generic electrical architecture of MEA concept of aircraft, [6]

As first concrete step, present work will be focused on HVDC to LVDC bidirectional power converter. Typical nominal voltage levels are presented in Figure 1.1: 270 VDC at HVDC and 28 VDC at LVDC. More precisely, this research will review isolated and bidirectional power electronic circuits -topologies-. The State-of-the-art revision goal is to select a promising topology that supports HVDC and LVDC ranges mentioned above. Application ranges are described in detail in Chapter 4.

This topology will be used to built low power modular bricks, where low power means few kilowatts. If the application requires high power transfer or high voltage levels, bricks can be connected forming a *cascaded multi-converter*, [7]. Each brick only handles a fraction of the total power. Converter bricks can be set in different configurations: if the brick terminals are connected in parallel, they will share the DC line current; in the other hand, if brick terminals are connected in series, DC line voltage is distributed among them. The optimum choice depends on the application.

Hence, despite of the voltage and power ranges are limited to magnitude order mentioned before, this research keeps utility for applications where high power and input/output voltages are involved.

1.2 Document structure

At the first place a condensed but fairly complete State-of-the-art has been carried out exploring the main available bidirectional and isolated topologies for DC to DC power conversion at certain HVDC and LVDC nominal levels, Chapter 2.

Chapter 3 describes briefly the key theoretical ideas to understanding the performance and physical operation of the power electronics circuit. A detailed explanation of two basic operating modes of converter will be exposed, giving waveform examples and describing the control of switches.

- **Buck mode.** This is the most usual working mode for such topology. The objective is power transfer from HVDC to LVDC.
- **Boost mode.** CDR is not widely used for this function: transfer power rising output voltage level to high values from low voltage input level.

This theoretical approach will be based on the circuit shows in Figure 3.2. Power converter will be connected at LV side either to load that requires LVDC power supply or LVDC network that impose constant voltage level. The same occurs at HV side.

Chapter 4 focuses on reviewing the main specifications and criteria design that will constitute the starting point to obtain a first estimation of main magnitudes.

Chapter 5, "Design of Components", described the main components of the power circuit and how they have been modelled.

A light description of numerical models and commercial software use for the simulation is contained in Chapter 6.

Chapter 7 collects the results of the whole study, which will be presented in different formats: graphics, tables, etc. Some of the expected results are:RMS currents through magnetics components and capacitors, and first order estimations of efficiency. All these results will be provided within the operating range provided by specifications.

At the end, Chapters 8 "Conclusions" and 9 "Future Work" sum up the main and more interesting ideas of the research and also review those issues that due to lack of time could not be completely solved. Moreover, some suggestions will be proposed as "work guidelines", i.e. parameters optimization and functional prototype manufacturing to compare experimental results with numerical ones.

1.3 Study objectives

Main study goals are summed up below.

- Compare topologies that fulfil essential requirements –high efficiency and high power density– for on-board electric and electronics power systems, as well as operating range defined by aeronautical application in the MEA concept framework.
- Select a promising topology and analyse it from a theoretical approach and also from a numerical approach.
- Using a single model with lossless components, estimate voltage and current levels over them. Accomplish an initial realistic components selection with this information, which withstand voltage and current maximum ratings.
- Finally, elaborate a slightly more advanced simulation model in order to calculate efficiency at certain operating points.

Chapter 2

State-of-the-art analysis

This chapter is a review on available DC to DC power converters, based on isolated and bidirectional topologies which are able to transfer power within the range of 1-5 kW, [8]. They also support well nominal working HVDC and LVDC ranges.

Hence the presented State-of-the-art focuses on some specific power circuits and excludes other ones that do not suit so well those specifications.

2.1 General architecture of DC to DC converter

A general configuration of a bidirectional DC to DC converter with galvanic isolation is shown in Figure 2.1.

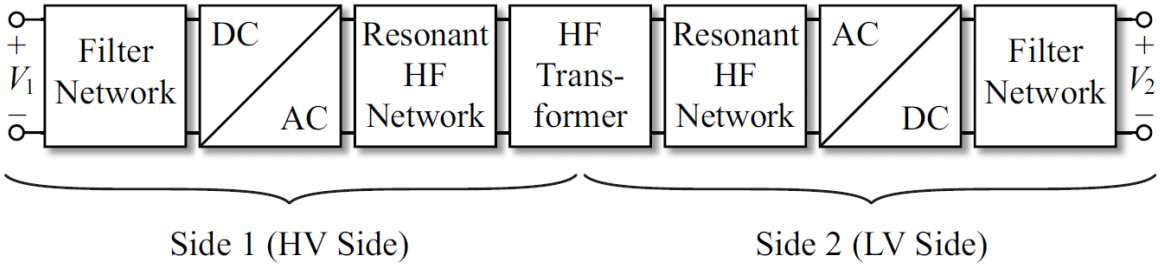

Figure 2.1: DC to DC converter general architecture, [8]

Filter networks in LV and HV side contain high frequency ceramic or thin film capacitors, a bank of electrolytic capacitors and an inductive component.

HF networks typically consist of an AC inductor (carrying AC currents) or a resonant network consisting of several AC inductors and capacitors. In the case of purely inductive networks, they can be integrated in the transformer (i.e. designing transformer leakage inductance value). In some topologies this HF network will determine AC waveforms of the converter, and in other cases they are simply used to control the switching transients waveforms. For example, these HF networks can be designed to allow soft switching at certain operating points.

2.2 Topologies description

A study of single-stage topologies with high efficiencies in a wide operation range has been carried out in [8]. As a consequence of the wide operation range requirement, some operation points might have low efficiencies. In those cases two stage topologies are interesting to drive the isolated converter at its optimal operating point in order to improve overall efficiency. However, adding an additional stage involves in general more complexity, losses and weight.

2.2.1. Single-phase DAB converter

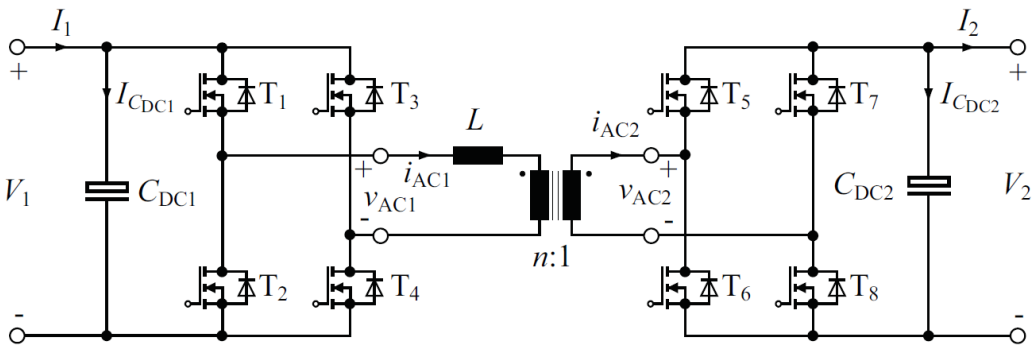

Figure 2.2: DAB converter topology, [8]

As it can be seen in Figure 2.2, DAB employs full bridge circuits on the HV side and LV side. In the DAB topology, reactive network integrates an inductor (L in Figure 2.2) connected in series to the HF transformer.

As stated previously, DAB topology can be driven using conventional PSM, but it also allows the use of alternative modulation schemes at certain operating points to achieve better converter performance. The aims of implementing advanced modulation schemes in the DAB are listed below:

- Minimize RMS inductor current.
- Achieve ZCS during switching process on LV side.
- Achieve ZVS operation on HV side.

2.2.2. Three-Phase DAB

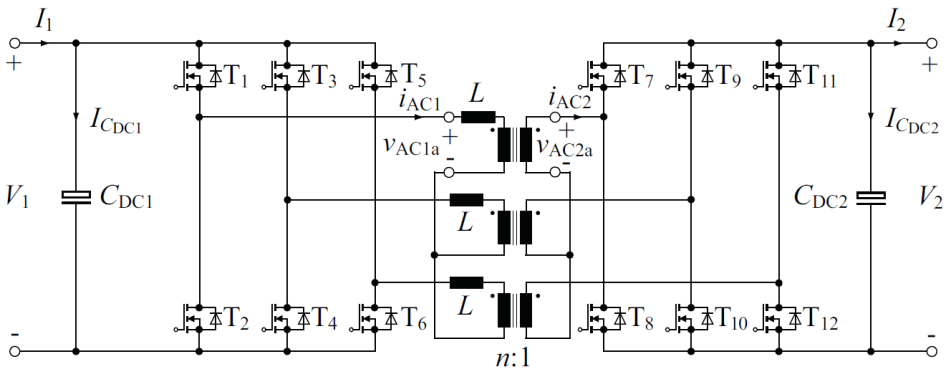

Figure 2.3: Three-phase DAB converter topology, [8]

This topology consists of three half bridges, both on HV and LV side, Figure 2.3. Reactive network consists of an inductor connected in series to HF transformer. Hence, this topology requires three inductors and three HF transformers, or a three-phase HF transformer.

2.2.3. Resonant LLC converter

Within dual bridge converters with resonant network, LLC converter makes reference to Series-Parallel Resonant Converter (SPRC) with a HF network constituted by two inductors and one capacitor. The capacitor is connected in series to the transformer stray inductance.

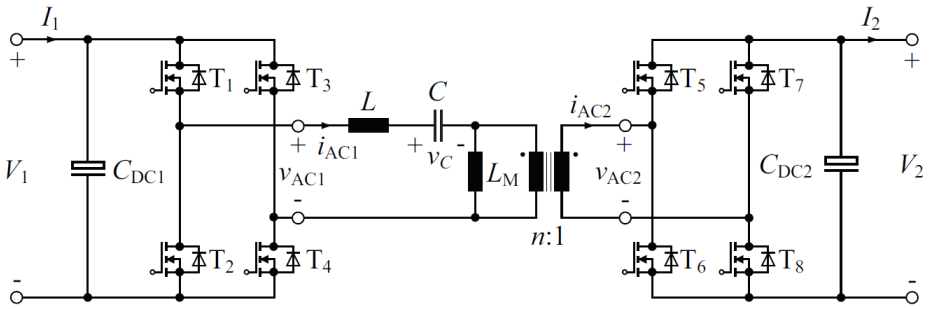

Figure 2.4: Bidirectional, series-parallel resonant LLC converter topology, [8]

In order to obtain bidirectional power transfer, full bridge circuits are used both on HV and LV side.

This topology also accepts alternative modulation schemes, enabling high efficiency in a wide operation range, as in DAB. The main inconvenient of this topology is that for constant frequency operation it is more complex than other topologies that provide similar performances. However, according to [8], this topology can be specially interesting if variable switching frequency is permitted.

2.2.4. Bidirectional and Isolated Full Bridge Converter

This topology presents a voltage sourced full bridge on the HV side and a current sourced full bridge on the LV side (using inductor L_{DC2}). The ZVS operation on HV side and the ZCS on LV side make feasible a high switching frequency and a high power density. This topology requires snubbers on the LV side, at least in boost mode [8], [9].

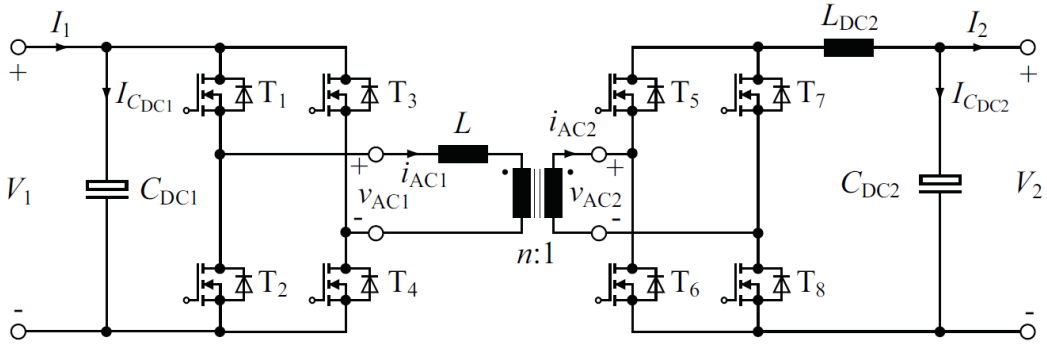

Figure 2.5: Bidirectional and isolated full bridge converter topology, [8]

2.2.5. Bidirectional and Isolated Current Doubler Converter

This topology is a variant of the previous one. Instead of the LV side full bridge converter, this configuration presents a current doubler topology on that side, as shown in Figure 2.6.

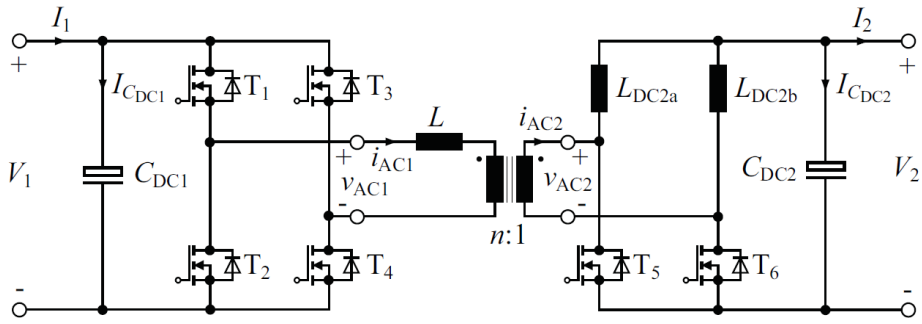

Figure 2.6: Bidirectional and isolated converter with a current doubler on the LV side, [8]

Essentially, current doubler circuit features two inductors instead of one. These inductors replace two of the four switches on LV side. On the one hand, the number of LV switches is reduced to a half, which is desirable because LV switches losses greatly contribute to converter achievable efficiency. On the other hand current doubler circuit requires switches with a rated voltage of twice the rated voltage of the full bridge switches (in the best case).

A derivation of this topology is used in [10]. The main difference is that in [10] more phases are used (multilevel), Figure 2.7.

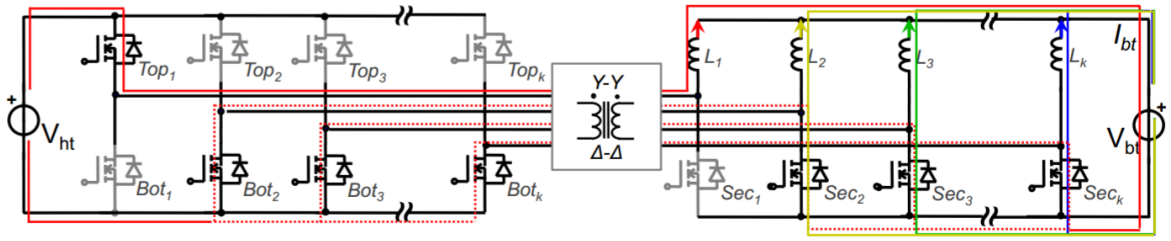

Figure 2.7: Multilevel boost topology derived from current doubler, [10]

An additional issue of this topology is the possible current unbalance between LV inductors (L_{DC}). This might also be an issue in the simple current doubler shown in Figure 2.6.

2.2.6. Bidirectional and Isolated Push-pull Converter

Another variant of bidirectional and isolated full bridge converter consists of replacing the LV side full bridge by a push-pull circuit, Figure 2.8.

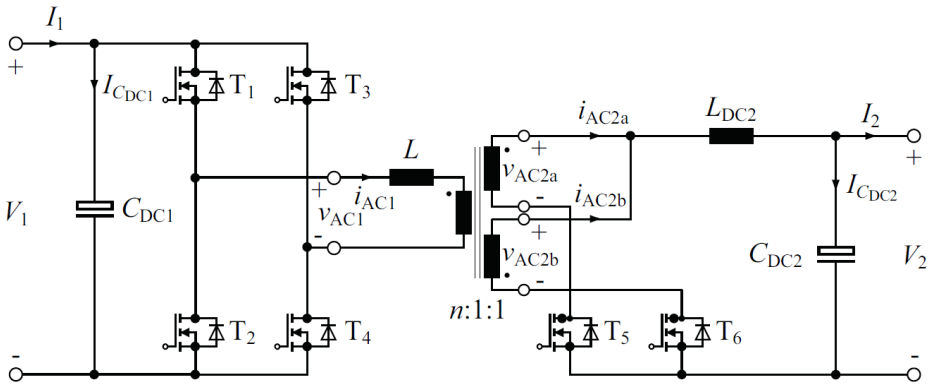

Figure 2.8: Bidirectional and isolated converter with a push-pull circuit on the LV side, [8]

In this case, the push-pull circuit connects to a centre-tapped transformer with two LV side transformer windings. According to [8], the fact that each winding conducts current during half a switching period leads to ineffective transformer utilization.

2.3 Topologies comparison

Topologies comparison are carried out by means of some key magnitudes and performance features that affect the circuit components directly: RMS current, DC current, number of components, VA rating, and so on.

Before doing actual comparison, *VA rating* needs to be defined as suitable comparative magnitude. It expresses electrical stress of component, so that the higher VA rating is, the lower efficiency and/or power density are.

2.3.1. Switches

For each switch this rating is calculated with Equation 2.1, [8]:

$$S_{switch} = \max(V_{switch,peak}) \cdot \max(I_{switch}) \tag{2.1}$$

Where $\max(V_{switch,peak})$ is the maximum voltage applied to the switch and $\max(I_{switch})$ is the maximum RMS current through the switch, [8].

2.3.2. Transformer

For a single-phase transformer with *m* windings operated with sinusoidal voltages and currents, *VA rating* is calculated using Equation 2.2, [8]:

$$S_{tr} = \frac{1}{2} \sum_{i=1}^{m} \hat{V}_{tr,i} \cdot \hat{I}_{tr,i} \tag{2.2}$$

Where $\hat{V}_{\text{tr,i}}$ denotes RMS voltage applied to the *i*-th winding and $\hat{I}_{\text{tr,i}}$ makes reference to RMS current through the *i*-th winding, [8].

Nevertheless, discussed DC to DC topologies do not employ purely sinusoidal waveforms. So the suitable modified expression is Equation 2.3, [8]:

$$S_{tr} = \frac{1}{2} \sum_{i=1}^{m} \hat{V}_{tr,i,eq} \cdot \hat{I}_{tr,i,eq} \tag{2.3}$$

Where $\hat{V}_{\text{tr,i,eq}}$ and $\hat{I}_{\text{tr,i,eq}}$ are defined as Equations 2.4 and 2.5 state, [8].

$$\hat{V}_{tr,i,eq} = \frac{\pi D}{\sqrt{2}} V_1 \tag{2.4}$$

$$\hat{I}_{tr,i,eq} = \hat{I}_{tr,i} \tag{2.5}$$

Regarding mathematical definition above, considered items for comparison are going to be enumerated.

- Number of components.
  - Active ones.
  - Magnetic ones.
- Switches:
  - VA rating sum of LV side.
  - VA rating sum of HV side.
- Transformer:
  - Maximum RMS current.
- Inductors:
  - Maximum DC current.
  - Maximum RMS current.
  - Peak energy.
- Capacitors:
  - Peak energy.
  - RMS current.
- Other considerations:
  - Pre-charge issues.
  - Modulation complexity.
  - Snubber required.

Table 2.1 sums up the final comparison between considered topologies.

Table 2.1: Topologies comparison, [8]

Topology	Advantages	Disadvantages
DAB (Conv. Mod.)	▪ Lowest component count. ▪ Avoids DC inductor. ▪ Simple modulation.	▪ Limited ZVS range. ▪ Transformer large currents. ▪ LV DC capacitor: very large RMS current.
DAB (Opt. Mod.)	▪ Lowest component count. ▪ Avoids DC inductor. ▪ Reduced circulating current. ▪ Reduced capacitor RMS currents. ▪ HV side switches: full range ZVS. ▪ LV side switches: full range ZCS. achievable.	▪ Complex modulation. ▪ LV DC capacitor: large RMS current.
Three-Phase DAB	▪ Comparatively low capacitor RMS currents. ▪ Avoids DC inductors. ▪ Reduced circulating currents.	▪ Limited ZVS range. ▪ High component count. ▪ LV DC capacitor: rahter large RMS currents.
LLC (Conv. Mod.)	▪ Slightly reduced component stresses compared to the DAB. ▪ Avoids DC inductors. ▪ Simple modulation.	▪ Large L and C. ▪ Limited ZVS range. ▪ Transformer: large circulating currents. ▪ LV DC capacitor: very large RMS currents.

Topology		Advantages	Disadvantages
LLC (Opt. Mod.)		■ Avoids DC inductors. ■ Reduced circulating currents. ■ Reduced capacitor RMS currents. ■ HV side: full range ZVS. ■ LV side switches: full range ZCS achievable.	■ Rather large L and C. ■ LV DC capacitor: large RMS currents. ■ Complex modulation.
Full Bridge Converter	*Current Fed Full Bridge*	■ LV side DC capacitor: low RMS currents. ■ HV side: full range ZVS.	■ Large DC inductor required. ■ Snubber may be needed. ■ Limited operating voltage range.
	Current Doubler	■ Lowest transformer currents: lowest losses in contact resistances (e.g. transf. terminal). ■ Lowest switches currents: better MOSFETs available (lower losses). ■ LV side: no high-side gate drivers. ■ LV side DC capacitor: low RMS currents. ■ HV side: full range ZVS.	■ Increased transformer VA rating. ■ Large DC inductors required. ■ Snubber may be needed. ■ Limited operating voltage range.

Topology		Advantages	Disadvantages
	Current Fed Push Pull	■ LV side: no high-side gate drivers. ■ LV side DC capacitor: low RMS currents. ■ HV side: full range ZVS.	■ Increased transformer VA rating. ■ Large DC inductor required. ■ Snubber may be needed. ■ Limited operating voltage range.

Regarding this comparison, a promising power circuit selected for studying is the *Full Bridge with Current Doubler*.

Chapter 3

Working principle description

The topology selected for the study is **Bidirectional and Isolated DC to DC Phase Shift Converter with Current Doubler Rectifier (CDR)**. There are some keywords that contain very important information about this topology.

- *Bidirectional Converter (BDC)*. First, the converter is able to transfer power in both directions. A simple way to achieve this feature would be modify conventional topologies by replacing rectifier diodes with bidirectional switches. Therefore, it is possible for the converter to work in buck mode –HVDC to LVDC –; and boost mode –LVDC to HVDC –.
- *Phase Shift Modulation (PSM)*. Phase shift modulation is an elementary modulation scheme whose parameter control is duty cycle (D).
- *Current Doubler Rectifier (CDR)*. Low voltage side has to withstand high current values. Moreover, the higher power is requested, the higher current is –the voltage level is established by specifications –.

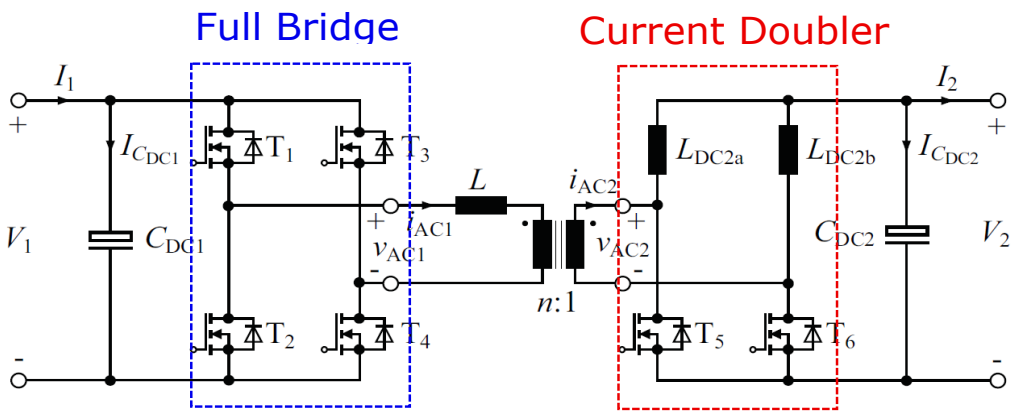

Figure 3.1: Current doubler rectifier original topology, [8]

Figure 3.1 shows the basic topology which meets all those features mentioned above. Nevertheless, a change will be introduced in the topology in order to limit voltage spikes at LV switches (T5 and T6) due to hard turn-off. The resulting topology is shown in Figure 3.2.

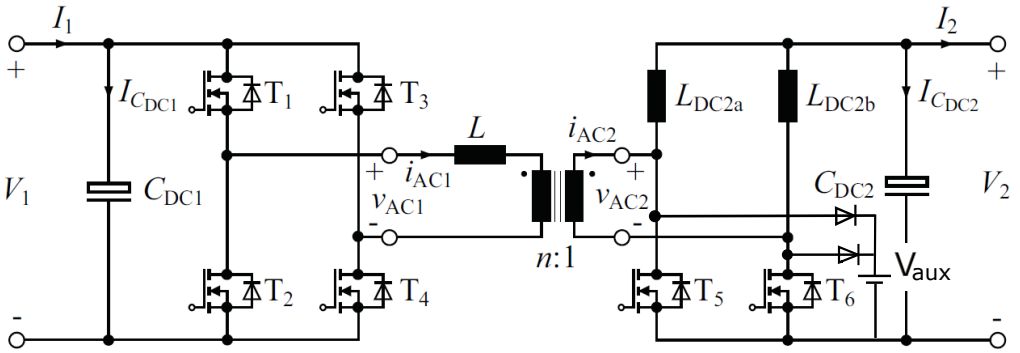

Figure 3.2: Current doubler rectifier modified topology, [8]

It is important to notice that V_1 represents high voltage DC level (HVDC) and V_2 represents low voltage DC level (LVDC).

Looking inside the topology, there is a semiconductors full bridge at HV side and a current doubler at LV side. Transistors are needed instead of diodes in order to make a bidirectional power transfer.

Transformer, represented by two coupled inductors, provides galvanic isolation between high and low voltage sides. Inductor connected in series with transformer

HVDC winding emphasizes the leakage inductance, represented by "*L*".

Regarding the general architecture of bidirectional and isolated DC to DC converter, Figure 2.1, circuit in Figure 3.2 also incorporates a basic filter network consisting of a capacitor connected in parallel with HVDC and LVDC.

Some of these elements have to be dimensioned to meet specifications and design criteria. This aspect will be addressed later.

As explained below, power transfer is controlled by switches states. A modulator turns on and turns off switches according to the PSM technique and its control parameter.

Moreover, some basic ideas must remain as underlying aspects for the current theoretical approach:

- Switches are considered ideal, so switching will be assumed instantaneous. This simplifies performance description and waveform analysis.
- Switches on the secondary side (HV or LV side, depends on the operating mode) are intended to act as power rectifiers. This physical behaviour is called *Synchronous rectification*, SR.

Regarding which side is powered, it is possible to distinguish two basic modes of operation:

- **Boost mode.** LVDC to HVDC.
- **Buck mode.** HVDC to LVDC.

These operating modes are explained in detail separately. For both modes, the following relationship between V_1, V_2 and D applies (Equation 3.1), [11]:

$$D = \frac{2nV_2}{V_1} \tag{3.1}$$

3.1 Steady State Analysis

The study will be carried out with a fixed duty cycle. A basic physical analysis of the circuit will be exposed. The explanation will be carry out considering a switching period (T_S). Four basic states are described during a period.

3.1.1. Buck mode

Turning-on and turning-off the right switches at the right time allows the voltage waveform in the transformer shown in Figure 3.7 which is necessary to perform a voltage reduction (from V_1 to V_2).

Power delivery mode ($t_0 \rightarrow t_1$)

During this time T1 is ON, T2 is OFF, T3 is OFF and T4 is ON. The current flows through active semiconductors in HV side, as it is shown in Figure 3.3. To allow power transfer, T5 is OFF and T6 is ON. This time interval is approximately $D \cdot \frac{T_S}{2}$. [12]

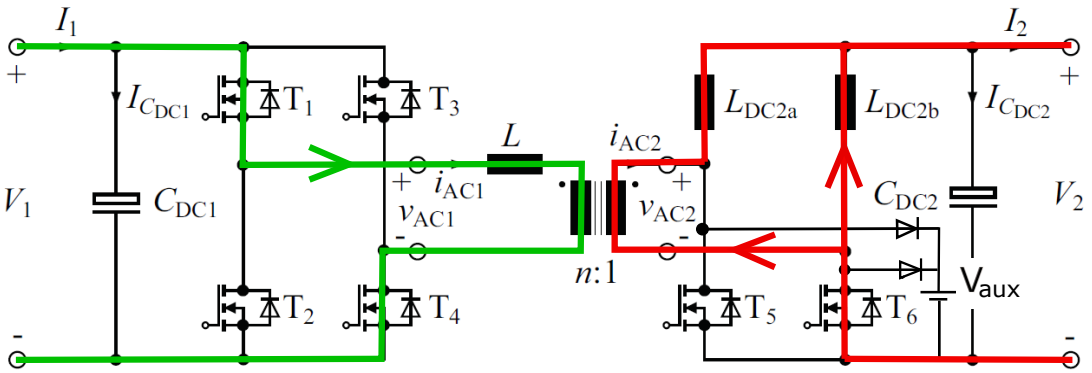

Figure 3.3: Power Delivery Mode, [13]

At this interval of time current through transformer increases. The relation between current and voltage is given by the Equations 3.2 and 3.3.

$$V_{AC1} = V_{AC2} \cdot n + V_L \tag{3.2}$$

$$V_L = L \cdot \frac{dI_{AC1}}{dt} \tag{3.3}$$

This behaviour is verified according to Figure 3.7. The slope of current through transformer is positive.

Freewheeling Mode ($t_1 \rightarrow t_2$)

The next interval of time starts when T4 is turned off. It is characterized by the following HV side semiconductors states: T1 ON, T2 OFF, T3 ON and T4 OFF. In LV side both switches are ON. The current path is drafted in Figure 3.4. [12]

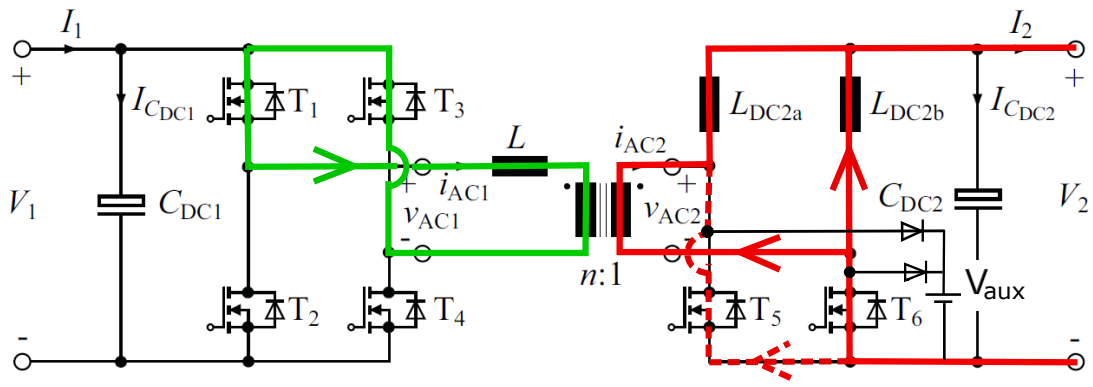

Figure 3.4: Freewheeling Mode, [13]

In this case, there is not net input current. Moreover, the slope of current through transformer is negative. Secondary voltage (V_{AC2}) is closed to zero. This second interval ends at the middle of the cycle, i.e. $\frac{T_S}{2}$.

Power Delivery Mode ($t_2 \rightarrow t_3$)

The third global state of the HV side semiconductor bridge is determined byT1 OFF, T2 ON, T3 ON and T4 OFF. With this configuration input current is allow to flow, as it is shown in Figure 3.5. In this case, T5 is required to be ON and T6 OFF. [12]

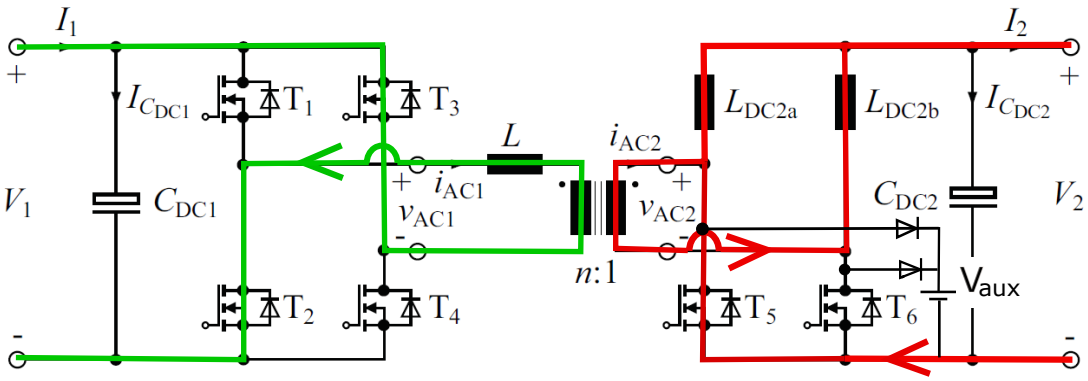

Figure 3.5: Power Delivery Mode, [13]

Current through transformer presents the reverse direction that in the first case (Figure 3.3). This physical behaviour is confirmed with Figure 3.7.

Freewheeling Mode ($t_3 \rightarrow T_s$)

Finally, the last combination of HV switches states is T1 OFF, T2 ON, T3 OFF and T4 ON. Net input current can not exist during this interval. Figure 3.6 shows it. T5 is required to be ON and T6 ON. [12]

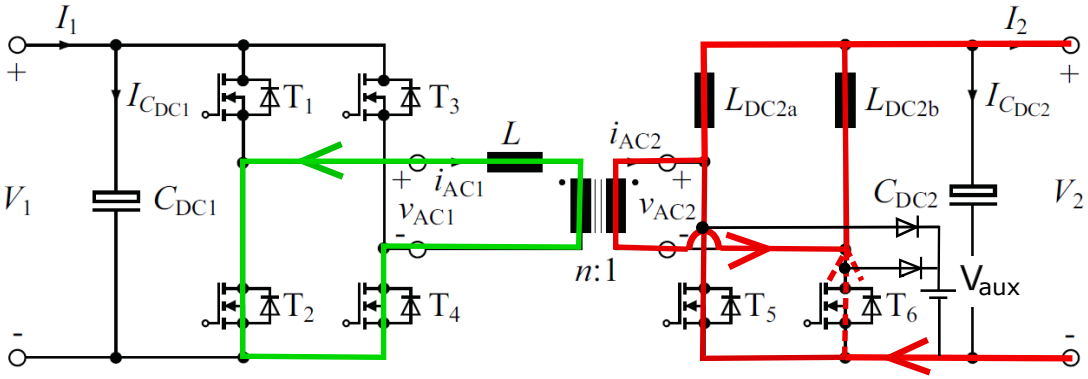

Figure 3.6: Freewheeling Mode, [13]

Fundamental magnitudes illustration

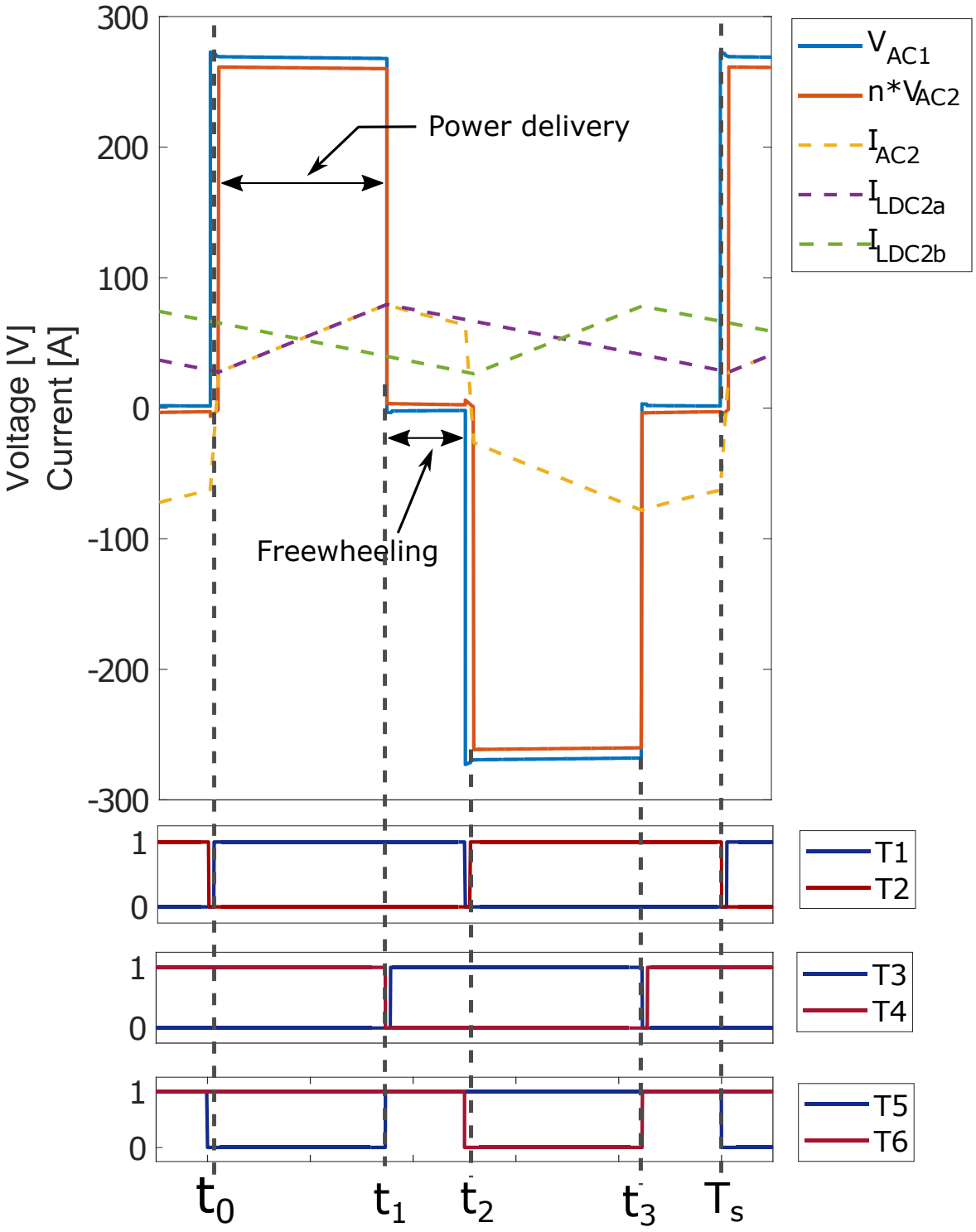

Figure 3.7: Transformer and DC inductors magnitudes - Buck mode

Figure 3.7 allows to understand some details. Effective power transfer to DC inductors takes place when both V_{AC1} and V_{AC2} reach their maximum absolute values. During this time, one of the LV side switches (T5 or T6) are turned off, and hence the current through LV side of transformer is equal to one of the DC inductors. When both LV side switches are ON, there is no power delivery and DC inductors voltage are discharged by the load. [12]

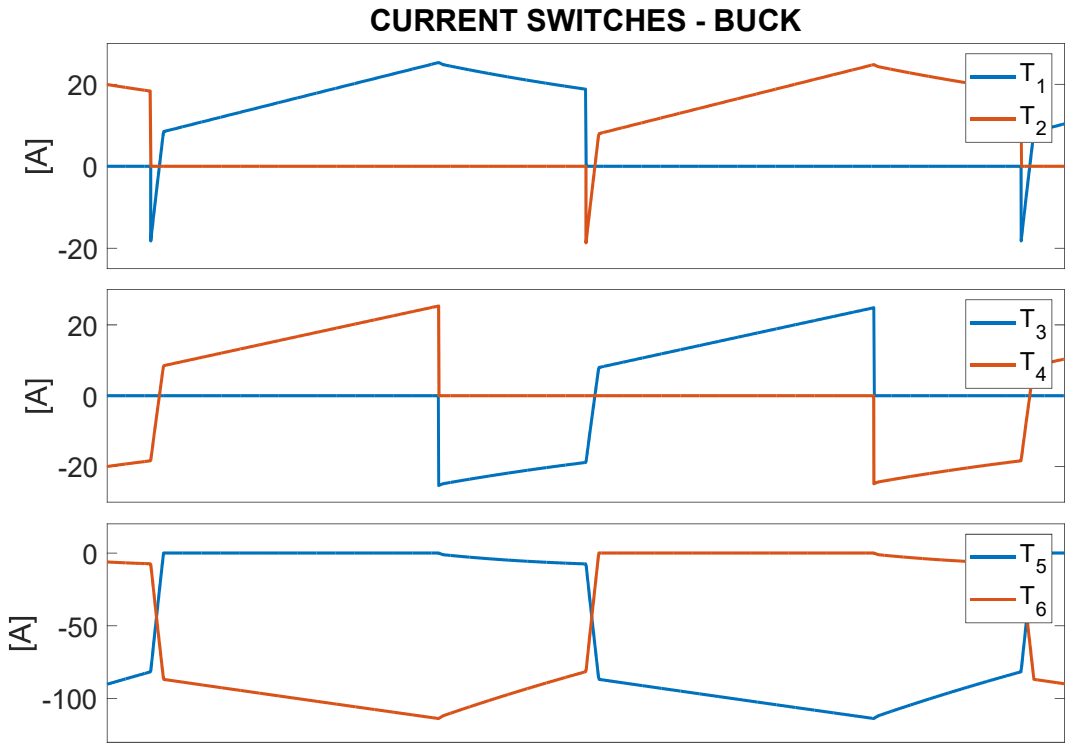

Figure 3.8: Current through switches - Buck mode

Figure 3.8 shows that current through HV switches flows in a different manner in one branch (T1, T2) and in the other (T3, T4).

3.1.2. Boost mode

In boost mode, electric power is transferred from LVDC to HVDC side. CDR topology is unusual to work in this mode of operation, [14] [15].

Following the same structure, a switching period converter performance is analysed. For instance, T_S starts with power delivery time interval. Note that when both switches on LV side are ON power transfer is not possible.

Power Delivery Mode ($t_0 \rightarrow t_1$)

So, in order to allow power transfer during this first time interval, T5 is required to be OFF and T6 is required to be ON; HV side switches have to present the following state: T1 ON, T2 OFF, T3 OFF and T4 ON. Current flow along both side of circuit is shown in Figure 3.9.

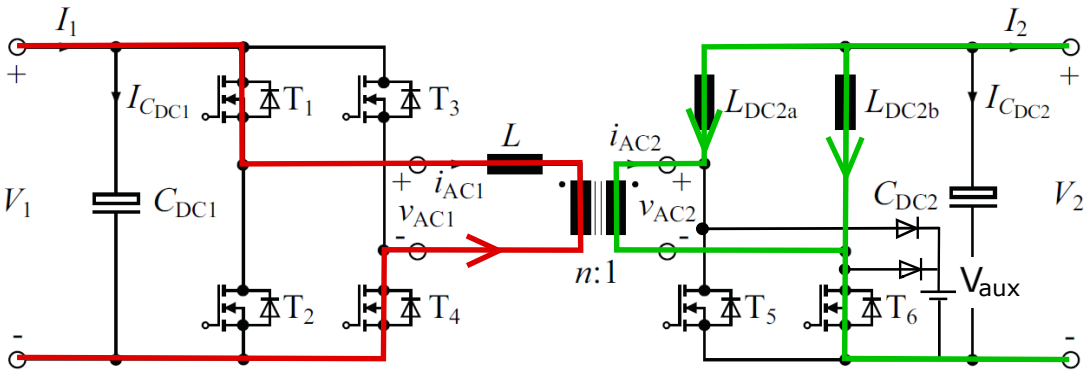

Figure 3.9: Power Delivery Mode, [13]

The beginning of Power Delivery Mode, for each half cycle, always starts with a LV switch turning-off (T5 in this case). As it can be seen in Figure 3.9, I_{AC2} has to reach $I_{L_{DC2a}}$; and since current through switches flows from drain to source in boost mode, voltage spikes, possible destructive, occurs at LV hard turned-off switch meanwhile.

Due to this fact, an active snubber (i.e. clamped diodes connected to an auxiliary voltage source) is added to original topology. During the time when I_{AC2} reaches $I_{L_{DC2a}}$, clamped diodes are conducting current. By this way, voltage in LV switches at hard turning-off is limited to auxiliary voltage source level (V_{aux}) at any case. On the one hand, LV switch has to withstand higher voltage levels than $V_{AC1} \cdot n$ –at least, V_{aux}–; on the other hand, clamped diodes protect them from voltage spikes.

Safety principle strongly suggests to leave a safety margin at V_{DS} switch maximum rating regarding V_{aux}. See Table 5.4.

This phenomena would be avoided with an advanced modulation technique.

Freewheeling Mode ($t_1 \rightarrow t_2$)

The next interval time extends up to the first half of T_S. Current through transformer has reversed its sense. LV side switches state is: T5 ON and T6 ON. During this interval V_{AC2} is almost zero .HV side bridge state is: T1 ON, T2 OFF, T3 ON and T4 OFF.

Behaviour of circuit during this interval is shown in Figure 3.10.

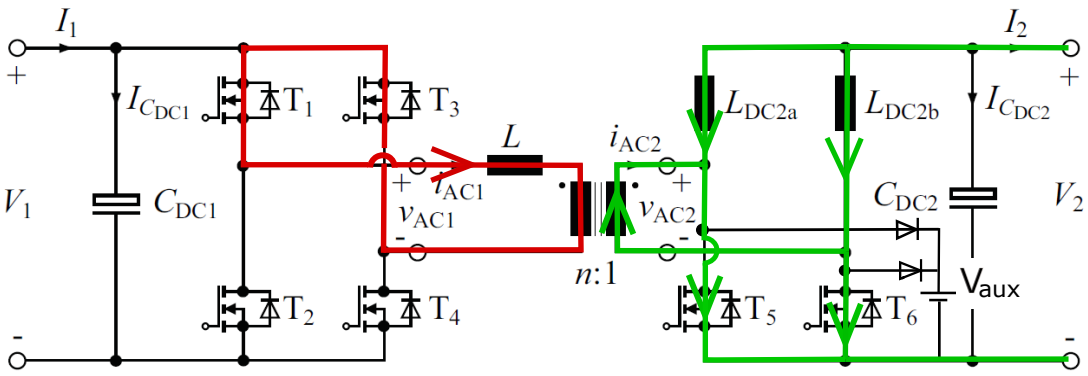

Figure 3.10: Freewheeling Mode, [13]

Power Delivery Mode ($t_2 \rightarrow t_3$)

During the third interval of time considered a power transfer process is carried out again. Switches are setting in the following manner: T1 OFF, T2 ON, T3 ON, T4 OFF, T5 ON and T6 OFF.

An schematic diagram of the circuit is presented in Figure 3.11.

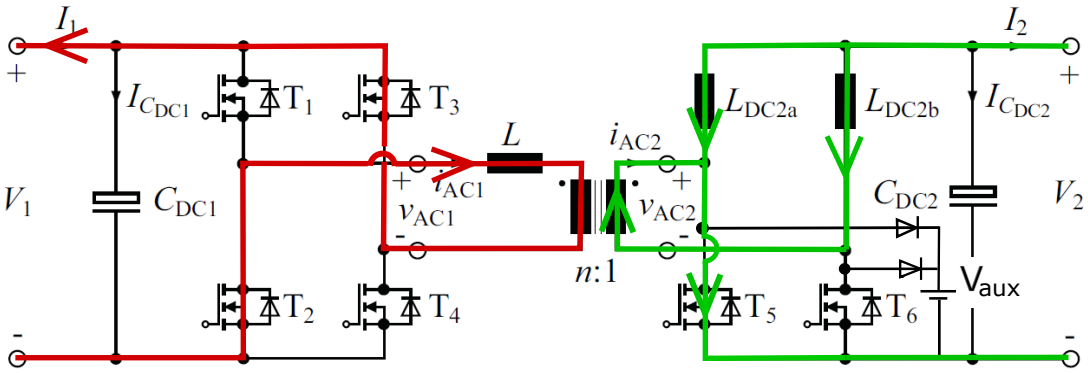

Figure 3.11: Power Delivery Mode, [13]

Freewheeling Mode ($t_3 \rightarrow T_s$)

During the last interval there is not net output current. Both T5 and T6 are ON, and in the HV side T1 is OFF, T2 is ON, T3 is OFF and T4 is ON. See Figure 3.12.

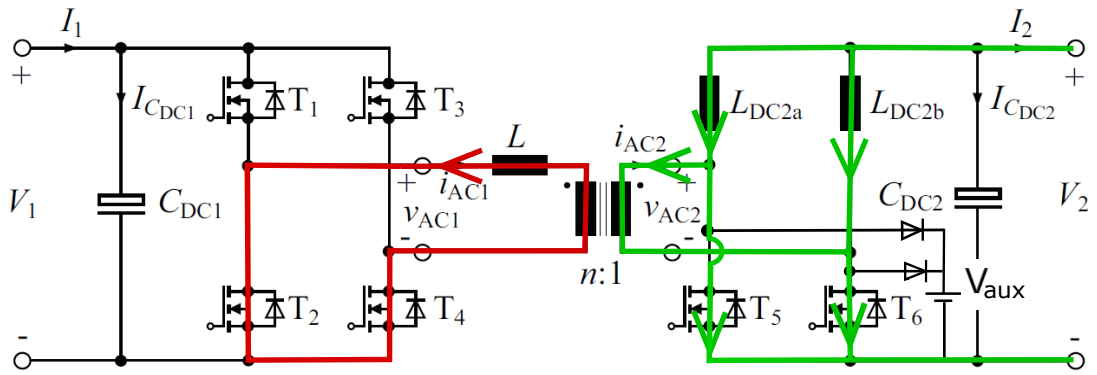

Figure 3.12: Freewheeling Mode, [13]

Fundamental magnitudes illustration

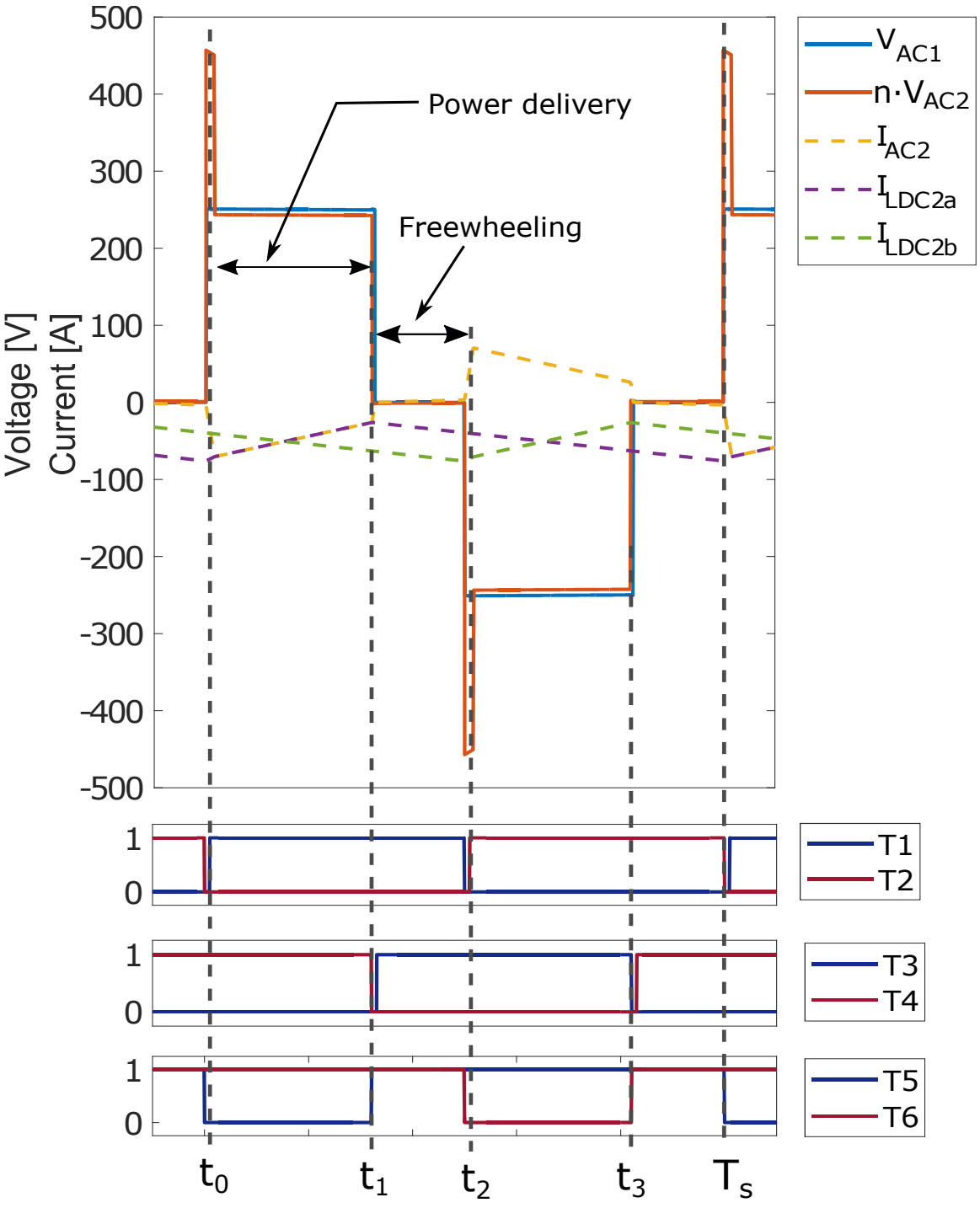

Figure 3.13: Transformer and DC inductors magnitudes - Boost mode

In the first place, it is quite apparent that in boost mode diodes allow current to flow during short interval time; this phenomena results in an overvoltage on LV side of the transformer. Overvoltage does not appear in Figure 3.7. The maximum value is limited by active snubber auxiliary circuit, i.e. clamped diodes and V_{aux} which is set to 150 V.

Transformer current waveform is also different in boost and buck mode. During power delivery mode, current decreases -regarding absolute value- in boost mode and increases in buck mode. During freewheeling period this magnitude is closed to zero in boost mode, and it is not in buck mode.

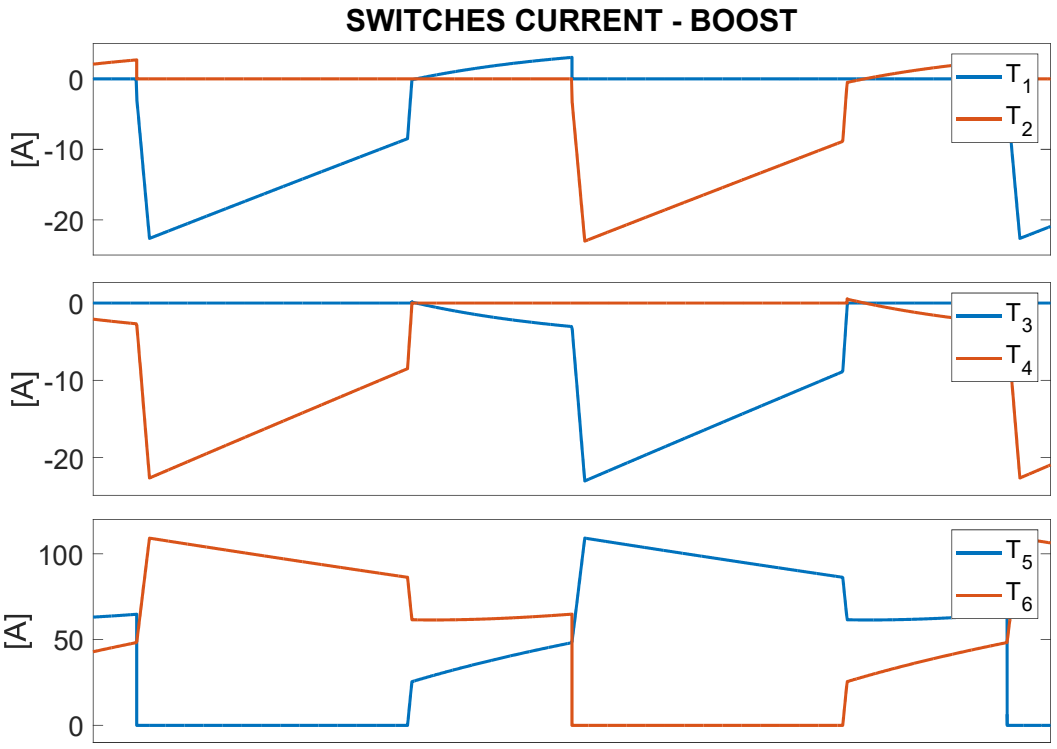

Figure 3.14: Current through switches - Boost mode

In boost case, current waveforms of (T1, T2) and (T3, T4) are more similar each other than in buck case.

3.2 Phase-Shifted Modulation

In this section modulation technique is outlined briefly. The basic control principles are described:

- Switches in the same leg never are switched on at the same time. Hence, the duty cycle between them is almost 50%, because it is necessary to keep a delay time, also called *dead time*, between the switch-on of one and the switch-off of the other -of the same branch-.
- Switches pairs of the two legs of HVDC full bridge are delay certain time. This time is controlled with a parameter called *duty cycle*, D, and it depends on operating point. From a physical point of view, power transfer occurs during this time.
- Switches on LVDC side are controlled according to SR control strategy.

The code that implements phase-shifted technique is attached in Appendix A.2.2.

There are modulation strategies that can achieve loss reduction in some operating points; two of them are described below.

Moreover, there could be some modulation scheme that improve switching process in boost mode. It will be discussed in Chapter 9.

3.2.1. Soft Switching

Basic requirements of converters are high efficiencies and small sizes. Increasing switching frequency may allow to reduce size, [16], but by this way switching losses also raise. A solution for this problem could be use soft switching techniques, [16], such as Zero Voltage Switching (ZVS) or Zero Current Switching (ZCS). [17].

Switching losses are due to drain current and drain to source voltage overlap and discharge of stored energy in C_{oss}. During ZVS, current at turn on is oriented from source to drain, which discharge MOSFET output capacitance before turning the device on, [18]. By this way, V_{DS} goes closed to zero before semiconductor begins to conduct, hence switching on losses are nearly eliminated. Notice that switching off losses remain with ZVS. In the HV bridge, ZVS can be achieved when, after a hard

turn-off, the current in the leakage inductance did not change its sign after dead time. In this manner, at turn-on, leakage inductance is circulating through the off mosfet, and ZVS can be achieved.

To allow wide ZVS range, the modulator dead time must be large enough to avoid cross conduction, but short enough to avoid L sign change.

3.2.2. Synchronous Rectification

Current MOSFETs technology allow lower voltage drop compared to diodes, so rectification becomes more efficient when current flows through the first ones. This technique require high modulator precision: switches should be open exactly during the time they are not conducting. Moreover this issue, there are some design trade-offs implementing SR, [19], [20].

3.2.3. Detailed modulation scheme

The concrete scheme of PSM implemented is shown in Figure 3.15.

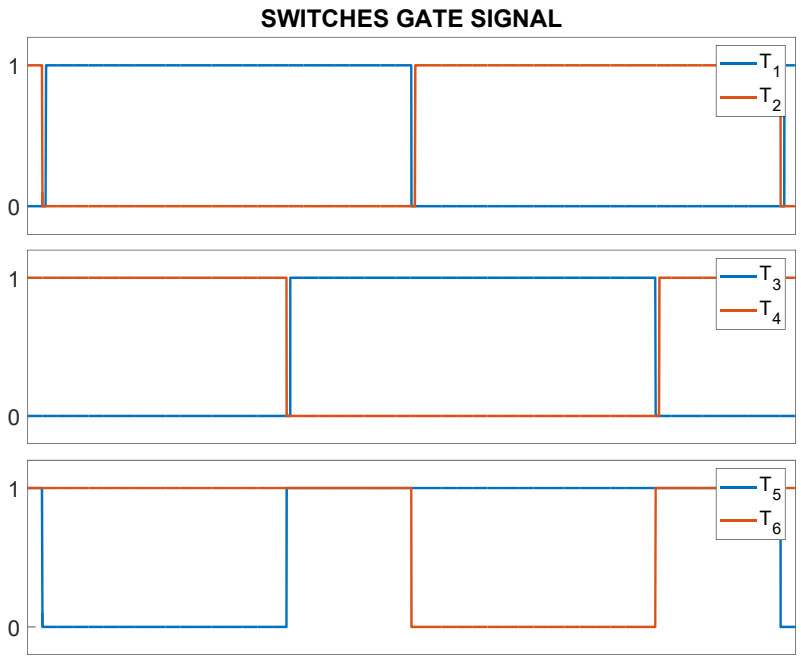

Figure 3.15: Switches logic gate signal

Notice that there is a time between the switch turn-off and the turn-on of the other same-branch switch. A fine tune of it, usually called *dead time*, is crucial because this parameter affects to several aspects of converter performance (avoiding short circuit, achieving ZVS).

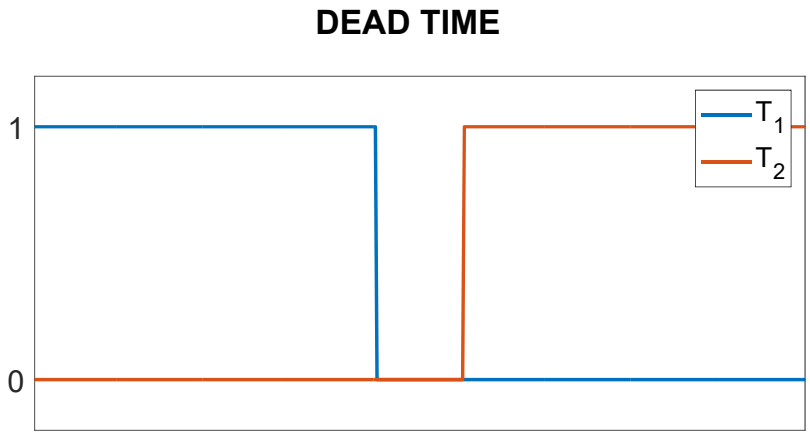

Figure 3.16: Dead time

As it appears in Figure 3.16, between T1 turn-off and T2 turn-on there is a time during which both logic gate signals are "OFF" because real switches -for instance, MOSFETs- need to discharge and charge, respectively, gate-source capacitances to reach a real "OFF" or "ON" state.

Scheme modulation proposed in Figure 6.5 allows to get, in buck mode:

- Synchronous rectification.
- ZVS in almost the whole operating domain.

Nevertheless, dead time has to be calculated accurately in order to guarantee ZVS and SR, when it is possible.

In boost mode none of these enhancement strategies have been reached with the modulation profile used.

Chapter 4

Specifications and criteria design

The criteria design has been established based on operating range (Section 4.1 and 4.2) and some design assumptions taken from [8] (Section 4.3).

4.1 Operating points

In first place, domain for input variables is specified in Table 4.1.

Table 4.1: Design voltage thresholds

Magnitude	Buck operating mode	Boost operating mode
V_1 [V]	235 < V_1 < 325	250 < V_1 < 360
V_2 [V]	22 < V_2 < 30	22 < V_2 < 30
P [W]	0 < P < 3000	-3000 < P < 0

4.2 Nominal operating point

In second place, nominal operating point is defined in Table 4.2.

Table 4.2: Nominal operating point

V_1 [V]	V_2 [V]	P [W]
270	28	$\pm$3000

4.3 Additional design criteria

In third place, it will be necessary to include some assumptions, taken from [8].

- T_C is less or equal than 7.5%T_S.
- T_{free} is less or equal than 2.5%T_S.
- Δ $I_{LDC2a+2b}$ is less or equal than 40%$\frac{P_2}{V_2}$

Chapter 5

Components design

5.1 Transformer

5.1.1. Simple model

Simple model, as discussed below, only considers n and L.

Turn ratio

In order to estimate n, the next steps have been followed.

First of all, a relationship between V_1, V_2, n and D has been taken into account, Equation 3.1.

Regarding D definition, it is obtained the following expression.

$$D = \frac{t_{on}}{T_S} = 1 - 2f_s(T_C + T_{free}) \tag{5.1}$$

By replacing T_C and T_{free} with their maximum values in Equation 5.1, the maximum achievable value ofD is reached.

Then, setting minimum value of V_1 and maximum value of V_2 in Equation 3.1,

the maximum value of n that can be used is obtained.

$$n = \frac{V_{1\,min}}{2V_{2\,max}} \cdot [1 - 2f_s \cdot (T_C + T_{free})] \tag{5.2}$$

Maximum admissible value for n results:

Table 5.1: Transformer turn ratio results

Buck mode	Boost mode	Design value
$n_{min_{buck}} = 3.1333$	$n_{min_{boost}} = 3.3333$	n = 3

Leakage inductance

A suitable design criteria for leakage inductance would be to extend as far as possible ZVS condition. It is intended to reduce current variation during switching process.

- L = 1.5 μH

The proposed value has also been set according to [12], which consider the same basic design criteria and operating conditions closed to nominal operation point, Table 4.2

5.1.2. Advanced model

Turn ratio is the only needed parameter for the ideal transformer model. Actually, transformers present losses both in the core and in windings due to multiple effects (hysteresis, ohmic losses, Eddy currents). Moreover, at high frequency transformer model has to be completed with parasitic capacitances.

In this research, the only parameter takes into account in a more advanced design is magnetizing inductance, L_m. A typical value of L_m is presented below.

- L_m = 1 mH

Including L_m explicitly allows to check that current through transformer core has zero value average and hence the core is unsaturated.

5.2 DC Inductor

5.2.1. Simple model

Inductance of DC inductors is directly related with peak-to-peak value of LV side current. Hence, in order to estimate these inductances, the following assumption has been made.

$$\Delta I_{LDC2a+2b} \leq 40\% \cdot \frac{|P_2|}{V_2} \tag{5.3}$$

Regarding peak-to-peak current definition and assuming an ideal behaviour, $\Delta I_{LDC2a+2b}$ may be expressed as it follows.

$$\Delta I_{LDC2a+2b} = max[i_{LDC2a}(t) + i_{LDC2b}(t)] - min[i_{LDC2a}(t) + i_{LDC2b}(t)] = \frac{(V_1/n - V_2) \cdot (D/2)}{f_s \cdot L_{DC}} \tag{5.4}$$

Imposing the additional condition:

$$L_{DC2a} = L_{DC2b} = L_{DC} \tag{5.5}$$

Combining 5.3, 5.4 and 5.5, the following expression for DC inductor is obtained.

$$L_{DC2a} = \frac{D/2}{f_s \cdot \Delta I_{LDC2a+2b}} \cdot (\frac{V_1}{n} - V_2) \tag{5.6}$$

The aim is to find the minimum value that fulfils Equation 5.3 at the worst operating condition.

$$L_{DC2a_{min}} = \frac{D/2}{f_s \cdot 40\%|P_2|/V_2} \cdot max(\frac{V_1}{n} - V_2) \tag{5.7}$$

Regarding nominal power (see Chapter 4, Table 4.2) and Equation 3.1, the following numerical results have been obtained:

Table 5.2: DC inductor results

Buck mode	Boost mode	Design value
$L_{DCmin_{buck}}$ = 3.35 μH	$L_{DCmin_{boost}}$ = 3.66 μH	L_{DC} = 3.7 μH

5.2.2. Advanced model

Advanced design of DC inductors involves adding a series resistance with the inductance in order to include ohmic losses.

- R_{LDC} = 0.5 mΩ

5.3 Switching frequency

Switching period (T_S) is related directly with switching frequency trough well-known Equation 5.8:

$$T_S = \frac{1}{f_s} \tag{5.8}$$

This parameter affects strongly all the components (magnetics, semiconductors acting as switches), especially when frequency reaches high values. It will be set at 100 kHz, and hence the switching period is 10μs.

Selected f_s is a reasonable value according to nominal operating point, Table 4.2, [19], [12]. Choosing f_s involves design trade-off's. On the one hand, higher f_s allows to reduce magnetic components size, [16]. On the other hand, the higher f_s, the higher switching losses are and also the higher EMI tends to be, [21]; more switching losses involve more dissipated heat and hence bigger heat sinks. Again, a trade-off decision.

5.4 Auxiliary voltage source and clamped diodes

5.4.1. Simple model

Auxiliary voltage source

Voltage source connected to clamped diodes has to fulfil the following condition:

$$V_{\text{aux}} \geq \frac{V_1}{n} \tag{5.9}$$

Regarding the maximum value of V_1, 120 V, the value has been set to 150 V.

Clamped diodes

Diode behaviour is modelled regarding only two electric features: forward voltage drop and ohmic conduction resistance.

- $V_{d_{\text{clamped}}} = 1.45$ V

5.4.2. Advanced model

Advanced model only takes into account conduction resistance of diodes.

Clamped diodes

- $R_{d_{\text{clamped}}} = 14.5$ mΩ

Both are realistic values for power diode regarding V_{aux} voltage level, [22].

5.5 Switches

5.5.1. Simple model

As a starting point, switches will be considered ideal both for physical working description of the converter, Chapter 3, and for an initial numerical simulation, in order to obtain starting results.

Simple model includes few non-idealities such as:

Parameter	LV side	HV side
R_{DSon}	10 mΩ	40 mΩ
$V_{d_{switch}}$	1.2 V	1.2 V

Table 5.3: Quasi-ideal switches parameters

5.5.2. Advanced model

Component selection is an iterative process during the overall design. Hence, according to obtained results based on simple model, which are shown in Chapter 7, MOSFETs referenced below are suitable for the application considered in this project.

Table 5.4: MOSFETs characteristics, [23], [24], [25]

Parameter	HV MOSFET	LV MOSFET
Supplier	Cree | Wolfspeed	Infineon Technologies
Model reference	C3M0030090K	IPB200N25N3 G
Technology	Silicon Carbide (SiC)	Silicon (Si)

ON Resistance I_{DS}, V_{GS}	36 mΩ 35 A, 15 V	36.25 mΩ 64 A, 10 V
Threshold voltage	1.875 V	2.2 V
Internal source resistance	1.42 mΩ	0.878 mΩ
Internal drain resistance	77.52 $\mu\Omega$	50 $\mu\Omega$
Parasitic capacitances [C_{iss}, C_{oss}, C_{rss}] at V_{DS} = 360 V	[1750, 150, 9.5] pF	[5340, 240, 4] pF
Body diode forward voltage drop	5 V	0.8
ON Resistance body diode	166.7 mΩ	12.5 mΩ
λ	0.01	0.25

Notice that breakdown voltage of LV MOSFET is considerably higher than clamped voltage, Section 5.4.

Advanced model also considers a passive RC snubber circuit in parallel with LV switches, see Figure 5.1. Passive snubber circuit function consists on reducing over-voltage at LV switches and avoiding as far as possible an oscillating behaviour of V_{DS} when switch is turned-off. During switching, parallel snubber capacitance is charged and discharged, and snubber resistance acts as damping element.

This oscillation is due to resonance between transformer leakage inductance and MOSFET output parasitic capacitance (C_{oss}).

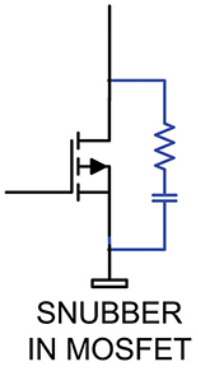

Figure 5.1: Passive snubber in parallel with LV switches, [26]

For setting snubber resistance and capacitance values, the next criteria design has been considered:

- Resistance. Some reasonable values has been tested. Final value is obtained from an iterative process.

$$R_{snb} = 5\ \Omega$$

- Capacitance. Design criteria laves a safety factor of 10 over the total output capacitance (C_{oss}) of the switch, regarding that each LV switch is compound of eight MOSFETs.

$$C_{snb} = 20\ nF$$

Chapter 6

Simulation models and Software tools

The chosen software to perform simulation has been MATLAB/Simulink. It is a well-known simulator that owns multiple solver and allows to elaborate models with different degree of complexity, since it provides some libraries with different model accuracy.

6.1 MATLAB/Simulink Models

The approach has been to begin with a simple model which includes the main parameters of all the components, and then, in a second stage, to develop a more advanced model taking into account components loss and parasitic effects.

6.1.1. Simple model

Figure 6.1 shows the initial version of the numerical model. It has been built with *Simscape/Power Systems/Specialized Technology* Simulink library.

Component parameters have been set according to description in *Simple model*

subsections of Chapter 5.

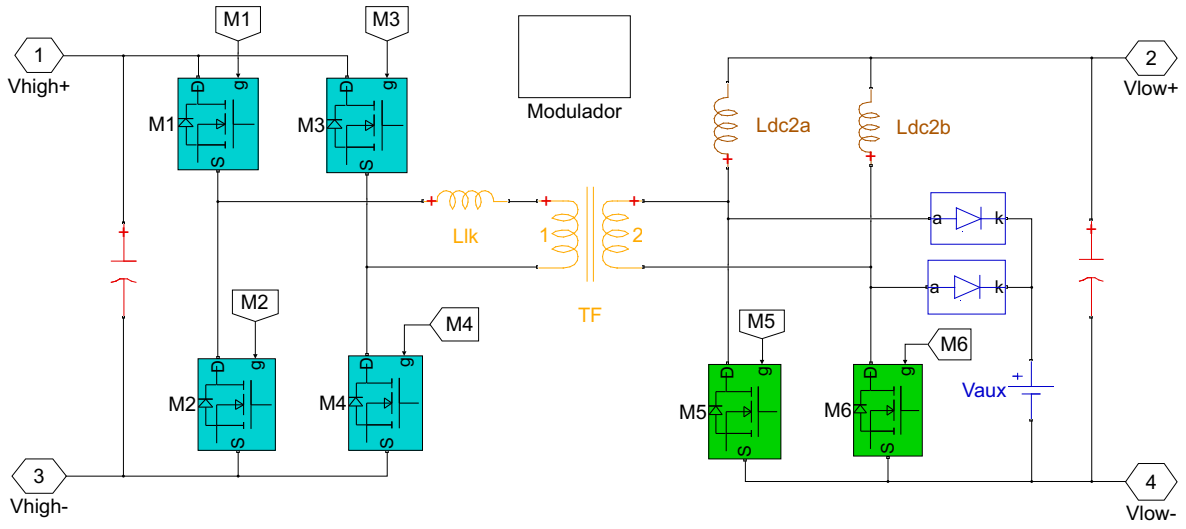

Figure 6.1: Basic MATLAB/Simulink model

6.1.2. Advanced model

A more specific Simulink library has been used to develop an accuracy numerical model. In this case, it is *Simscape/Electronics* Simulink library.

Diodes and L_{DC} incorporate ohmic resistances and hence these models include ohmic losses. Transformer magnetizing inductance is also taking into account.

But, above all, switches are modelled as real semiconductors -MOSFET in this case- with ohmic losses and also parasitic effects. In this case, listed parameters in Chapter 5, Section 5.5 have been added to the model and realistic effects have been taking into account, such as parasitic inductance due to MOSFETs package and switches layout. Figures 6.2 and 6.3 illustrate it.

To see concrete values, go to Chapter 5.

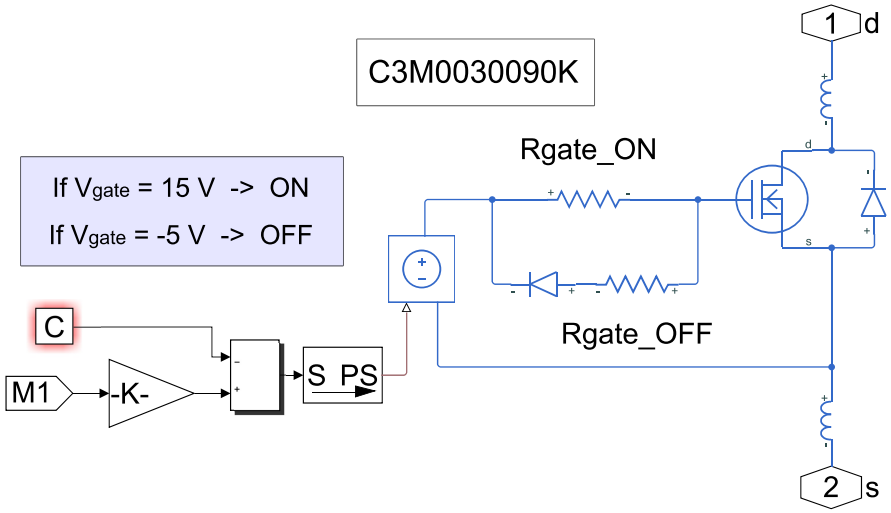

Figure 6.2: HV MOSFET model with parasitic effects

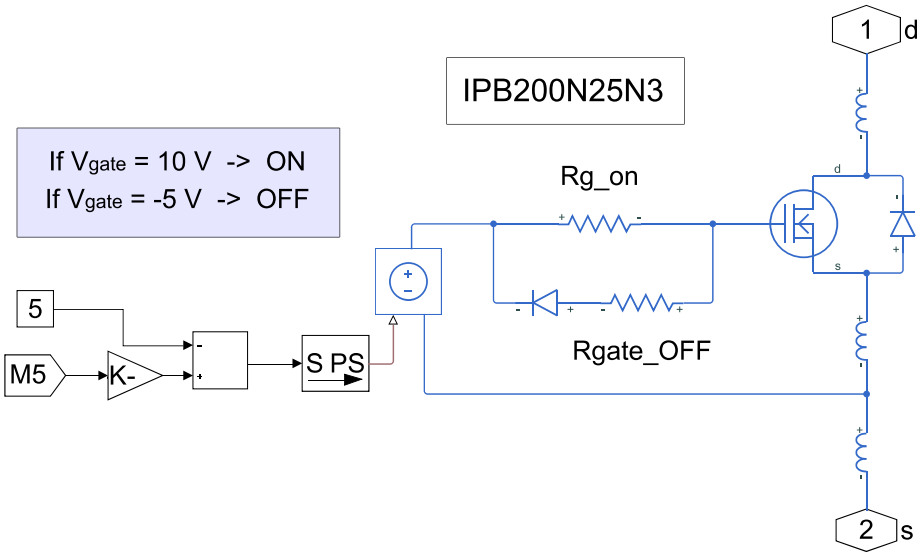

Figure 6.3: LV MOSFET model with parasitic effects

Face to results that will be obtained with advanced model, it should be noted that at HV side each switch is compound by one single MOSFET, whereas at LV side each switch is compound by eight MOSFETs connected in parallel. This consideration is also important because results under actual operating conditions will be different to what it will be obtained with simple model.

Both models, simple one and advanced one, have been implemented so that buck and boost simulations can be programmed. It has been achieved using ideal circuit breakers that activate and deactivate pertinent voltage source and load in each case. Circuit breakers state are preset before simulation calling a parameter function. A programming example is given in Appendix A.2.1.

6.2 Modulator

Modulator has the same design for both models.

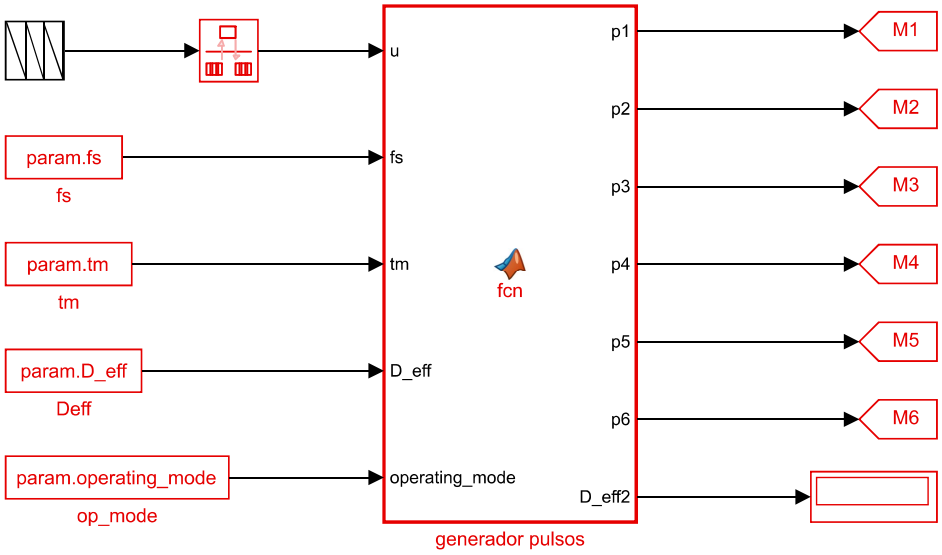

Figure 6.4: Simulink block diagram of Modulator

Modulation programming has been carried out time independently. Comparing periodic reference triangular waveform which depends on switching frequency and constant values according to Figure 6.5 is possible to generate switches gate signal.

Figure 6.5 clarifies this idea. To certain timed value, e.g. t = 0.5·$D \cdot T_S$, corresponds an specific vertical value, regarding relationship between similar triangles.

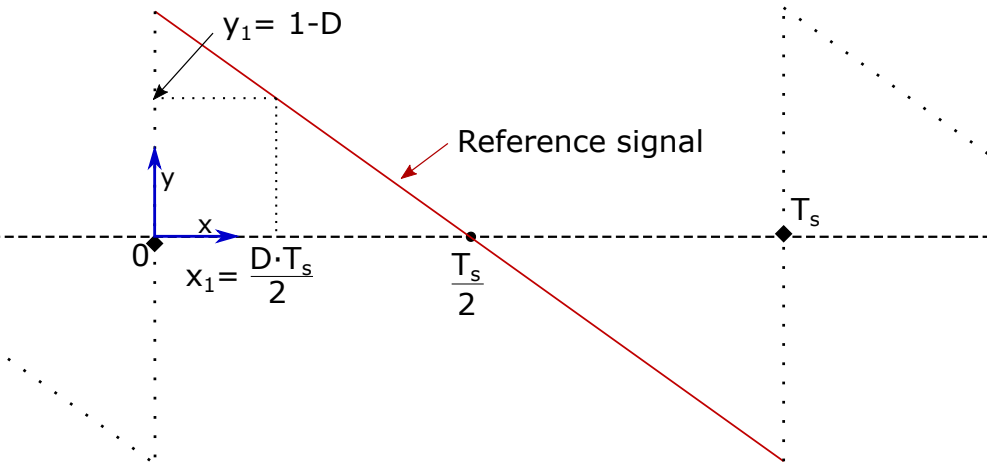

Figure 6.5: Gate signal generation principle

Modulator code is attached in Appendix A.2.2.

Chapter 7

Results

Just as in the previous chapter, the content of this one are divided into two categories: results coming from Simple model and results coming from Advanced model.

7.1 Simple model results

Figures from 7.1 to 7.16 have a double objective. On the one hand, they reveal circuit performance patterns when input and output voltage level are modified. On the other hand, by knowing certain magnitudes help to make a preliminary sizing of components and also would allow to do an efficiency estimation. Choosing suitable semiconductors -MOSFET in this case- to carry out switching function is particularly crucial.

7.1.1. Switches

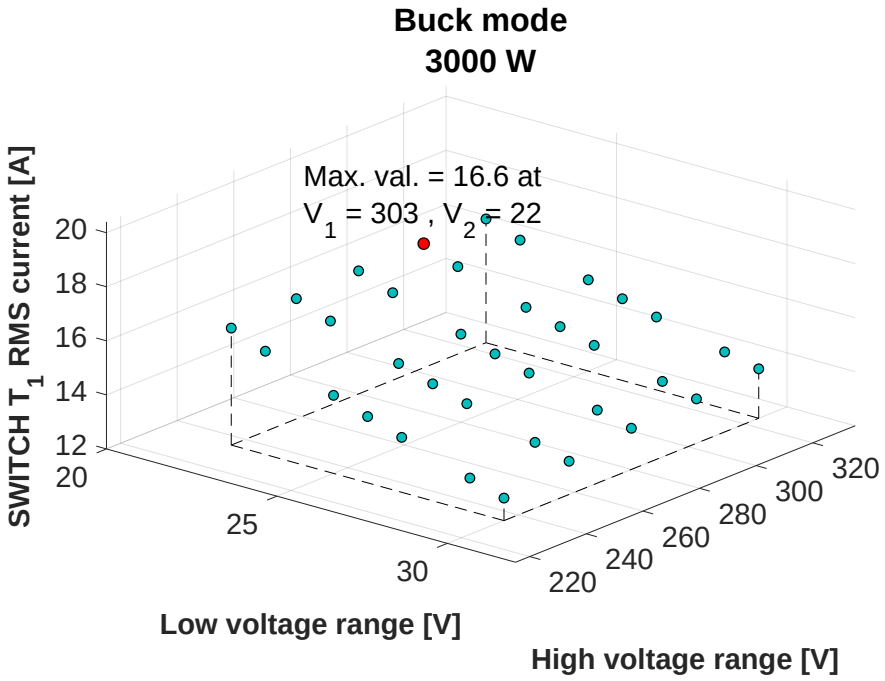

Figure 7.1: Current through HV side switches in buck mode operation

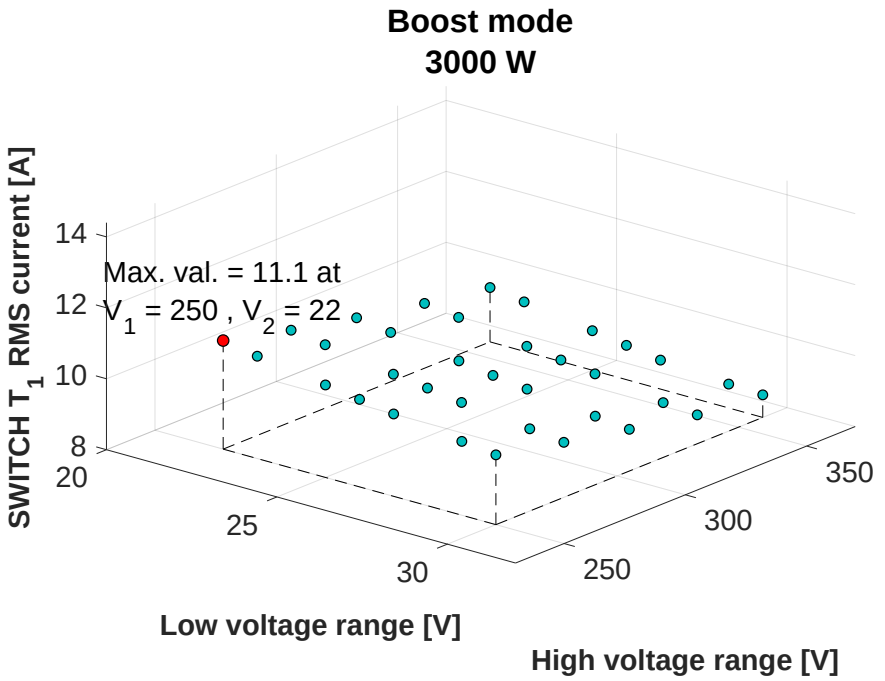

Figure 7.2: Current through HV side switches in boost mode operation

Figures 7.1 and 7.2 show RMS current through respective switches, and they also point maximum values -red ball-. Maximum RMS currents are: 16.6 A in buck mode and 11.1 A in boost mode.

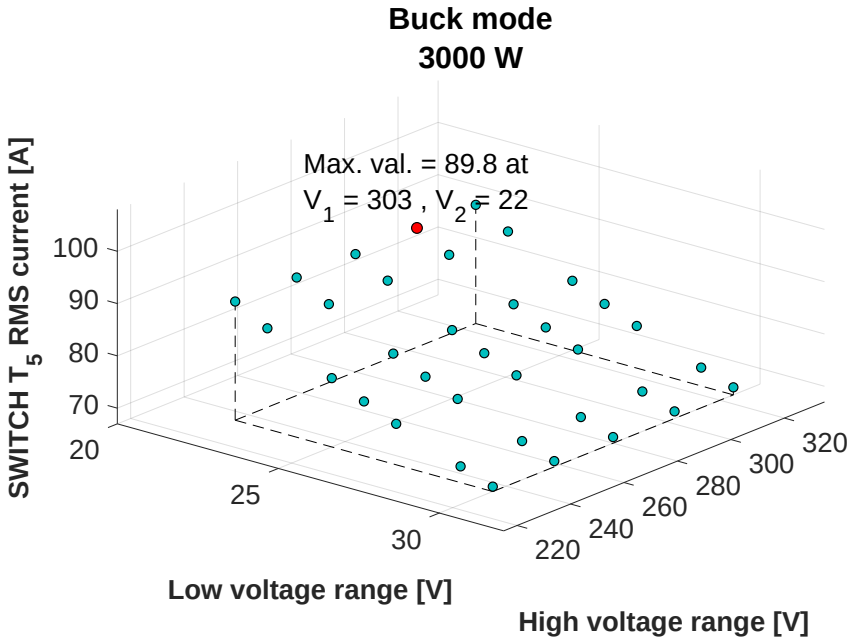

Figure 7.3: Current through LV side switches in buck mode operation

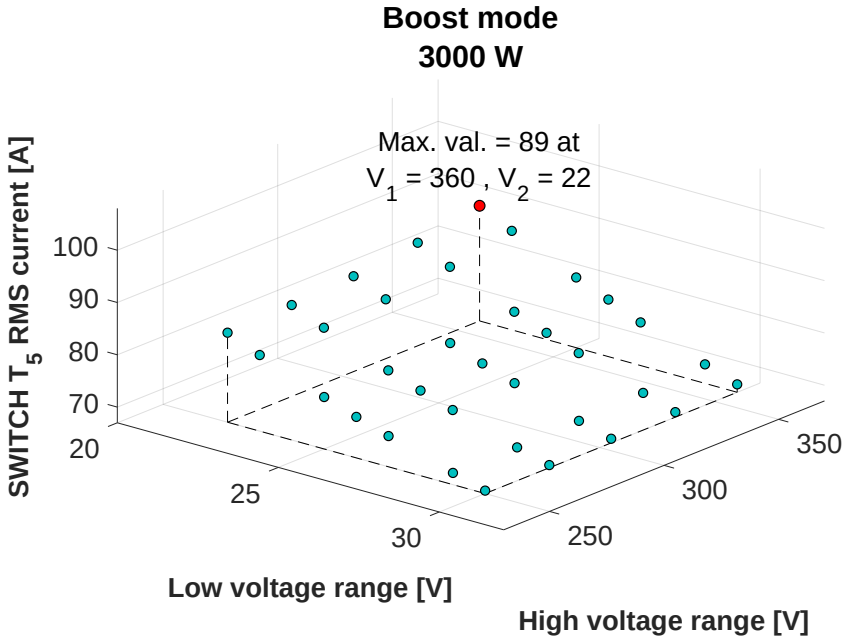

Figure 7.4: Current through LV side switches in boost mode operation

Figures 7.3 and 7.4 show RMS current through LV switches. Current is much higher than in HV switches clearly. Maximum values are: 89.9 A in buck mode and 89 A in boost mode.

Knowing maximum RMS help to select suitable real semiconductors for switches. Moreover, this maximum values, together with voltage drop, would allow to estimate maximum VA ratings for switches. Information obtained from this preliminary results and nominal operating point specifications (Chapter 4) justify MOSFET selection for both HV and LV sides. To see their main characteristics in detail, go to Chapter 5, Section 5.5.

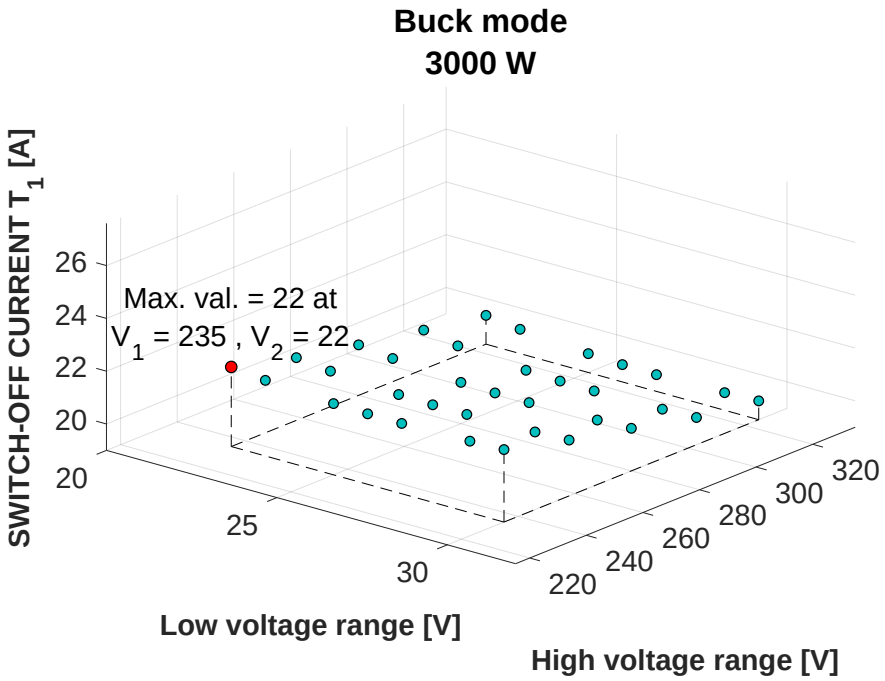

Figure 7.5: Current at SWITCH-OFF on HV side switches in buck mode operation

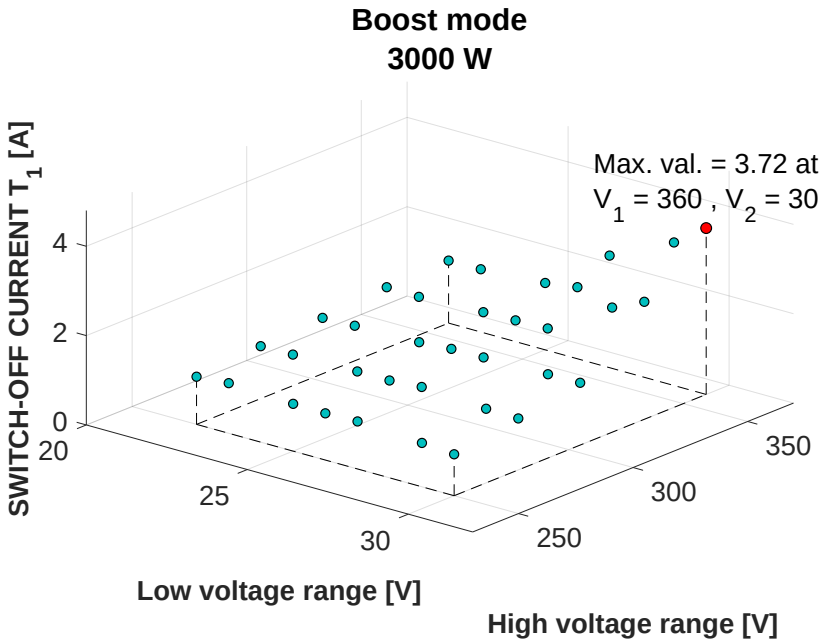

Figure 7.6: Current at SWITCH-OFF on HV side switches in boost mode operation

Figures 7.5 and 7.6 present current at the switching-off instant for HV switches. In boost mode this current is very low -the maximum value reached is 3.72 A-, whereas un buck mode it is higher, from 20 to 22 A -maximum value reached is 22 A.

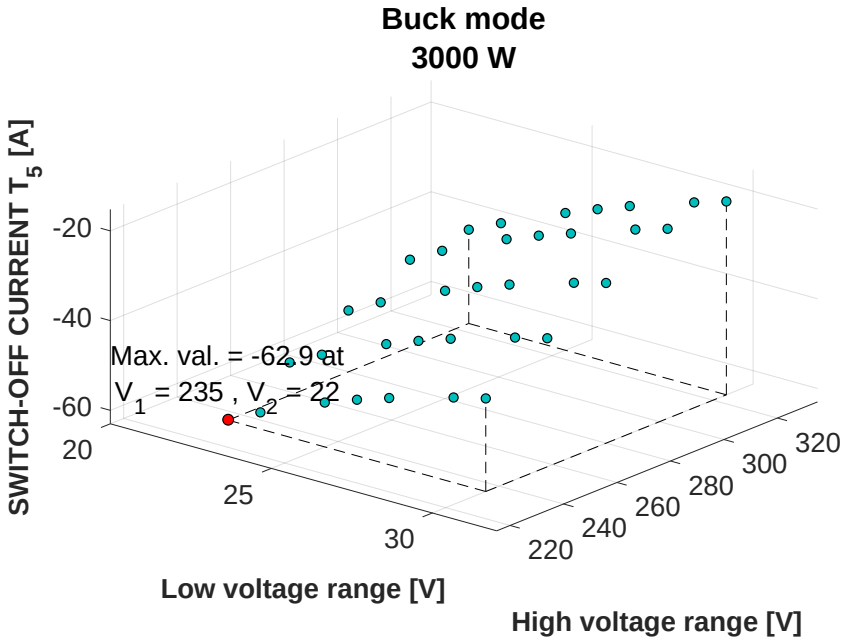

Figure 7.7: Current at SWITCH-OFF on LV side switches in buck mode operation

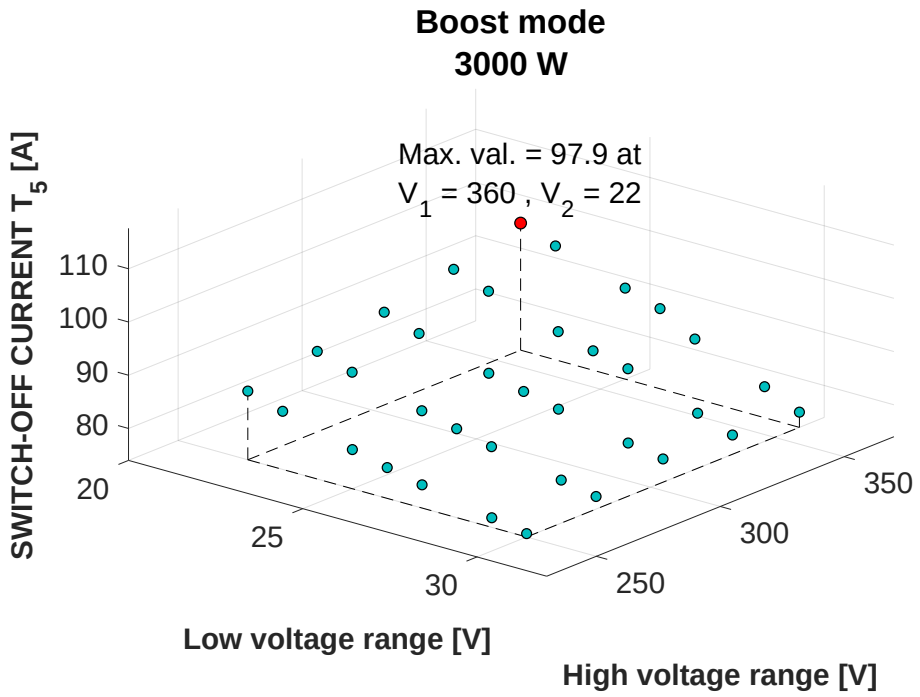

Figure 7.8: Current at SWITCH-OFF on LV side switches in boost mode operation

Figures 7.7 and 7.8 show current at switching-off instant on LV switches. They are much higher than HV side, and it can be observed that boost mode is worst –maximum value of 97.9 A–than buck mode –maximum value of 62.9 A in absolute terms–.

Notice that switches turning-off current is negative in buck mode, which indicates that current flows in the body diode direction. This behaviour involves a soft turn-off and hence regardless losses. In boost mode, by contrast, current at turning-off is positive, i.e. in the opposite direction of the body diode.

Figures from 7.5 to 7.8 provide valuable information, since it could be used to estimate switching losses both on HV and LV switches. Nevertheless, in this work it has been decided to make an efficiency estimation in some operating points of the domain based on advanced model results analysis.

7.1.2. Transformer

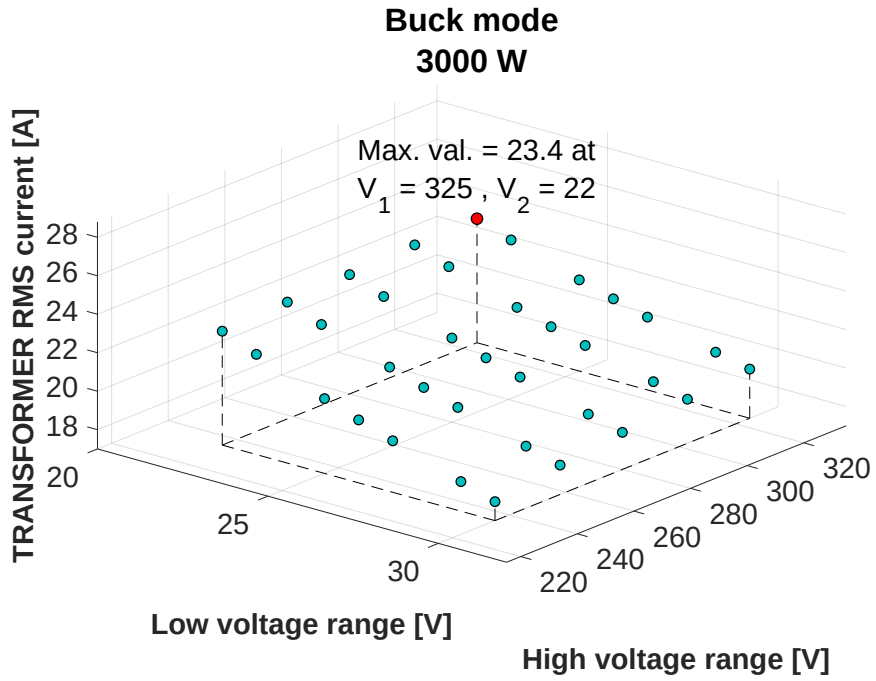

Figure 7.9: Current through HV side transformer in buck mode operation

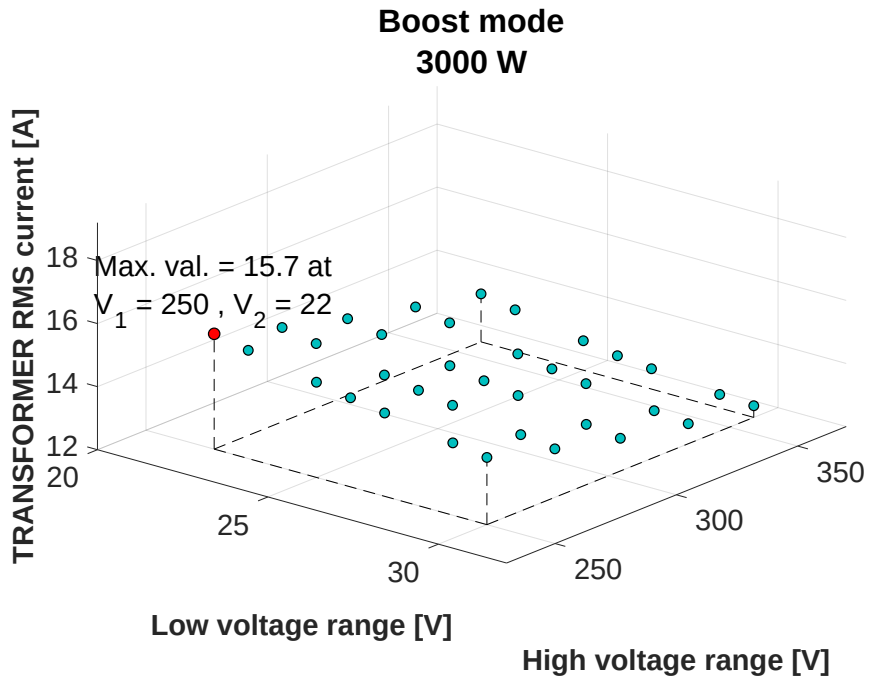

Figure 7.10: Current through HV side transformer in boost mode operation

In Figures 7.9 and 7.10 it can be seen that RMS current through transformer is higher in buck mode (23.4 A) than in boost mode (15.7 A). Maximum RMS current values, together with maximum voltage values, would allow to calculate transformer maximum VA ratings.

7.1.3. DC Inductor

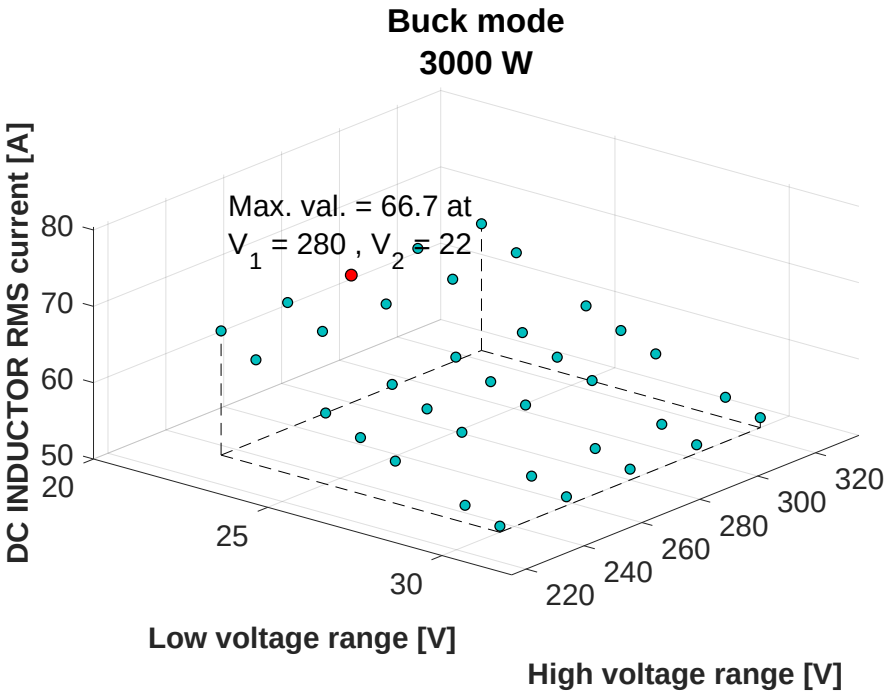

Figure 7.11: L_{DC} RMS current in buck mode operation

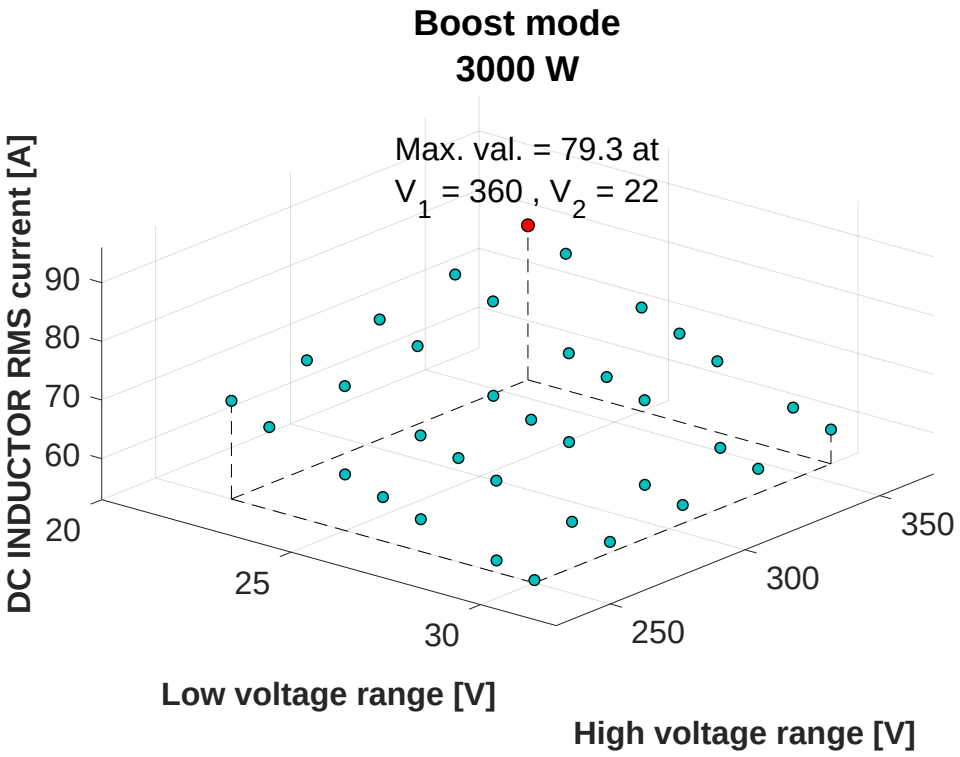

Figure 7.12: L_{DC} RMS current in boost mode operation

In the same way, maximum values obtained from Figures 7.11 and 7.12 help to select suitable DC inductors that withstand these current levels. RMS currents in boost mode are higher than in buck mode. Maximum values are 79.3 A in boost mode and 66.7 A in buck mode.

7.1.4. Capacitors

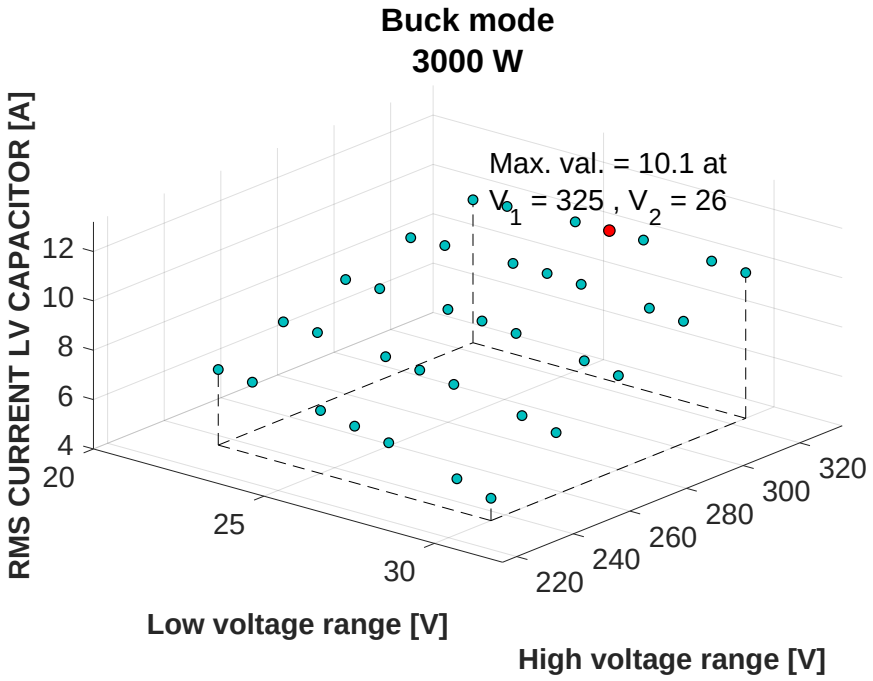

Figure 7.13: LV capacitor RMS current in buck mode operation

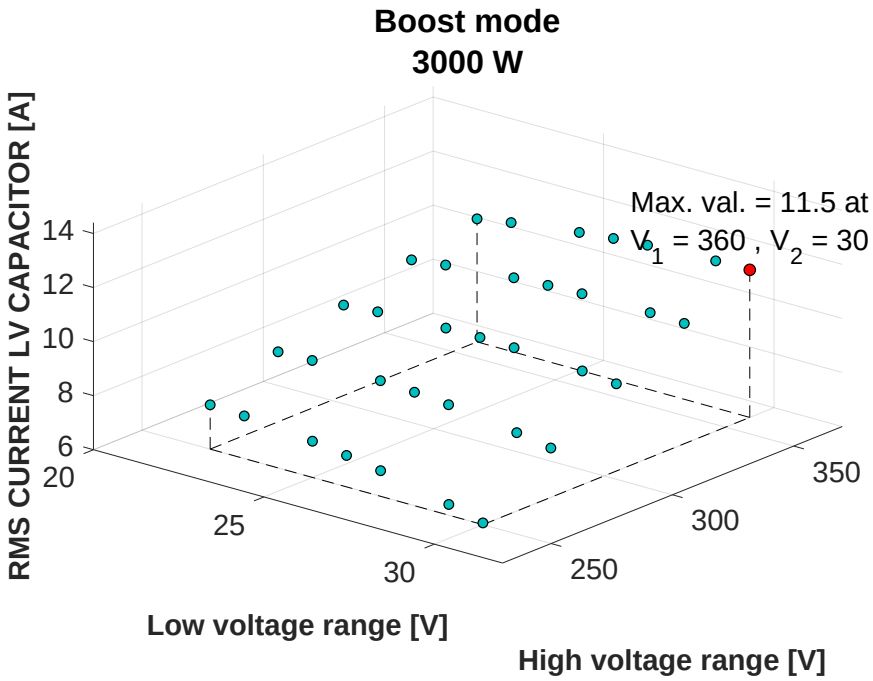

Figure 7.14: LV capacitor RMS current in boost mode operation

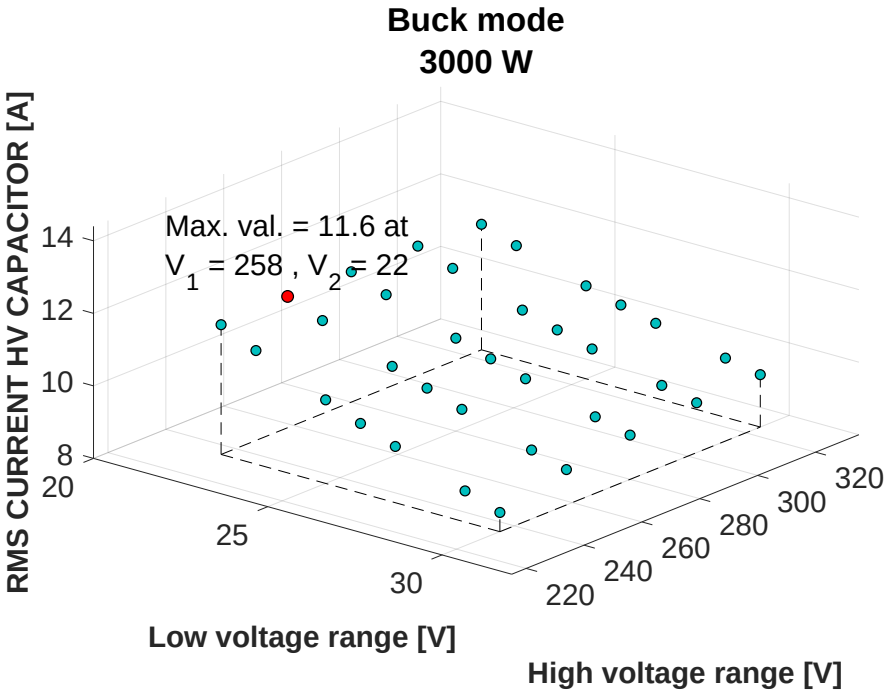

Figure 7.15: HV capacitor RMS current in buck mode operation

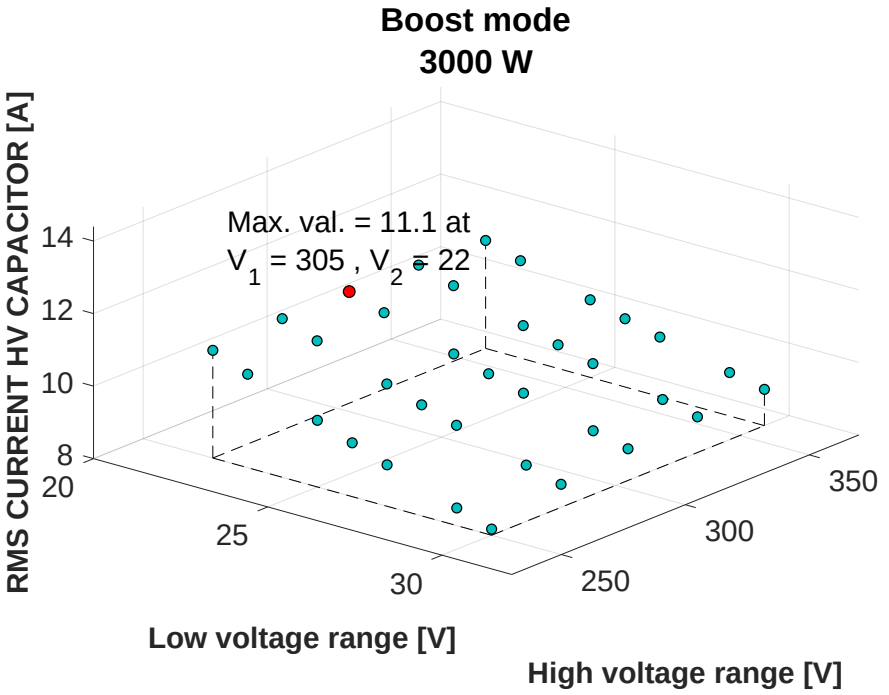

Figure 7.16: HV capacitor RMS current in boost mode operation

It can be seen in Figures 7.13 to 7.16 that RMS currents through capacitors are very similar in both modes and even in both HV and LV side. Nevertheless, this result does not obey to physical reason: if other design criteria for L_{DC} would be considered, those similar values would not have been get.

Again, maximum values obtained from this results allow to choose suitable capacitors.

7.2 Advanced model results

Information presented in this section try to highlight converter efficiency in certain operating points. Before a brief explanation about numeric results, some definitions are going to be established in order to understand them better.

It is important to notice that the only losses considered come from switches mainly. Hence, converter efficiency gives information about switches efficiency. Switch losses can be separated into conduction losses and switching losses, [27]. They are calculated as indicated in Equations 7.1 to 7.4.

$$\bar{P}_{COND} = \bar{P}_{COND_{HV}} + \bar{P}_{COND_{LV}} \tag{7.1}$$

$$\bar{P}_{COND_{HV}} = R_{\mathrm{DSon}HV} \cdot RMS(I_{HV}) \tag{7.2}$$

$$\bar{P}_{COND_{LV}} = R_{\mathrm{DSon}LV} \cdot RMS(I_{LV}) \tag{7.3}$$

$$\bar{P}_{SW} = (\bar{P}_{IN} - \bar{P}_{OUT}) - \bar{P}_{COND} \tag{7.4}$$

Where P_{IN} denotes input power, P_{OUT} denotes output power, P_{COND_i} denotes conduction losses, P_{SW} denotes switching losses, RMS(I_i) denotes switch RMS current,

and subindex i makes reference to either HV or LV.

Converter efficiency is calculated according to Equation 7.5.

$$\eta = \frac{P_{out}}{P_{in}} \cdot 100 \tag{7.5}$$

It is important to note that within switching losses are included passive snubber losses.

Table 7.1 summarizes this section results.

Table 7.1: Advanced model results

V_1	V_2	P_{NOM}	P_{IN}	P_{OUT}	P_{COND}	P_{SW}	η
Buck mode							
270	22	1500	1344.0	1278.2	28.2	37.6	**95.1**
270	28	1500	1387.1	1330.1	20.4	36.5	**95.9**
325	22	1500	1362.7	1282.6	28.0	52.1	**94.1**
325	28	1500	1404.2	1332.1	21.0	51.0	**94.9**
270	22	3000	2436.2	2301.0	91.0	44.2	**94.5**
270	28	3000	2585.2	2477.8	64.9	42.4	**95.8**
325	22	3000	2466.2	2317.4	89.9	58.9	**94.0**
325	28	3000	2611.6	2489.4	65.2	57.0	**95.3**
Boost mode							
270	22	1500	1549.2	1434.5	22.2	92.6	**92.6**
270	28	1500	1568.1	1475.4	16.7	75.9	**94.1**
325	22	1500	1586.4	1442.5	21.2	122.7	**90.9**

325	28	1500	1604.8	1483.0	16.1	105.7	**92.4**
270	22	3000	2989.2	2599.6	86.1	303.5	**87.0**
270	28	3000	3047.9	2775.3	59.7	212.9	**91.1**
325	22	3000	3087.4	2625.8	83.2	378.4	**85.0**
325	28	3000	3133.3	2799.4	56.3	277.6	**89.3**

An overview of last column shows that efficiency in boost mode is lower than buck mode in any case. Whereas efficiency is equal or higher than 94% in buck mode, *maximum* value in boost mode is 94.1%.

If results at nominal power are compared with half nominal power, the conclusion is that differences in boost are much higher than in buck mode. Differences are percentage tenths in buck mode, whereas they are percentage units in boost mode.

Attending to switches losses, conduction losses are approximately similar but in boost mode switching losses grow up enormously.

Chapter 8

Conclusions

Bidirectional and Isolated Current Doubler Topology with clamped diodes is a promising topology to develop power converters. It also allows modularity implementation, which is important to achieve higher power levels than the optimal operating point of single brick.

In contrast with other topologies, important advantages of this one are low RMS currents at both HV and LV side switches and also at transformer, which involves lower conduction losses. Another advantage is low RMS current through DC link capacitors, which involves smaller size of them. From reliability point of view, this topology does not have too many components. The lower number of components, the lower failure probability.

Project objective has been to study working principle of this topology and, taking a single modulation technique, perform numerical simulations to obtain a first order estimation results of efficiency. As in real life, it is necessary to follow an iterative process. So with information about current and voltage over ideal switches, real semiconductors have been selected in order to do a more accurate efficiency estimation, since switches are components with higher losses, especially at high frequency.

As it can be checked in first section of Chapter 7, switches are not withstand currents too high. In HV side they are specially low, so VA ratings also are low for this components.

Essential design parameters to be considered are efficiency and power density.

This study has been focused on estimating the topology efficiency at certain operating points in order to ensure quantitatively how good is the topology under test. Although power density has not been calculated, parameters which affect it have been taken into account, such as switching frequency –the higher f_s is, the smaller magnetics components are but the higher switching losses are– ; voltage and current ratings of DC link capacitors, number of components, and so on.

From efficiency point of view, Current Doubler Converter is more efficient working in buck mode than in boost mode, since switching losses are lower -regarding modulation technique programmed-. Consider an enhanced modulation technique would reduce losses in boost mode, by avoiding voltage spikes at LV switches at turn-off.

It should not be forget that real power circuits have more losses sources. DC inductors and transformers losses should be taking into account in a deeper efficiency analysis of the converter.

Chapter 9

Future Work

9.1 PSpice simulations

Currently there are several software based on PSPICE solver. A fine calculation of efficiency and VA ratings should be done with them, since they provide accurate results for power electronics circuits. Moreover, thermal considerations -dynamic thermal model for example- could be taking into account with this tools.

Some manufacturers, as *Infineon Technologies*, supply PSPICE semiconductor models -MOSFETs, diodes,...- and they also suggest the best solver configuration to make the program run.

9.2 Alternative modulation technique

Switches gate signals are driven using Single PSM in this project. There is not any difference between buck and boost mode from gate signals point of view. Nevertheless, as it is proposed in [8], there is another modulation scheme that improves the implemented one.

Alternative modulation would generate differences between operating modes

gate signals, since they are not symmetric (even if they have the same switches gate signals). Basically, it calculates the freewheeling time and switching-on and switching-off LV side switches are modified -reduced in fact- according to this time. Figures 9.1 and 9.2 illustrate the idea.

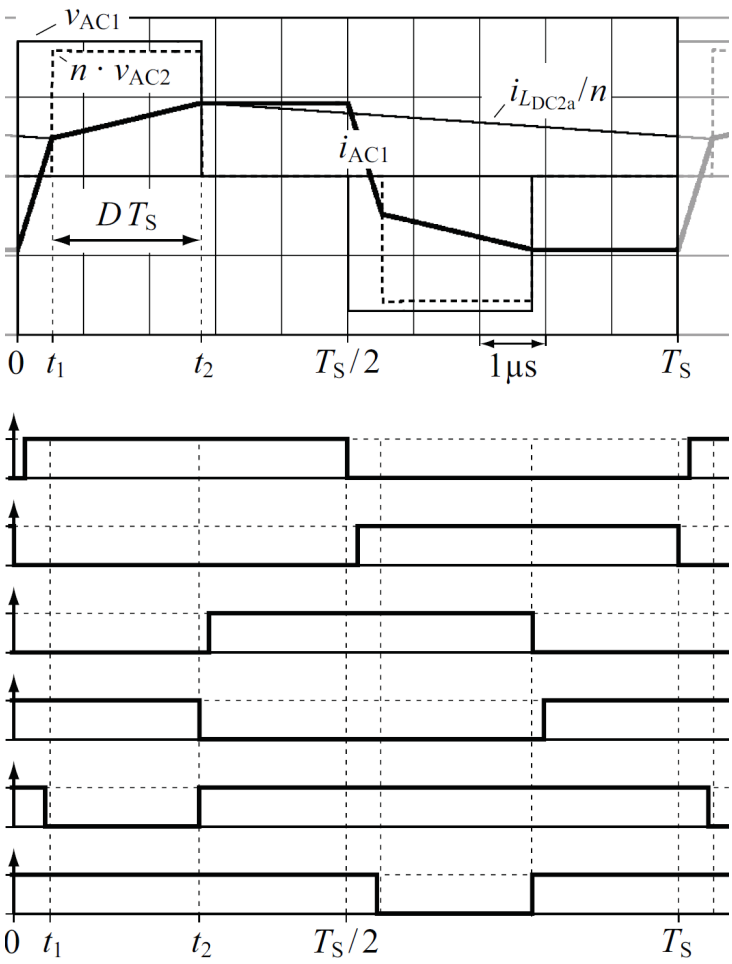

Figure 9.1: Alternative modulation scheme for buck mode, [8]

Figure 9.1 shows that in buck mode, whit the proposed switching scheme for HV side switches, during the freewheeling period T5 and T6 remain ON and they are OFF only during the effective power delivery. Freewheeling period occurs in buck mode at the beginning, i.e. before power transfer period as it can be seen in Figure 9.1. As result, the time during LV swithces are ON is reduced in a time quantity denoted by ΔT in respect to time during switches of each HV branch are ON simultaneously.

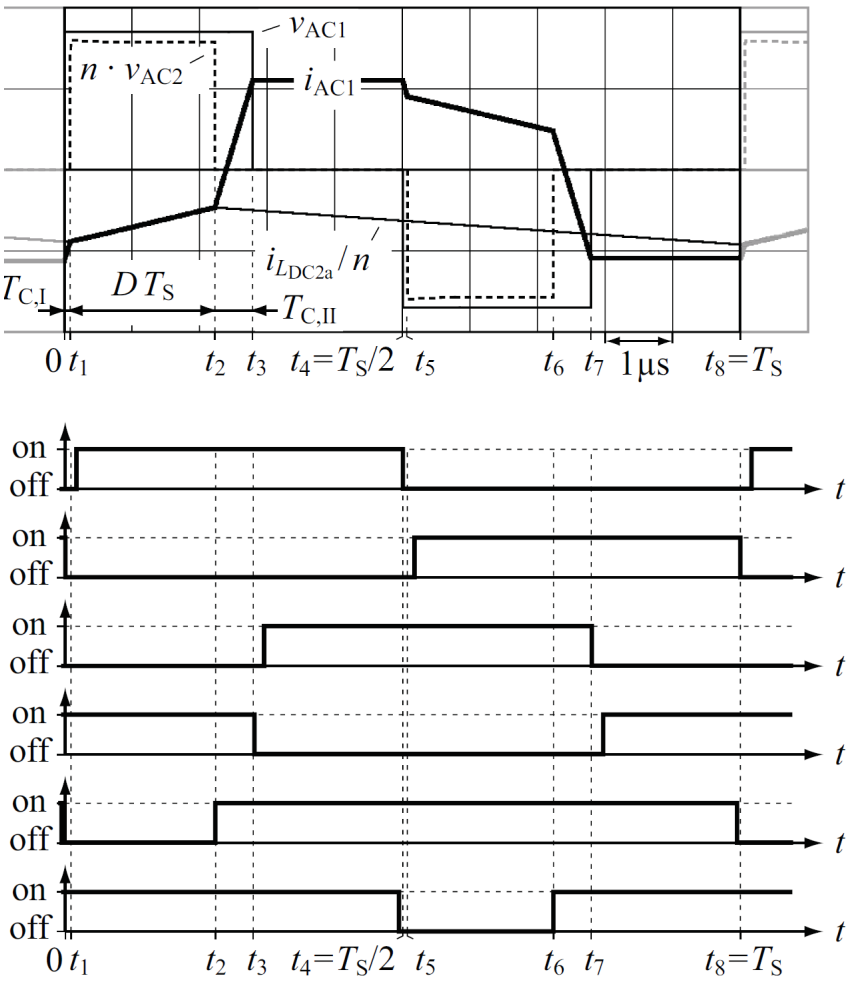

Figure 9.2: Alternative modulation scheme for boost mode, [8]

In boost mode, on the other hand, freewheeling period takes place after power delivery period. However, in the same way as in buck mode, T5 and T6 only are ON during effective power delivery whereas HV switches (T1 to T4) are ON during effective power delivery plus the time interval called ΔT.

Moreover, alternative modulation in boost mode adds an additional advantage, because it allows to avoid voltage spikes on LV switches. The main disadvantage of this technique is that, even if ΔT could be calculated accurately in steady state, it would be necessary a complex solver to calculate it during dynamic transient, because if at any switching event the turning-off current was from drain to source, a voltage spike, possibly destructive, would occur. Another possible disadvantage of this modulation scheme are higher RMS currents in LV switches.

9.3 Further simulation analysis

Advanced model simulations results have permitted to show an estimation of efficiency and its behaviour with the domain variables. Nevertheless, these simulations take too time and only a few operating points have been analysed. It would be desirable to explore more operating points of the whole domain in order to achieve stronger conclusions.

As mentioned in Chapter 7, it would be possible to calculate efficiency using presented magnitudes over the whole domain. It would be interesting to make a comparison between efficiency obtained from advanced model simulation results and efficiency calculated regarding operating points from simple model results.

Appendices

A.1 Comparative results between medium power and full power

A.1.1. Buck mode

HV SWITCH, P = $P_N/2$ = 1500 W							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
235	9.47	9.23	8.76	8.53	8.31	7.87	7.65
258	9.63	9.41	9.00	8.81	8.62	8.25	8.06
280	9.75	9.56	9.19	9.02	8.86	8.54	8.38
303	9.86	9.68	9.35	9.20	9.06	8.79	8.66
325	9.94	9.78	9.49	9.35	9.23	8.99	8.88

Table A.1: RMS current [A] on HV switch for $P_N/2$ in buck mode

HV SWITCH							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
235	-41.99	-41.45	-41.08	-40.57	-40.02	-41.69	-41.07
258	-40.62	-39.86	-39.44	-41.18	-40.38	-39.76	-38.80
280	-38.29	-40.97	-40.07	-39.35	-38.30	-37.74	-40.78
303	-39.78	-39.00	-37.82	-37.21	-40.49	-39.27	-38.33
325	-36.93	-36.23	-40.40	-39.06	-38.01	-36.52	-35.76

Table A.2: Percentage change in RMS current on HV switch for $P_N/2$ with regard to P_N in buck mode

LV SWITCH, P = $P_N/2$ = 1500 W							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
235	46.72	44.91	41.62	40.13	38.74	36.15	34.96
258	46.78	44.99	41.78	40.32	38.94	36.42	35.24
280	46.80	45.06	41.90	40.48	39.12	36.65	35.50
303	46.85	45.11	42.01	40.61	39.30	36.87	35.76
325	46.88	45.17	42.12	40.74	39.45	37.08	35.99

Table A.3: RMS current [A] on LV switch for $P_N/2$ in buck mode

LV SWITCH							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
235	-41.99	-41.45	-41.08	-40.57	-40.02	-41.69	-41.07
258	-40.62	-39.86	-39.44	-41.18	-40.38	-39.76	-38.80
280	-38.29	-40.97	-40.07	-39.35	-38.30	-37.74	-40.78
303	-39.78	-39.00	-37.82	-37.21	-40.49	-39.27	-38.33
325	-36.93	-36.23	-40.40	-39.06	-38.01	-36.52	-35.76

Table A.4: Percentage change in RMS current on LV switch for $P_N/2$ with regard to P_N in buck mode

TRANSFORMER, P = $P_N/2$ = 1500 W							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
235	13.39	13.05	12.38	12.06	11.75	11.13	10.82
258	13.62	13.31	12.73	12.45	12.19	11.66	11.40
280	13.79	13.51	13.00	12.76	12.52	12.08	11.85
303	13.94	13.69	13.23	13.02	12.82	12.43	12.25
325	14.06	13.83	13.42	13.23	13.05	12.72	12.56

Table A.5: RMS current [A] on transformer for $P_N/2$ in buck mode

TRANSFORMER							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
235	-41.56	-40.96	-40.56	-40.38	-40.03	-41.25	-40.58
258	-40.09	-39.83	-39.43	-40.71	-39.86	-39.20	-38.79
280	-38.29	-40.48	-39.53	-38.77	-38.30	-37.74	-40.27
303	-39.23	-38.40	-37.82	-37.21	-39.97	-38.69	-37.70
325	-36.93	-36.22	-39.85	-38.46	-37.37	-36.51	-35.76

Table A.6: Percentage change in RMS current on transformer for $P_N/2$ with regard to P_N in buck mode

L_{DC2A}, P = $P_N/2$ = 1500 W							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
235	13.39	13.05	12.38	12.06	11.75	11.13	10.82
258	13.62	13.31	12.73	12.45	12.19	11.66	11.40
280	13.79	13.51	13.00	12.76	12.52	12.08	11.85
303	13.94	13.69	13.23	13.02	12.82	12.43	12.25
325	14.06	13.83	13.42	13.23	13.05	12.72	12.56

Table A.7: RMS current [A] on L_{DC2a} for $P_N/2$ in buck mode

L_{DC2a}							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
235	-46.70	-46.59	-46.56	-46.33	-46.05	-46.44	-46.31
258	-46.23	-45.79	-45.67	-45.90	-45.67	-45.51	-44.93
280	-44.76	-45.59	-45.33	-45.09	-44.45	-44.27	-45.26
303	-44.95	-44.70	-43.95	-43.74	-44.57	-44.16	-43.82
325	-42.91	-42.63	-44.21	-43.74	-43.34	-42.36	-42.04

Table A.8: Percentage change in RMS current on L_{DC2a} for $P_N/2$ with regard to P_N in buck mode

A.1.2. Boost mode

HV SWITCH, P = $P_N/2$ = 1500 W							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
250	6.22	6.16	6.09	6.05	6.02	5.93	5.89
278	6.28	6.28	6.23	6.22	6.21	6.13	6.10
305	6.44	6.52	6.55	6.56	6.56	6.54	6.52
333	6.81	6.93	7.01	7.03	7.04	7.09	7.08
360	7.27	7.35	7.54	7.57	7.64	7.68	7.72

Table A.9: RMS current [A] on HV switch for $P_N/2$ in boost mode

HV SWITCH							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
250	-43.78	-40.66	-36.76	-30.67	-23.76	-43.36	-39.86
278	-35.08	-28.52	-21.75	-42.61	-38.53	-32.95	-25.58
305	-17.24	-42.22	-37.87	-31.88	-24.41	-15.53	-41.70
-37.14	-31.03	-23.28	-13.34	-41.17	-36.57	333	-29.56
-20.21	-11.50	-40.93	-36.09	-29.00	-19.72	360	-10.64

Table A.10: Percentage change in RMS current on HV switch for $P_N/2$ with regard to P_N in boost mode

LV SWITCH, P = $P_N/2$ = 1500 W							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
250	44.26	42.73	39.92	38.67	37.51	35.43	34.48
278	44.11	42.51	39.67	38.41	37.23	35.09	34.12
305	44.32	42.73	39.83	38.57	37.37	35.18	34.19
333	44.96	43.36	40.43	39.14	37.90	35.76	34.72
360	46.04	44.39	41.47	40.13	38.93	36.69	35.71

Table A.11: RMS current [A] on LV switch for $P_N/2$ in boost mode

LV SWITCH							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
250	-47.38	-47.78	-48.00	-48.15	-48.28	-47.61	-48.06
278	-48.23	-48.26	-48.34	-48.11	-48.54	-48.65	-48.58
305	-48.44	-48.32	-48.76	-48.84	-48.70	-48.50	-48.53
333	-48.96	-49.03	-48.87	-48.26	-48.83	-49.28	-49.38
360	-48.86	-48.06	-48.96	-49.46	-49.57	-48.91	-47.88

Table A.12: Percentage change in RMS current on LV switch for $P_N/2$ with regard to P_N in boost mode

TRANSFORMER, P = $P_N/2$ = 1500 W							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
250	8.90	8.82	8.71	8.66	8.62	8.50	8.44
278	8.96	8.96	8.89	8.88	8.86	8.75	8.72
305	9.16	9.27	9.31	9.32	9.32	9.29	9.26
333	9.64	9.81	9.91	9.94	9.95	10.04	10.01
360	10.25	10.36	10.63	10.68	10.77	10.81	10.87

Table A.13: RMS current [A] on transformer for $P_N/2$ in boost mode

TRANSFORMER							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
250	-43.17	-40.23	-36.51	-30.83	-24.22	-42.86	-39.40
278	-34.89	-28.61	-22.16	-42.01	-38.17	-32.74	-25.77
305	-17.83	-41.61	-37.47	-31.79	-24.56	-16.32	-41.16
333	-36.83	-30.95	-23.47	-14.81	-40.55	-36.06	-29.53
360	-21.25	-13.01	-40.30	-35.61	-28.98	-20.74	-12.10

Table A.14: Percentage change in RMS current on transformer for $P_N/2$ with regard to P_N in boost mode

L_{DC2A}, P = $P_N/2$ = 1500 W							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
250	8.90	8.82	8.71	8.66	8.62	8.50	8.44
278	8.96	8.96	8.89	8.88	8.86	8.75	8.72
305	9.16	9.27	9.31	9.32	9.32	9.29	9.26
333	9.64	9.81	9.91	9.94	9.95	10.04	10.01
360	10.25	10.36	10.63	10.68	10.77	10.81	10.87

Table A.15: RMS current [A] on L_{DC2a} for $P_N/2$ in boost mode

L_{DC2a}							
V_1[V]/V_2[V]	22	23	25	26	27	29	30
250	-46.20	-46.63	-47.11	-47.71	-48.86	-46.10	-46.62
278	-47.06	-47.77	-48.77	-45.98	-46.27	-46.82	-47.48
305	-48.48	-45.82	-46.09	-46.47	-47.26	-48.07	-45.53
333	-45.75	-46.19	-46.94	-47.25	-45.04	-45.22	-45.37
360	-45.48	-46.24	-44.72	-44.84	-44.96	-44.94	-45.59

Table A.16: Percentage change in RMS current on L_{DC2a} for $P_N/2$ with regard to P_N in boost mode

A.2 Matlab code

A.2.1. Code for setting a simulation

```
function [param]=current_doubler_parameters(V1, V2, P_act, model_type)

    % Time parameters
    param.Tint = 1e-9; % s
    param.tm = 50e-9; % s
    param.fs = 100e3; % Hz
    param.Ts = 1/param.fs; % s


    % Operating point parameters
    param.Vhigh = V1; % V
    param.Vlow = V2; % V
    param.Pnom = abs(P_act); % W


    % Operating mode defined by power sign
    if sign(P_act)>=0
        op_mode = 'buck';
    else
        op_mode = 'boost';
    end

    % Components parameters

    % MOSFET
    switch model_type
        case 'simple'
            param.Rds_on_lv = 36.25e-3; % Ω
            param.Ron_d_lv = 0.8/64; % Ω
            param.Vd_m_lv = 0.8; % V
            param.Rds_on_hv = 36e-3; % Ω
            param.Ron_d_hv = 5/30; % Ω
```

```
        param.Vd_m_hv = 5; % V

    case 'advanced'
        param.source_gain_hv = 20;
        param.source_gain_lv = 15;
        param.L_par_mos = 2e-9; % H
        param.C_snb = 20e-9; % F
        param.R_snb = 5; % Ω
        % Mosfet HV side
        param.Rgate_high_on = 6; % Ω
        param.Rgate_high_off = 12; % Ω
        param.Rds_on_hv = 36e-3; % Ω
        param.Ids_hv = 35; % A
        param.Vgs_hv = 15; % V
        param.Vth_hv = 1.875; % V
        param.Rs_hv = 1.42e-3; % Ω
        param.Rd_hv = 77.52e-6; % Ω
        param.Ciss_hv = 1750; % nF
        param.Crss_hv = 9.5; % nF
        param.Coss_hv = 150; % nF
        param.Vfd_hv = 5; % V
        param.Ron_d_hv = 5/30; % Ω
        param.lambda_hv = 0.01;
        % Mosfet LV side
        param.Rgate_low_on = 6; % Ω
        param.Rgate_low_off = 12; % Ω
        param.Rds_on_lv = 36.25e-3; % Ω
        param.Ids_lv = 64; % A
        param.Vgs_lv = 10; % V
        param.Vth_lv = 2.2; % V
        param.Rs_lv = 878e-6; % Ω
        param.Rd_lv = 50e-6; % Ω
        param.Ciss_lv = 5340; % nF
        param.Crss_lv = 4; % nF
        param.Coss_lv = 240; % nF
```

```
        param.Vfd_lv = 0.8; % V
        param.Ron_d_lv = 0.8/64; % Ω
        param.lambda_lv = 0.25;
end

% TRANSFORMER
param.N2N1 = 3;
param.L_lk = 1.5e-6; % H

switch model_type
    case 'simple'
        param.Rm = 1e7; % Ω

    case 'advanced'
        param.Rm = 1e7; % Ω
        param.Lm = 1e-3; % H

end

% DC INDUCTOR
param.L_dc = 3.7e-6; % H
param.R_ldc = 0;

% VAUX AND CLAMPED DIODES
param.Rd = 20e-3; % Ω
param.Vd = 1.2; % Ω
param.Vaux = 150; % V


% CAPACITORS
param.Chigh = 500e-6; % F
param.Clow = 500e-6; % F


% CIRCUIT BREAKER RESISTANCE
param.Ron_break = 1e-15; % Ω
```

```
% OPERATING MODES SELECTION
switch op_mode
    case 'buck'
        param.operating_mode = 1;

        % Circuit breakers state
        param.gate_break_source_hv = 1;
        param.gate_break_source_lv = 0;
        param.gate_break_load_hv = 0;
        param.gate_break_load_lv = 1;
        param.gate_hv_cap = 0;
        param.gate_lv_cap = 1;

        % DC networks voltage
        param.Vin = V1;
        param.Vout = V2;

        % Adjust load for nominal power
        param.Rload = param.Vout^2/param.Pnom;

        % Capacitors initial voltage
        param.Chigh_initial = 0;
        param.Clow_initial = 0;

        param.D_nom = (2*param.Vout*param.N2N1)/param.Vin;
    case 'boost'
        param.operating_mode = 2;

        % Circuit breakers state
        param.gate_break_source_hv = 0;
        param.gate_break_source_lv = 1;
        param.gate_break_load_hv = 1;
        param.gate_break_load_lv = 0;
        param.gate_hv_cap = 1;
        param.gate_lv_cap = 0;

        % DC networks voltage
```

```
            param.Vin = V2;
            param.Vout = V1;

            % Adjust load for nominal power
            param.Rload = param.Vout^2/param.Pnom;

            % Capacitors initial voltage
            param.Chigh_initial = param.Vout*0.9;
            param.Clow_initial = 0;
            param.D_nom = (2*param.Vin*param.N2N1)/param.Vout;
        end
end
```

A.2.2. Modulator algorithm

```
function [p1, p2, p3, p4, p5, p6, D_eff] = fcn(u, fs, tm, D_nom, operating_mode)

    Ts = 1/fs; % Hz


    if operating_mode==1 % BUCK MODE
        D_eff = D_nom;

        y0 = 1-(tm/(Ts/2));
        x0 = 1-y0;

        y2 = 1-(D_eff+(tm)*2/Ts);
        x2 = 1-y2;

        y4 = 1-(D_eff);
        x4 = 1-y4;

        % GATES 1 AND 2
        if u >= 0
            p2 = 0;
            if u>y0
                p1 = 0;
            else
                p1 = 1;
```

```
        end
    else
        p1 = 0;
        if u>=-(x0)
            p2 = 0;
        else
            p2 = 1;
        end
    end

    % GATES 3 AND 4
    if u>y2 || u<-(x4)
        p3 = 0;
        if u>y4 || u<=-(x2)
            p4 = 1;
        else
            p4 = 0;
        end
    else
        p3 = 1;
        p4 = 0;
    end

    % GATE 5
    if u>=y4 && u<=1
        p5 = 0;
    else
        p5 = 1;
    end

    % GATE 6
    if if u<=0 && u>=-(x4)
        p6 = 0;
    else
        p6 = 1;
    end
else % BOOST MODE
```

```
D_eff = D_nom;

y0 = 1-(tm/(Ts/2));
x0 = 1-y0;

y2 = 1-(D_eff+(tm)*2/Ts);
x2 = 1-y2;

y4 = 1-(D_eff);
x4 = 1-y4;

% GATES 1 AND 2
if u >= 0
    p2 = 0;
    if u>y0
        p1 = 0;
    else
        p1 = 1;
    end
else
    p1 = 0;
    if u>=-(x0)
        p2 = 0;
    else
        p2 = 1;
    end
end

% GATES 3 AND 4
if u>y2 || u<-(x4)
    p3 = 0;
    if u>y4 || u<=-(x2)
        p4 = 1;
    else
        p4 = 0;
    end
else
    p3 = 1;
```

```
        p4 = 0;
    end

    % GATE 5
    if u>=y4 && u<=1
        p5 = 0;
    else
        p5 = 1;
    end

    % GATE 6
    if if u<=0 && u>=-(x4)
        p6 = 0;
    else
        p6 = 1;
    end
end
```

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