Thus at step 7 we have

$$e_{12}-1=0 \quad e_1-2=0 \quad e_2-1=0 \quad e_0-3=0$$
$$d_{12}+2=0 \quad d_1+3=0 \quad d_2+4=0 \quad d_0+4=0.$$

So there are 8 nonlinear equations in 20 unknowns. To make use of Bremermann's Algorithm, we have introduced new variables to obtain equations of the form $H_i=0$ so that each of the H_i's reduce to that of a polynomial of degree 2. Thus we get 98 nonlinear equations in 110 unknowns. Some of the equations are given below:

$$x_1-t_3t_7=0; \quad x_2-t_{13}t_{19}=0; \quad x_3-t_3t_8=0;$$
$$x_4-t_7t_8=0; \quad x_5-t_{14}t_{19}=0; \quad x_6-t_4t_{14}=0;$$
$$\vdots \qquad \vdots \qquad \vdots$$
$$x_{88}-x_{33}x_{71}=0; \quad x_{89}-x_{34}x_{55}=0; \quad x_{90}-x_{34}x_{57}=0$$
$$t_1x_1+t_4x_2-1=0;$$
$$t_1t_{19}+t_1x_3+t_1x_4+t_4x_5+x_3x_6+t_5x_2+x_1x_8 - x_1x_9-x_6x_{10}-2=0;$$
$$\vdots$$

Using a variant form of Bremermann's Algorithm [3] we have a set of solution for

$$H=\sum_{i=1}^{98} H_i^2=0.$$

(In fact there are infinite many solutions): $t_1=1$; $t_3=1$; $t_4=-0.4$; $t_5=-0.6$; $t_6=-0.8$; $t_7=0.2$; $t_{13}=1.195$; $t_{14}=3.333$; $t_{17}=-0.1213$; and $t_2=t_8=\cdots t_{20}=0$. With some additional arithmetic manipulations for exact fractions one can have $t_1=t_3=1$; $t_4=-\frac{2}{5}$; $t_5=-\frac{3}{5}$; $t_6=-\frac{4}{5}$; $t_7=\frac{1}{5}$; $t_{13}=\frac{6}{5}$; $t_{14}=\frac{10}{3}$; $t_{17}=-\frac{3}{25}$, and $t_2=t_8=\cdots t_{20}=0$.

The corresponding combinatorial realization is shown in Fig. 2. Since there is no delay free loop in the realization, this is also the circuit-theoretic realization.

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Circuits and Systems Letters

A Novel SC Oscillator

J. L. HUERTAS, A. RODRÍGUEZ-VÁZQUEZ, AND B. PÉREZ-VERDÚ

I. Introduction

Switched-capacitor (SC) networks have been recognized as an efficient tool for performing analog (sampled-data) signal processing in monolithic integrated circuit form. Such an appealing feature is a good motivation for investigating new application areas beyond the traditional simulation of analog filters. In particular, SC oscillators begin to emerge as an alternative for low- and medium-frequency sinusoidal waveform generation. Several circuit realizations for SC oscillators have been reported recently [1]–[4] and it seems interesting to search for more advantageous circuit realizations.

The purpose of this paper is to present a simple SC oscillator using unity-gain buffers and a minimum number of capacitors. When compared with the oscillator reported in [1], the new structure results more appropriate to be acommodated in a fully integrated MOS system because it does not require either additional resistors nor high capacitor ratios. On the other hand, if compared with the oscillators reported in [2]–[4], the new design does not employ infinite gain devices. Moreover, the proposed circuit is a robust oscillator since it is based on a nonlinear oscillator mechanism.

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II. Proposed Oscillator

Fig. 1 shows the new SC oscillator which employs two unity-gain buffers. Switches appearing in that figure are controlled by a two-phase nonoverlapping clock. One phase of the clock will be named as even phase and the other as odd phase. Furthermore, we will assume a 50-percent duty cycle clock with a period of T_c seconds. Supposing linear operation for both active devices we may formulate the following equation set:

$$\begin{bmatrix} V_{C_1}^e(n) \\ V_{C_2}^e(n) \end{bmatrix} = \begin{bmatrix} 1 & C_4/C_1 \\ -C_3/C_2 & 1 \end{bmatrix} \begin{bmatrix} V_{C_1}^e(n-1) \\ V_{C_2}^e(n-1) \end{bmatrix}. \quad (1)$$

This linear transformation has two characteristic roots given by

$$Z_{1,2}=1\pm j\sqrt{C_3C_4/C_1C_2} \quad (2)$$

which obviously lie outward the unity circle. This result suggests that linear modeling is inaccurate because the growing nature of the output will force the system to saturate.

Thus we need to take into consideration that at least one of the buffers must go into saturation. When that happens, both eigenvalues move towards the unit circle and reach it for some amplitude value. As it is well known, oscillation will be maintained for that amplitude. Then, for proper oscillation operation at least one of the output signals (V_{01} or V_{02}) would be saturated. In order to get a low-distortion sinusoidal output we need to force that only one of the buffers is saturated during a half cycle. Moreover, we will require that the same buffer reaches saturation during both clock phases.

Let us choose V_{01} as the output of the buffer going into

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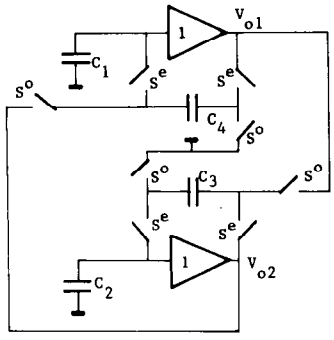


Fig. 1. Proposed oscillator.

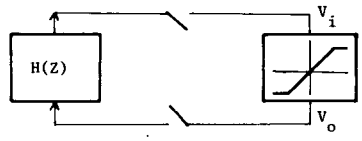


Fig. 2. Nonlinear model of the oscillator.

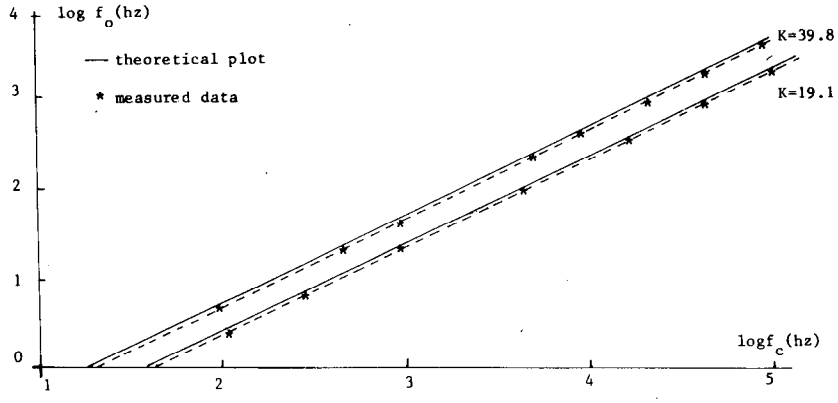


Fig. 3. Plot of oscillation frequencies against clock frequencies for two different k values.

saturation. It can be shown that a necessary condition which guarantees that V_{02} does not reach saturation too is

$$\frac{C_4}{C_1} > \frac{C_3}{C_2}. \tag{3}$$

With the above assumption in mind, we can write the state equation for the system taking into account saturation nonlinearity

$$\begin{bmatrix} V_{C_1}^e(n) \\ V_{C_2}^e(n) \end{bmatrix} = \begin{bmatrix} \frac{C_1}{C_1+C_4} & \frac{C_4}{C_1+C_4} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_{C_1}^e(n-1) \\ V_{C_2}^e(n-1) \end{bmatrix} + \begin{bmatrix} \frac{C_4}{C_1+C_4} \\ -C_3/C_2 \end{bmatrix} f\left[V_{C_1}^e(n-1)\right] \tag{4}$$

with

$$f\left[BVV_{C_1}^e(n)\right] = \begin{cases} V_{C_1}^e(n), & \text{for } -V_{\text{sat}} < V_{C_1}^e(n) < V_{\text{sat}} \\ V_{\text{sat}}, & \text{for } V_{C_1}^e(n) > V_{\text{sat}} \\ -V_{\text{sat}}, & \text{for } V_{C_1}^e(n) < -V_{\text{sat}} \end{cases} \tag{5}$$

where V_{sat} is the saturation voltage for V_{01} and we have assumed a symmetrical saturation for that buffer.

Finding an exact solution for (4) is rather involved. Instead, we will consider an approximate solution based on the use of a first order describing function [6]. To do that, we will model the oscillator by the block diagram shown in Fig. 2 where the linear block may be described by

$$H(Z) = \frac{C_4}{C_1+C_4} \frac{Z^2 - Z - \frac{C_3}{C_2}}{Z^2 + \left(\frac{C_4}{C_1+C_4} - 2\right)Z + \frac{C_1}{C_1+C_4}}. \tag{6}$$

We will assume a sinusoidal input to the nonlinearity given by

$$V_i(n) = A \sin(nw_0 T_c) \tag{7}$$

where T_c is the clock period, A is the oscillation amplitude, and w_0 is the angular oscillation frequency.

Now, we may represent the static nonlinearity by an equivalent gain $N(A)$ corresponding to the first harmonic of the nonlinearity output. After some algebraic manipulations we obtain the value of f_0

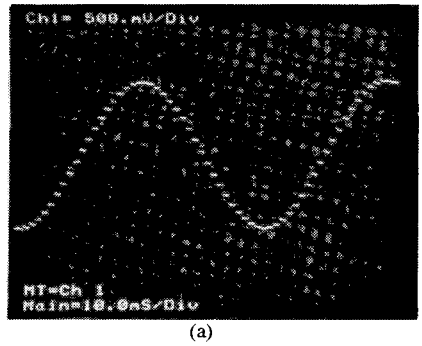
$$f_0 = \frac{f_c}{2\pi} \cos^{-1}\left[1 - \frac{1}{2\left\{1 + \frac{C_1}{C_4}\left(1 + \frac{C_2}{C_3}\right)\right\}}\right] = \frac{f_c}{K}. \tag{8}$$

Also, the oscillation amplitude may be evaluated from the equation

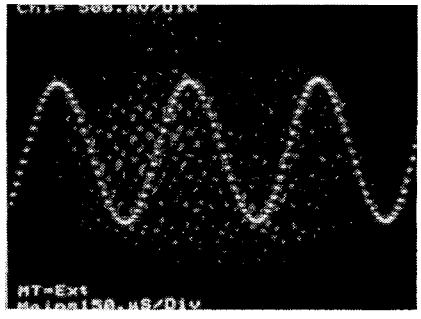
$$\frac{1}{1+\frac{C_3}{C_2}} = \frac{2}{\pi}\left[\sin^{-1}\left(\frac{V_{\text{sat}}}{A}\right) + \frac{V_{\text{sat}}}{A}\sqrt{1-\left(\frac{V_{\text{sat}}}{A}\right)^2}\right]. \tag{9}$$

III. Discussion of Results

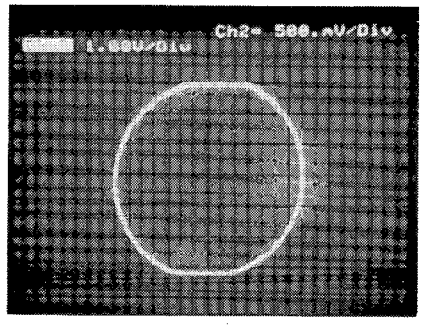
Empirical data have been collected for different capacitor ratios. Agreement with theoretical predictions seems reasonable taking into account the nonexact nature of the describing function approach. In Fig. 3 we have plotted the dependance between



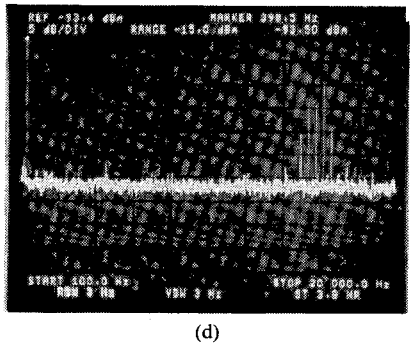
(a)



(b)



(c)



(d)

Fig. 4. (a) Output waveform for $f_c = 669.3$ Hz; measured oscillation frequency: 17 Hz. (b) Output waveform for $f_c = 81229$ Hz; measured oscillation frequency: 2063 Hz. (c) Limit cycle for $f_c = 15690$ Hz. Horizontal axis: V_{02}, 0.5 V/div. Vertical axis: V_{01}, 1 V/div. (d) Measured spectra for $f_c = 15\,690$ Hz.

both oscillation and clock frequencies for two different theoretical values of parameter k in (8) (namely, $k = 19.1$ and $k = 39.8$). Measured κ were 21.3 and 44.2, respectively. From that figure, it should be clear that linearity is preserved over a wide range of clock frequency values.

Fig. 4 depicts some oscillograms showing the performance of the new circuit. We have used the same capacitor values for all the pictures in Fig. 4 ($C_1 = 5.6nf$; $C_2 = 30nf$; $C_3 = 1.8nf$; $C_4 = 3nf$). Fig. 4(a) and (b) show the output voltage V_{02} for two different clock frequency values. Amplitude does not suffer a significant change because we have used the same capacitor values. Fig. 4(c) represents the form of the limit cycle for a clock frequency of 15 690 Hz. The measured oscillation frequency was 398.5 Hz. Vertical axis corresponds to V_{01} and exhibits the predicted saturation. By the contrary, V_{02} (horizontal axis) does not saturate. Finally, Fig. 4(d) illustrates the output signal distortion. It shows the experimental spectral analysis for the output V_{02} of the oscillator whose limit cycle is shown in Fig. 4(c). As can be seen in Fig. 4(d), the only significant low-frequency component is the first harmonic. In fact, the second and third harmonics were measured to be, respectively, -41 and -47 dB below the fundamental one.

Finally, it is worth considering the influence of parasitic capacitances. We note that the structure can be made insensitive to bottom capacitances. However, it will be sensitive to top ones. It means that the design equations must slightly changed in order to include stray capacitors. For the practical cases considered above we have evaluated the incidence of strays in a pesimistic situation. Assigning to the top capacitor associated with C_j ($j = 1,2,3,4$) a value of the 5 percent of C_j, we got an actual frequency deviation about the nominal value ranging from 0.39 to 1.91 percent.

IV. Conclusions

A new SC oscillator has been reported. The proposed circuit is a fully SC and does not require any resistor. In addition, that oscillator is robust and its oscillatory mechanism depends only on the active elements used. Finally, there exists a linear relation between both the clock and the oscillation frequencies which is preserved for three decades. It has very good performance for a low-priced components VCO.

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Optimum Adaptive Algorithms with Applications to Noise Cancellation

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***Abstract*—A new simple formulation for the choice of the optimum convergence factor μ in adaptive filtering using gradient techniques is given. This leads to several optimum adaptive filtering algorithms each of**

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