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On the Active Compensation of Operational **Amplifier Based VCVS**

J. L. HUERTAS AND A. RODRIGUEZ-VAZOUEZ

Abstract - A unified treatment of the active compensation for VCVS realized by operational amplifiers is presented. It is a summary of lowsensitivity circuit structures which can be either magnitude or phase compensated. The performance of such a circuits is discussed in detail. Experimental data for some of them are also included.

I. INTRODUCTION

The high-frequency roll-off of the operational amplifier imposes a practical limitation to their usefulness in RC-active filter design. With the advent of low cost internally compensated dual operational amplifiers, the design of active-compensated voltagecontrolled voltage sources (VCVS) is currently the most popular way to overcome such a limitation. In that sense, many ad hoc circuit configurations have been reported for realizing compensated amplifiers but a clear statement of the connections among these structures is missing and it remains difficult to select anyone of them for a specific application. In particular, most discussion fail to point out two important considerations. The first one is a detailed exposition of the different criteria which can be used for achieving an improvement of the amplifier frequency response. The second one being a discussion of the sensitivity properties of the proposed compensation schemes.

This paper presents a unified approach to the generation of active-compensated VCVS's. Starting from a second-order active-R low-pass section, a procedure is formulated for finding circuit implementations to realize an amplifier either with amplitude (maximally flat magnitude) or with phase (\rightarrow 0) compensation.

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¹BW' can be considered as a meaningful measure since for phase compensation only circuit structures with $Q \ge 1$ are of interest.

Most of the previously reported designs follow as special cases of this general section which is shown to exhibit minimum sensitivity. In fact, although some new circuit structures result, the main objective of our work is to tie all the ad hoc papers about compensated amplifiers together and to provide guidelines of what should be done to obtain low-sensitivity active compensated VCVS's. As a consequence, the paper also gives a framework for comparing existing (and in some cases new) alternative designs for VCVS's.

II. ACTIVE COMPENSATION SCHEMES FOR MINIMUM SENSITIVITY

The availability of low-cost dual amplifiers is one of the most important motivations for the development of active compensation schemes. All of the known configurations use two operational amplifiers and it appears reasonable to derive structures which only require a pair of active elements.

It should be clear that any VCVS based on two operational amplifiers is a second-order active-R filter which exhibits a low-pass characteristic, i.e., a two-integrators circuit with a transfer function given by

$$T(s) = k_0 \frac{w_0^2}{w_c} \frac{s + w_c}{s^2 + s\left(\frac{w_0}{Q}\right) + w_0^2}.$$
 (1)

Brand and Schaumann [6] have shown that all second-order active-R filters can be derived from the general structure depicted in Fig. 1(a). The transfer function denominator associated with both possible outputs v_{01} and v_{02} , is

$$D(s) = s^2 + s(c_0GB_2 + \gamma_0GB_1) + GB_1GB_2(c_0\gamma_0 - c_2\gamma_2).$$
 (2)

Routine calculations shown that the condition for minimum sensitivity with complex poles is [6]

$$c_0 \gamma_0 = 0. (3)$$

Fulfilling that condition is equivalent to opening the local feedback loop of one integrator. Because the configuration is symmetrical we may take $c_0 = 0$ and consider alternatively either v_{01} or v_{02} as the output of the compensated VCVS. Henceforth we shall call type-I structures the circuit configurations with v_{01} as the output of the compensated amplifier. Similary, we shall call type-II structures the configurations with v_{02} as the output.

Equations (4) and (5) show, respectively, the transfer function for both types of structures

type-I:
$$T_{\rm I}(s) = \frac{v_{01}}{v_i} = \frac{s\gamma_1 GB_1 + GB_1 GB_2 \gamma_2 c_1}{D(s)}$$
 (4)

type-I:
$$T_{I}(s) = \frac{v_{01}}{v_i} = \frac{s\gamma_1 GB_1 + GB_1 GB_2 \gamma_2 c_1}{D(s)}$$
 (4)
type-II: $T_{II}(s) = \frac{v_{02}}{v_i} = \frac{sc_1 GB_2 + GB_1 GB_2 (c_1 \gamma_0 + c_2 \gamma_1)}{D(s)}$ (5)

where to ensure stability we must impose the following condi-

$$\gamma_0 > 0 \quad \text{and} \quad c_2 \gamma_2 < 0. \tag{6}$$

It is worth noting [6] that all parameters are differences of resistor ratios, i.e., e.g. $(\gamma_i, c_i) = x_i - y_i$, with $0 \le (x_i, y_i) \le 1$, however, in order to avoid large sensitivity due to difference effects, we shall choose either x_i or y_i always equal to zero. Assuming that, the circuit in Fig. 1(b) shows the general structure of any low-sensitivity compensated VCVS and provide definition

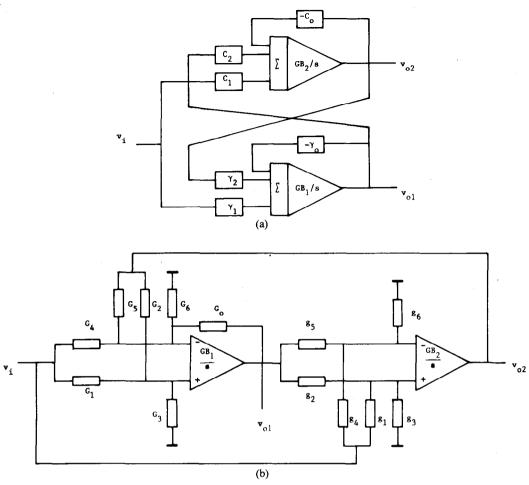


Fig. 1. (a) Schematic representation of a general second-order active-R filter. (b) General circuit structure of a low-sensitivity compensated VCVS.

for the parameters in term of specific resistor ratios as follows:

$$c_{i} = \frac{g_{i}}{3} - \frac{g_{i+3}}{6}, \qquad i = 1, 2$$

$$\sum_{j=1}^{3} g_{j} \sum_{j=4}^{5} g_{j} \qquad (7-a)$$

$$\gamma_{i} = \frac{G_{i}}{\sum_{j=1}^{3} G_{j}} - \frac{G_{i+3}}{\sum_{j=4}^{6} G_{j} + G_{0}}, \quad i = 1, 2$$

$$\gamma_{0} = \frac{G_{0}}{\sum_{j=4}^{6} G_{j} + G_{0}}$$

$$(7-c)$$

$$\gamma_0 = \frac{G_0}{\sum_{j=-4}^{6} G_j + G_0}$$
 (7-c)

where either $g_i(G_i)$ or $g_{i+3}(G_{i+3})$ is always equal to zero depending on the sign of $c_i(\gamma_i)$, i=1,2. Note that since the summations are performed by a resistive node, the following additional interconnection requirements can be derived:

amplifier one:
$$0 \le \gamma_0 - \frac{1}{2} \{ (1 - \operatorname{sgn} \gamma_1) \gamma_1 + (1 - \operatorname{sgn} \gamma_2) \gamma_2 \} \le 1$$
 (8-a)

$$0 \le \frac{1}{2} \left\{ (1 + \operatorname{sgn} \gamma_1) \gamma_1 + (1 + \operatorname{sgn} \gamma_2) \gamma_2 \right\} \le 1$$
 (8-b)

amplifier two:
$$0 \le -\frac{1}{2} \{ (1 - \operatorname{sgn} c_1) c_1 + (1 - \operatorname{sgn} c_2) c_2 \} \le 1$$
 (8-c)

$$0 \le \frac{1}{2} \left\{ (1 + \operatorname{sgn} c_1) c_1 + (1 + \operatorname{sgn} c_2) c_2 \right\} \le 1$$
 (8-d)

which must be considered when making a particular design.

PARAMETER b CORRESPONDS TO GB_1/GB_2 TYPE-1 k_o $-\frac{c_1}{c_2}$ $-\frac{c_1\gamma_o + c_2\gamma_1}{c_2\gamma_2}$ $GB_1GB_2(-c_2\gamma_2) = GB_1GB_2 = \frac{1}{2}$ phase compensation condition ϕ $-\frac{v_0}{gB_2GB_1} = \frac{v_0}{gB_2GB_1} = \frac{v_0}{gB_2GB_2}$ $-\frac{v_0}{gB_2GB_1} = \frac{v_0}{gB_2GB_1} = \frac{v_0}{gB_2GB_1}$

TABLE I
DESIGN EQUATIONS FOR TYPE-I AND TYPE-II STRUCTURES;
PARAMETER b CORRESPONDS TO GB_1/GB_2

III. COMPENSATION REQUIREMENTS

Expressions (4)–(8) allow considerable freedom in choosing the different design parameters. In fact, many choices are possible and some of them correspond to particular cases which have been reported elsewhere [1]–[5]. Hence, in order to take advantage of that freedom we will identify the problem of what must be optimized in a compensated VCVS. Basically, authors engaged with that question have considered two different approaches, emphasizing either magnitude-oriented or phase-oriented compensation criteria.

A design based on the phase-compensation must minimize the low-frequency phase error [4]. That error, from (1), is approximately given by

$$\phi(w) \simeq \tan \phi(w) \simeq \frac{w}{w_0} \left(\frac{w_0}{w_c} - \frac{1}{Q} \right) - \frac{w^3}{w_0^3} \frac{1}{Q} \left(1 + \frac{w_0^2}{w_c^2} - \frac{w_0}{w_c} \frac{1}{Q} \right) + \cdots$$
 (9)

From (9) it is clear that we must impose the condition

$$Q = \frac{w_c}{w_0} \tag{10}$$

in order to reduce the value of $\phi(w)$ to

$$\phi(w) \simeq -\frac{w^3}{w_0^3} \frac{1}{Q}. \tag{11}$$

In the phase-oriented case the purpose of the design technique is twofold. The remaining phase-error must be reduced to a minimum while at the same time extending as much as possible the effective bandwidth, BW', which will be defined as the frequency at which the gain value is increased by 3-dB.¹ After routine calculations we get, using (10)

$$BW' = w_0 \sqrt{\left(1 - \frac{1}{4Q^2}\right) + \sqrt{\left(1 - \frac{1}{4Q^2}\right)^2 - \frac{1}{2}}} . \quad (12)$$

From (11) and (12), it should be clear that a "good" phase

compensated design requires obtaining the highest w_0 and Q values compatible with (10).

A magnitude-oriented compensation scheme has to be directed towards maximizing the frequency range where the magnitude response is flat. From (1) this results in

$$Q = \frac{w_c/w_0}{\sqrt{1 + 2\frac{w_c^2}{w_0^2}}}.$$
 (13)

Furthermore, a condition may be derived consisting in maximizing the 3-dB bandwidth of the circuit. From Geiger's paper [1] that bandwidth is given with (13) by

BW =
$$w_0 \sqrt{\frac{1}{2Q^2} - 1 + \sqrt{\frac{1}{4Q^4} - \frac{1}{Q^2} + 2}}$$
 (14)

Then a maximum of BW compatible with (13) must be looked for.

IV. PRACTICAL CIRCUITS

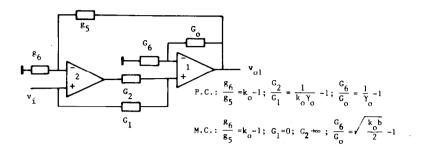
Table I provides the design equations for type-I and type-II structures. In what follows, we shall name these equations in a compact way by using a matrix-like terminology. For instance, the equation giving BW for the type-II will be termed as (II-7). These design equations have to be completed with the interconnection requirements given by (7) and (8). Matched operational amplifiers were not assumed since both structure types are sensitive to GB mismatch in a different way.

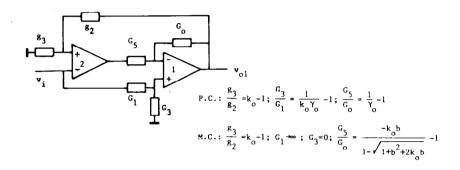
In fact, we can generate different compensated VCVS's by considering the combinations of the sign of the parameters in (7) and (8) which are compatible with the equations on Table I as well as with the stability conditions given by (6). Also, for type-II structures it is interesting to impose the additional constraint:

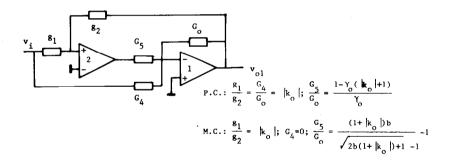
$$\operatorname{sgn}(c_1 \gamma_0) = \operatorname{sgn}(c_2 \gamma_1) = \operatorname{sgn} k_0 \tag{15}$$

which avoids an unnecessary limitation on the attainable value for m, in Table I.

Figs. 2 and 3 show all the resulting practical circuits. In each







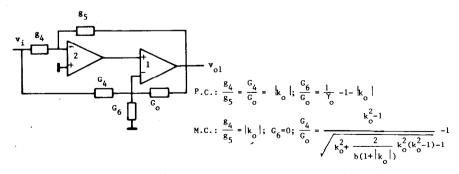
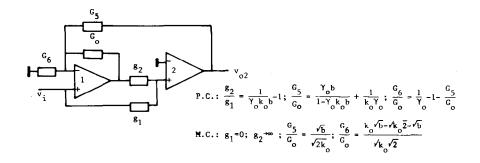
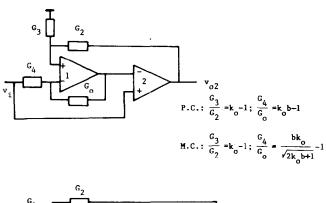
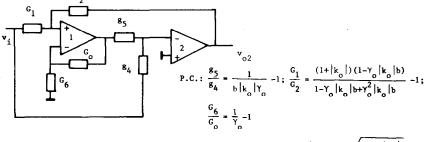


Fig. 2. Circuit configurations for type-I compensated amplifiers: CI.1; CI.2 [4] CI.3 [5]; CI.4 [4]. Parameter b corresponds to GB_1/GB_2 .







M.C.:
$$g_4=0$$
; $g_5\to\infty$; $\frac{G_1}{G_2}=|k_o|$; $\frac{G_6}{G_o}=\sqrt{\frac{b(1+|k_o|)}{2}}$ -1

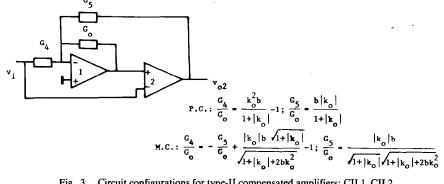


Fig. 3. Circuit configurations for type-II compensated amplifiers: CII.1, CII.2 [1][3] CII.3 and CII.4. Parameter b corresponds to GB_1/GB_2 .

TABLE II(a) Parameter Values for Phase Compensation; $k_0 > 0$; Parameter b Corresponds to GB_1/GB_2

Teter signs an interconection requirements.	n	Optimum design	parameter	values	
	Υ ₁	Υ2	°1	°2	m .
$\begin{array}{c} c1.1\\ (c_1, Y_1, Y_2) > 0\\ c_2 < 0\\ Y_1 + Y_2 = 1 \end{array}$	Y _o k _o	1-Y _o k _o	1	- \frac{1}{k}_0	1/o (1-7 o k o)
$\frac{\text{CI.2}}{(c_2, Y_1) > 0}$ $(c_1, Y_2) < 0$ $Y_0 - Y_2 = 1$	Y _o k _o	Y _o -1	-1	1 k o	ل (۱-۲ _۰)
$\frac{\text{CII.1}}{(c_1, c_2, Y_1) > 0}$ $\frac{Y_2 < 0}{(c_1 + c_2 = 1)}$ $\frac{Y_0 - Y_2 \le 1}{(c_1 + c_2 = 1)}$	1	$-\frac{1+\gamma_{o}k_{o}h(\gamma_{o}-1)}{k_{o}(1-\gamma_{o}k_{o}h)}$	Yokob	1-c ₁	$\frac{1}{k_o} \{1 - k_o \gamma_o b (1 - \gamma_o)\}$
$\frac{\text{CII.2}}{(c_1, \gamma_2) > 0}$ $(c_2, \gamma_1) < 0$ $\gamma_0 = \gamma_1 = 1$	Y_0^{-1} $Y_0 = \frac{1}{k_0 b}$	1 k o	1	-1	l k o

TABLE II(b) PARAMETER VALUES FOR PHASE COMPENSATION; $k_0 < 0$; PARAMETER b Corresponds to GB_1/GB_2

requirements	Optimum design parameter values						
	Υ1	$^{Y}_2$	c ₁	c ₂	•		
$\frac{\text{C1.3}}{(c_1, c_2) > 0}$ $(\gamma_1, \gamma_2) < 0$ $(\gamma_1 + c_2 = 1)$ $(\gamma_0 - \gamma_1 - \gamma_2 = 1)$	۲ ₀ k ₀	Υ _ο ~Υ ₁ -1		1 1+ k ₀	$\frac{1}{1+ k_{o} } \{1-\gamma_{o}(1+ k_{o})\}$		
$\frac{\text{C1.4}}{Y_2 > 0}$ $(c_1, c_2, Y_1) < 0$ $c_1 + c_2 = -1$ $Y_0 - Y_1 = \alpha$	Y _o k _o	I	$\frac{- \mathbf{k}_o }{1+ \mathbf{k}_o }$	-1 1+ k _o	1 1+ k ₀		
$\frac{\text{C11.3}}{(Y_1, Y_2) > 0}$ $\frac{(c_1, c_2) < 0}{(c_1 + c_2) = 1}$ $\frac{(c_1 + c_2) < 0}{(c_1 + c_2) = 1}$		$\frac{1}{1+ k_{o} }(1+\frac{\gamma_{o}^{2} k_{o} b}{1-\gamma_{o} k_{o} b})$	Y _o k _o b	-1-c ₁	$\frac{1}{1+ k_o }(1- k_o \gamma_ob+\gamma_o^2 k_o b)$		
$\begin{array}{c} \text{CII.4} \\ c_2 > 0 \\ (c_1, \gamma_1, \gamma_2) < 0 \\ \gamma_0 - \gamma_1 - \gamma_2 = 1 \end{array}$	$Y_o = Y_2 = 1$ $Y_o = \frac{1}{ \mathbf{k} \mathbf{b} }$	$\frac{-1}{1+ \mathbf{k_o} }$	-1	1	1 1+ k _o		

circuit the actual resistor ratios must be choosen in order to fulfill either the phase or the magnitude compensation condition. Next, we will consider the particular choices for both compensation conditions.

Circuit, para

A. Phase Compensation

Phase compensation conditions have been applied to both type-I and type-II structures. The results are summarized in Table II(a) for $k_0 > 0$ and Table II(b) for $k_0 < 0$. A few remarks

TABLE III(a) PARAMETER VALUES FOR MAGNITUDE COMPENSATION; $k_0 \ge 0$; PARAMETER b Corresponds to GB_1/GB_2

Circuit	Optimum design parameter values					
	Yo	Yı	Υ2	c ₁	c ₂	
CI.1	$\sqrt{\frac{2}{k_o b}}$	o o	1	1	- l	
C1.2	$\frac{1}{bk}(\sqrt{1+2k_0^2+b+b^2}-1)$	1	Y ₀ -1	-1	$\frac{1}{k}_{o}$	
C11.1	$\sqrt{\frac{2}{bk_o}}$	1	$-\frac{1}{k}$	0	1 .	
C11.2	$\frac{1}{k_0 b} \sqrt{1 + 2k_0 b}$	Υ ₀ -1	l k o	1	-1	

TABLE III(b)

PARAMETER VALUES FOR MAGNITUDE COMPENSATION; $k_0 < 0$;

PARAMETER b CORRESPONDS TO GB_1/GB_2

Circuit	Circuit Optimum design parameter values						
	Y	Y 1	Y 2	c ₁	c ₂		
C1.3	$\frac{\sqrt{2b(1+ k_0)+1} -1}{(1+ k_0)b}$	9	Y _o -1		1 1+ k _o		
CI.4	$\frac{1}{k_o^2 - 1} (\sqrt{k_o^2 + \frac{2k_o^2(k_o^2 - 1)}{b(1 + \frac{1}{2}k_o)}} - 1)$	Y _o -1	1	- k _o 1+ k _o	-1 1+ k _o		
C11.3	$\sqrt{\frac{2}{b(1+ k_0)}}$	k _o + k _o	$\frac{1}{1+ \mathbf{k}_{o} }$	n	-1		
C11.4	$\frac{1}{b k_o } \sqrt{\frac{2bk_o^2}{1+ k_o } + 1}$	Yo-Y2-1	-1 1+ k _o	-1	1		

are noteworthy:

- 1) Note from (I-2) and (II-2) that $|c_2|$ and $|\gamma_2|$ have to be selected as high as possible in order to attain a maximum value for w_0 . Hence, the interconnection requirements involving such a parameter have been chosen as unity whenever it does not give rise to a contradiction with the design equations.
- 2) The values of the different parameters are listed as functions of γ_0 and k_0 . In most cases, the designer is free to choose the particular value for γ_0 but, from the expressions for BW' and ϕ (see Table I), it should be clear that γ_0 must be selected as small as possible in order to optimize the compensation.
- 3) An additional constraint on the minimum value for γ_0 is derived from a more detailed stability analysis including the operational amplifier's second pole [7]. It results in

$$\gamma_0 \frac{w_{21}w_{22}}{GB_2(w_{21} + w_{22})} + \gamma_0^2 \frac{GB_1}{GB_2} \frac{w_{21}^2}{(w_{21} + w_{22})^2} > |c_2\gamma_2| \quad (16)$$

where w_{2i} is the location for the *i*th (i=1,2) operational amplifier's second pole.

B. Magnitude Compensation

Table III(a) and III(b) depict the results of applying the magnitude compensation conditions to both types of structures. For every circuit, the parameter values allowing to attain a maximum BW are shown. These particular values have been

derived by a computer-aided numerical analysis on the c_1 and γ_1 values.

V. DISCUSSION

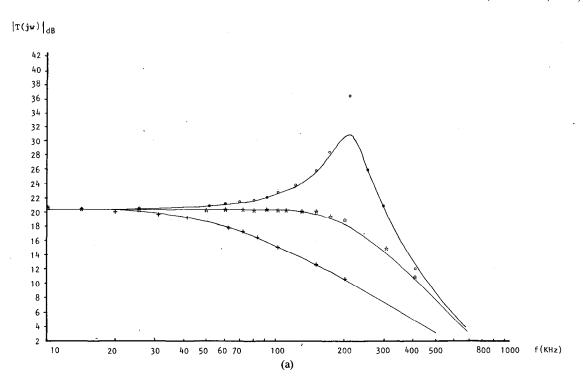
For convenience, we shall consider separately two cases depending on the sign of k_0 . A number of conclusions follow for both of them.

A.
$$k_0 > 0$$

From a phase compensation point of view the circuit CI.2 exhibits performance superior to that of circuit CI.1. It is due to the fact that for the same γ_0 the former allows to obtain a higher (lower) value for $m(\phi)$, defined in Table I, than the latter. It must be remarked that Reddy's circuit [4] is a special case of circuit CI.2, for $\gamma_0 = 1/k_0$. The maximum value for m is obtained for the circuit CII.2 [3]. Nevertheless, the circuit CI.2 allows to attain a lower phase error and higher BW' than CII.2 whenever γ_0 for the former is selected, respectively, to be

$$\frac{\gamma_0}{(1-\gamma_0)^2} < \frac{1}{k_0}$$
 or $\frac{\gamma_0}{\sqrt{1-\gamma_0}} < \frac{1}{k_0}$. (17)

At the other hand, the maximum BW is obtained for circuit CII.2 in accordance with Geiger's paper [1]. Moreover, it is important to note that circuits CI.1 and CII.1 have infinite input impedance, and in addition obtaining a BW value which is not



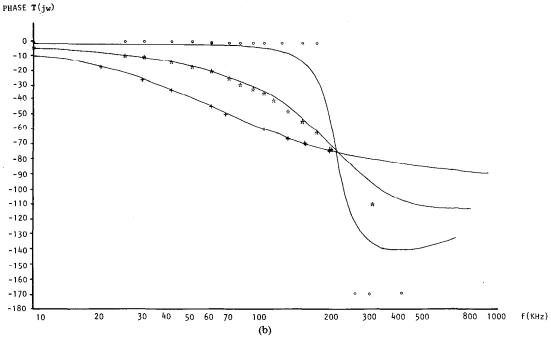


Fig. 4. Circuit CII.2 compensated amplifier for $k_0 = 10.9$. (a) Magnitude characteristics. (b) Phase characteristics. continuous trace lines correspond to the theoretical responses.

- $\,+\,$ corresponds to the measured response for the uncompensated amplifier.
- * corresponds to the measured response for the magnitude compensation.
- o corresponds to the measured response for the phase compensation.

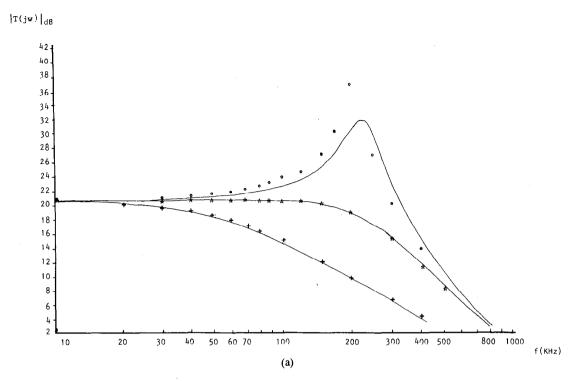
too far from the one obtained by the Geiger's circuit (see Table I).

$$B. k_0 < 0$$

For phase compensation, the circuits CI.4 and CII.4 yield the maximum value for m, defined in Table I. Moreover, the circuit

CI.4 allows lower phase errors than CII.4. The former has been previously reported by Reddy for $\alpha = 1$, α defined in Table II(b) [4]. However, for magnitude compensation, the maximum BW is obtained from circuit CII.4.

Finally, it is interesting to note that the phase compensation condition remains still valid for type-I structures no matter what



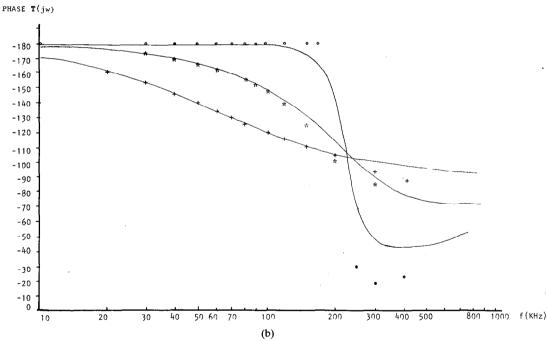


Fig. 5. Circuit CII.4 compensated amplifier for $k_0 = -10.9$. (a) Magnitude characteristics. (b) Phase characteristics.

the degree of mismatch. This is an advantage when compared with phase-compensated type-II circuits. Quite in the contrary, for magnitude compensation, both types are sensitive to the mismatch, as can be seen on Tables I and III.

VI. EXPERIMENTAL RESULTS

As an example of the performance of the different circuits, we show the magnitude and phase characteristics for the CII.2 and CII.4 considering both magnitude- and phase-compensation cases. Fig. 4 depicts the magnitude and phase response for the circuit CII.2 with $k_0 = 10.9$. Alternatively, Fig. 5 depicts the correspond-

ing characteristics for the circuit CII.4 with $k_0 = -10.9$. For both circuits we have used μ A747 dual operational amplifiers.

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