Nonlinear Switched-Capacitor Networks: Basic Principles and Piecewise-Linear Design

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Abstract — **The applicability of switched-capacitor (SC) components to the design of nonlinear networks is extensively discussed in this paper. The main objective is to show that SC's can be efficiently used for designing nonlinear networks. Moreover, the design methods to be proposed here are fully compatible with general synthesis methods for nonlinear n-ports. Different circuit alternatives are given and their potentials are evaluated.**

GLOSSARY OF COMMON TERMS

ϕ^e	Even clock phase.
ϕ^o	Odd clock phase.
S^e	Electronic switch being closed during the even clock phase.
S^o	Electronic switch being closed during the odd clock phase.
f_c	Clock frequency.
T_c	Clock period.
i	Current in the continuous time domain.
v	Voltage in the continuous time domain.
q	Charge in the continuous time domain.
$\hat{I}$	Average current at an arbitrary clock period.
V	Sample voltage at an arbitrary clock period.
Q	Sample charge at an arbitrary clock period.
V^e	Sample voltage at an arbitrary even clock phase.
V^o	Sample voltage at an arbitrary odd clock phase.
$\hat{V}$	Voltage source comprising previous values of voltages and charges in a discretized model.
E	Constant voltage.
m	Slope of a linear segment from a piecewise-linear characteristic.
δ	Discontinuous jump from a piecewise-linear characteristic.
V_{sat}	Voltage saturation level for op amps and unity-gain-buffers.
$\delta(t)$	Time impulse function.

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Further, some of the previous terms can be specialized with subscripts in different ways: 1) To denote a particular discrete time instance, i.e., V_{n+1}; 2) To denote a particular segment into a piecewise-linear characteristic, i.e., m_j; and 3) to denote that a variable is associated to a specific element or point into a circuit, i.e., V_C^o or V_1.

I. INTRODUCTION

AT PRESENT, any procedure for the synthesis or design of circuits is strongly influenced by its technological feasibility for large scale integration. In connection with signal processing, several techniques (analog, sampled-data, and purely digital) have evolved exhibiting specific advantages which render them potentially useful for VLSI. Without a doubt, one of such techniques is the use of *switched-capacitors* (*SC*) for filtering of continuous as well as sampled-data signals. The state of the art has given rise to a new field where many design methods have gained popularity and where specific analysis procedures and simulation programs have been developed. What mainly makes SC filters attractive is the present day fabrication tolerances of capacitors built with MOS technologies, another appealing feature being their compatibility with digital circuits. Thus combined digital–analog circuits on the same LSI chip may be mass-produced in the future.

The purpose of this paper is to discuss the applicability of SC techniques to the design of *nonlinear* networks. Up till now, only modest attempts in the use of SC techniques for designing nonlinear components have been made [1]–[5]. Work in this area has been devoted to synthesizing nonlinear functions for specific applications, the interest in designing SC multipliers being remarkable [2], [3]. However, to the best of our knowledge, no general methods have yet been developed for synthesizing nonlinear characteristics using SC networks. This discourages use of SC methods in those applications where a nonlinear transformation is required, as for instance, in AGC circuits, curve fitting, adaptive filters, and so on. Our goal here is to investigate the use of SC's for designing nonlinear components in a way compatible with general synthesis methods for *nonlinear n-ports*. Different synthesis methods have been reported in the past for the realization of nonlinear multiports, but all of them require the design of specific nonlinear elements using off-the-shelves components such

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as op-amps, diodes, etc. We will extend some of these methods by giving an implementation technique which is based on *SC components*. Section II reviews some basic ideas in order to clarify the difference between SC filters, where we are always interested in *transfer relations*, and SC circuits, where we are also interested in *driving-point* functions. Essentially, it is emphasized that a switched-capacitor is not a true resistor but a pseudoresistor and the concept of *SC-resistor* is proposed. This concept is formalized in Section III, where two methods are given for implementing any *piecewise-linear* (PL) SC-resistor. Thus Section III is the core of the paper in the sense that our main goal of generalizing continuous nonlinear synthesis techniques using SC-resistors is presented. Section IV considers the *stability properties* of the basic building blocks introduced in Section III. The importance that a detailed stability study has on refining the new design methods must be kept in mind. Next, Section V deals with the realization of transfer characteristic plots (TC-plots) by using SC-resistors. Finally, Section VI shows how a sampled-data TC-plot may be used to synthesize continuous nonlinear resistors. Summarizing, we will introduce the concept of SC-resistors and give procedures to implement them in the design of discrete-time as well as continuous-time nonlinear circuits.

II. SC-Resistors: Preliminaries

Most design techniques for linear SC networks involve the use of the so-called SC building blocks (SCBB) which function as conductances [5]–[7] or transconductances [8]. Basically, such elements function by sampling a floating voltage and providing charges which are proportional to the sampled voltage. As it was stated in Section I, our aim in this paper is to extend the basic idea underlying the use of SC components in the synthesis of nonlinear networks. To this end, the first step is the development of a technique for designing nonlinear SC conductances in a way compatible with current MOS technologies. Subsequently, such new elements are used in turn as building blocks for synthesizing nonlinear driving point (DP) and TC plots, in close analogy with the synthesis procedures for continuous nonlinear networks [10], [11]. Since the intention of this paper is to illustrate both the basic approach and its limitations, we will be only concerned with the realization of PL networks. A companion paper will be devoted to describing other approaches that are also compatible with SC techniques.

A *truncation operator* is the only nonlinear function that must be added to the set of SC linear components for synthesizing PL networks. Let us define what we will call a *threshold controlled switch* (TCS) as the circuit component represented in Fig. 1. There, port 2 is implemented by an electronic switch whose conduction state is controlled by the logic variable Z_2, i.e., it turns ON for $Z_2 = 1_B$ and turns OFF otherwise. Further, the logic value of Z_2 depends on the voltage associated with port 1 as follows

$$Z_2 = \begin{cases} 1_B, & \text{for } V_1 > E \\ 0_B, & \text{otherwise} \end{cases} \tag{1}$$

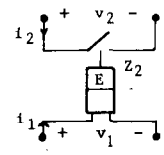


Fig. 1. Circuit representation for a threshold controlled switch. The rectangular block stands for an implementation of the threshold operation defined by (1). The logical value of $Z2$ controls the state of the switch.

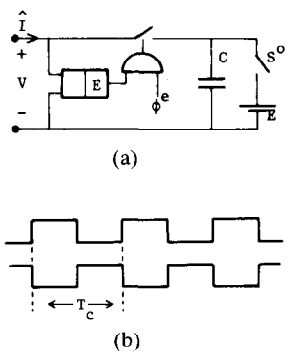


Fig. 2. (a) Circuit realization of a positive concave SC conductance using a TCS. The switch is controlled by combining both the TCS output and the even clock phase through an AND gate. (b) Time diagram showing both clock phases for the circuit of Fig. 2(a).

where 1_B and 0_B denote "one" and "zero", respectively, in the binary number system.

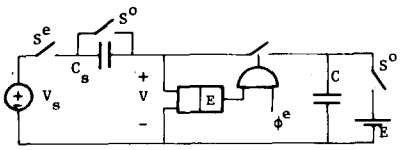
Fig. 2(a) shows an example of the use of a TCS for implementing a positive concave SC conductance. Fig. 2(b) shows the corresponding timing diagram. It is assumed that the switch named S^o (alternatively S^e) turns ON in synchronization with the odd (even) clock phase. After imposing some restrictions on the electrical variables, it is possible to get the average charge as a function of the voltage

$$\hat{I} = \begin{cases} (Cf_c)(V - E), & \text{for } V > E \\ 0, & \text{elsewhere} \end{cases} \tag{2}$$

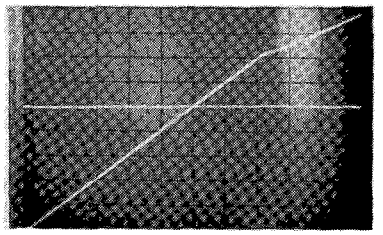
where C denotes the capacitance in Fig. 2(a) and f_c denotes the clock frequency. Linear SC circuits in addition to circuits like the one shown in Fig. 2(a) lead to the definition of a new type of networks, namely the SC-resistors. We have chosen the name SC-resistor to emphasize the pseudoresistive character of the SC. However, the name, as well as its pseudo-resistive character, may be misleading if we do not carefully consider the way in which SC-resistors may be used to implement TC and DP plots (either linear or nonlinear). The use of such "resistors" for designing TC plots is direct. See for example the simple voltage divider shown in Figure 3(a), where the concave resistor of Fig. 2 is utilized. Using (2) we obtain the following TC plot:

$$V = \begin{cases} V_s \dfrac{C_s}{C_s + C} + E \dfrac{C}{C_s + C}, & \text{for } V_s > E \\ V_s, & \text{elsewhere} \end{cases} \tag{3}$$

The oscillogram in Fig. 3(b) depicts the actual TC plot measured with $C_s = C = 1$ nF and $E = 2$ V.



(a)



(b)

Fig. 3. (a) Nonlinear SC voltage divider using the SC conductance in Fig. 2(a). (b) Experimental TC plot for the circuit in Fig. 3(a) with $C = C_s = 1$ nF and $E = 2$ V; vertical signal; V scale: 1 V/dv horizontal signal; V_s, scale: 1 V/dv.

The constitutive relation describing any SC-resistor is valid under the same restrictions that apply to conventional SC-filters; namely,

1) Excitation signals are sampled and held until they change in synchronization with the clock waveform.
2) Electrical variables in the network are only of interest when no charge is flowing through any branch and all of the voltages are constant.

The design of DP plots has to be considered more carefully. In fact, the above constraints preclude the use of SC-resistors for designing continuous-time DP plots, and the inclusion of some auxiliary elements is required. It is tempting to use the analogy given by (2), but we must keep in mind that in DP plot synthesis we are interested in obtaining relations linking *instantaneous* voltage and current at a physical port. It is not enough to find a switching scheme that nullifies the "memory" of a capacitor. If we do that, we still have a capacitor. Indeed, note that although we will obtain an *algebraic* relation between the *average* voltage and the average current, a *differential* relation exists between their *instantaneous* values.

Our problem boils down to implementing a physical resistor using SC-resistors. To do this, we convert an instantaneous $q-v$ characteristic into an instantaneous $i-v$ relation by connecting an SC-resistor to a mutator [15]. Hence, our problem is to find a mutator circuit which is compatible with the SC design philosophy. The circuit of Fig. 4 fits this specification. In this figure, the symbol at the right denotes a SC-resistor. We have assumed that charge only flows through the SC resistor during the even clock phase and is an algebraic function of the voltage samples. Then, the charge is integrated by C_o, giving a voltage V_{C_o}, which is converted into the current i via a voltage-controlled current-source (VCCS). It must be mentioned that this source is the only part of the mutator that requires a resistive element, as will be seen later on.

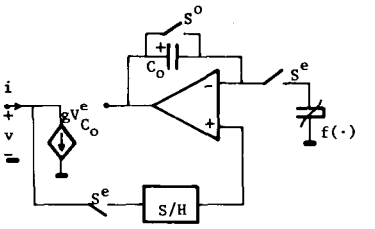


Fig. 4. Conceptual circuit diagram for a SC mutator.

Thus, the process of implementing a resistive DP plot using SC techniques can be described as follows:

1) Implement an SC-resistor by interconnecting as many SC building blocks as needed.
2) Transform the SC DP plot into a TC plot.
3) Convert the TC plot into a resistive DP plot.

We can conclude, therefore, that both TC and DP plot synthesis may be treated in a unified way with respect to SC-resistors; the only significant difference being the use of a mutator when DP characteristics are required. Consequently, we will devote the next section to the formal synthesis procedures for SC-resistors, keeping in mind their usefulness for performing both types of plots.

III. Synthesis of SC-Resistors

3.1. Discretized Capacitive Models for Nonlinear Resistors: The SC-Resistor Approach

In Section II SC-resistors appears in a rather simple way. Let us now define them in a more precise manner. In fact, it follows from the example in Fig. 3, that the synthesis of TC plots using SC techniques can be viewed as a procedure for simulating resistors. Thus, our aim here is to find "substitution" models for nonlinear resistors which allow us to simulate them using SC techniques.

Let us consider a time-invariant voltage-controlled resistor described by

$$i = f(v). \tag{4}$$

We will try to simulate this resistor by using a sampled-data system built basically with capacitors and switches. Our natural variables in this case are charges and voltages. Choosing these variables, (4) may be written as a first-order differential equation

$$\frac{dq}{dt} = f(v). \tag{5}$$

The simulation we propose to perform is essentially discrete in nature. Thus, inside any sampling period we must resort to a discrete equivalent of (5). Of course, we can use the model associated with any numerical integration algorithm for representing the time derivative of q. Furthermore, applying the general formula for multistep algorithms [12], we obtain the following discrete version of (5), valid for the time $t = t_{n+1}$:

$$Q_{n+1} - Q_n = T_c \sum_{j=-1}^{p} b_j f(V_{n-j}) + \sum_{j=1}^{p} a_j Q_{n-j} \tag{6}$$

where T_c is the sampling clock period.

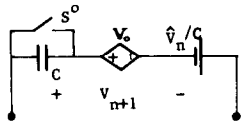


Fig. 5. Discretized capacitive model for a nonlinear resistor.

To emphasize some aspects of this expression, let us rewrite it as follows:

$$Q_{n+1} - Q_n = T_c b_{-1} f(V_{n+1}) + \hat{V}_n \tag{7.a}$$

where

$$\hat{V}_n \triangleq T_c b_0 f(V_n) + \sum_{j=1}^{p} \left\{ T_c b_j f(V_{n-j}) + a_j Q_{n-j} \right\}. \tag{7.b}$$

Observe that, since $\hat{V}_n$ depends on the previous values of voltage and charge, it is a constant at the present time interval. Hence, we may interpret (7) as the $Q-V$ curve of a nonlinear capacitor. We can, therefore, assert that a discretized capacitive circuit model for a nonlinear resistor associated with a general multistep integration algorithm at the time $t = t_{n+1}$ is simply the one-port network shown in Fig. 5. Note that C is a linear capacitor and the switch is periodically closed and open in synchronization with the clock. Hence, if the voltage-controlled source is given by

$$V_o = V_{n+1} - f(V_{n+1}) \tag{8}$$

the equation describing the network at $t = t_{n+1}$ becomes

$$Q_{n+1} - Q_n = Cf(V_{n+1}) + \hat{V}_n \tag{9}$$

which is equivalent to (7). Hence, we may formalize the concept of a SC-resistor as follows:

Definition 1: The circuit implementation of any *capacitive discretized model* for a resistor is said to be a SC-resistor iff the components used are linear capacitors, ideal switches, and voltage-controlled voltage-sources (VCVS).

Remark 1: In Definition 1, independent voltage sources are considered as a *degenerate* VCVS.

Remark 2: Expression (9) suggests that inside any sampling interval, there is a static description for a SC-resistor given by

$$g(V, \hat{I}) = 0 \tag{10}$$

where $\hat{I}$ is the average charge flowing during that sampling interval. The term static is used here to mean dc excitations.

Depending on the properties of $g(\cdot, \cdot)$, we may define several subclasses of SC-resistors. For illustrative purposes, we will consider next linear SC-resistors, since it is interesting to relate our work here with the known linear applications of SC networks.

Definition 2: A SC-resistor is said to be linear if $g(\cdot, \cdot)$ in (10) is a linear function.

Definition 3: A linear SC-resistor is said to be *one-step linear* if its associated capacitive discretized model has the form

$$Q_{n+1} - Q_n = GT_c(b_{-1}V_{n+1} + b_o V_n) \tag{11}$$

where G denotes the conductance of the simulated resistor.

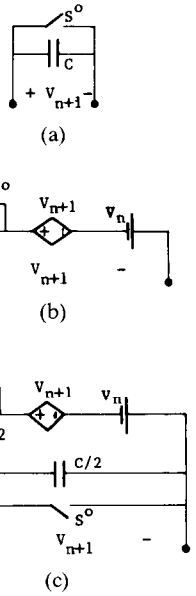


Fig. 6. (a)–(c) Discretized models for linear BE-, FE-, and TR-SC-resistors: (a) BE. (b) FE. (c) TR.

Remark 3: Particular cases of (11) are SC-resistors derived from the following three well-known algorithms; namely,

a) Backward Euler (BE): $b_{-1} = 1,\ b_o = 0$
b) Forward Euler (FE): $b_{-1} = 0,\ b_o = 1$
c) Trapezoidal rule (TR): $b_{-1} = 1/2,\ b_o = 1/2.$

Linear SC-resistors do not share all the properties of continuous resistors. This should not be surprising because they are circuit implementations of a model. The basic properties of linear SC-resistors depend on the integration algorithm on which they are based. For example, consider the 3 one-step linear resistors defined above. Fig. 6 shows three circuits associated respectively with the BE, FE, and TR algorithms. In all of these figures it is assumed that $C = T_c G$. The only passive realization corresponds to BE which does not require a voltage source. This is to be expected because BE is the only strictly passive algorithm from this set of three [13]. Roughly speaking, BE is the one-step linear SC-resistor which best resembles a continuous resistor since its storage property has been removed. On the other hand, the TR algorithm is lossless. This motivates the search for other implementations not requiring sources. One of them is the well-known SC-resistor shown in Fig. 7, which has been introduced in the SC filter literature from the bilinear transformation [6].

Two interesting conclusions from the preceding paragraph are: 1) previous SC realizations of one-port elements are included in the one-step linear SC-resistors appearing here in a much more general context; 2) both the function structure of $g(\cdot, \cdot)$ and the properties of the integration algorithm used in the simulation of SC-resistors are important.

Nevertheless, the type in which we are really interested here is that of PL SC-resistors.

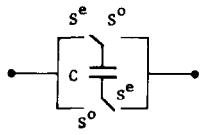


Fig. 7. Circuit diagram for a bilinear SC-resistor [6].

Definition 4: An SC-resistor is said to be *piecewise-linear* (*PL*) if it can be described by a PL function.

In what follows, we focus on methods for simulating PL SC-resistors. Two design approaches will be developed, one based on FE and the other on BE, since they can be shown to give the simplest circuit configurations [14]. On the other hand, TR SC-resistors can always be designed by connecting one BE SC-resistor in parallel with one FE SC-resistor, as shown in Fig. 6, for the linear case.

Limiting ourselves to one-step algorithms is not so restrictive as it relates to the current practice in linear SC networks. In fact, extensions of linear SC filters to include multistep algorithms have not been reported to the best of our knowledge. However, they may be of interest at least from a theoretical point of view. For instance, the second-order Gear algorithm is passive [13] and hence, could be implemented by using only ideal switches and linear capacitors. Indeed, a systematic search of the applications of passive multistep algorithms to the simulation of linear and nonlinear resistors could lead to new realization schemes for either filters or nonlinear circuits.

3.2. Synthesis of PL SC-Resistors

Let us consider a PL SC-resistor with $N+1$ segments and N breakpoints in $E_1, E_2, \cdots, E_N$. Following the results reported in [9], a global function describing such a generic element is given by

$$\hat{I} = \frac{1}{T_c}\left\{ m_o V + f^o(0) + \frac{1}{2}\sum_{j=1}^{N}\left\{1+\operatorname{sgn}(V-E_j)\right\} \cdot \left\{\delta_j + (m_j - m_{j-1})\right\}(V-E_j)\right\} \quad (12)$$

where

$$\operatorname{sgn}(x) = \begin{cases} 1, & \text{for } x > 0 \\ -1, & \text{elsewhere} \end{cases} \quad (13)$$

and δ_j denotes a discontinuous jump at the jth breakpoint, m_j denotes the slope of the jth segment, and $f^o(0)$ denotes the ordinate at $x = 0$ corresponding to the extension of the leftmost segment of the PL curve.

The last expression suggests the introduction of a family of basic elements for designing PL SC-resistors.

a) *Positive Concave SC-Resistor* (PCSC): This element is described by

$$\hat{I} = \begin{cases} 0, & \text{for } V < E \\ \dfrac{m}{T_c}(V-E) + \dfrac{\delta}{T_c}, & \text{elsewhere} \end{cases} \quad (14)$$

where m is a positive number and E is any constant voltage.

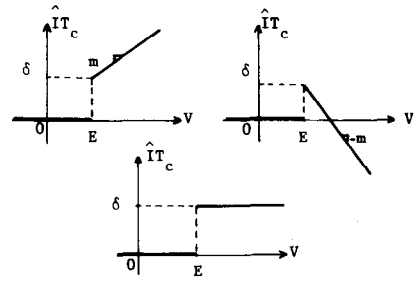


Fig. 8. $\hat{I}-V$ port characteristics for the basic PL SC-resistors.

b) *Negative Concave SC-Resistor* (NCSC): This element is described also by (14) but with a negative value for m.

c) *Step Charge Source:* This element is described by

$$\hat{I} = \begin{cases} 0, & \text{for } V < E \\ \dfrac{\delta}{T_c}, & \text{elsewhere.} \end{cases} \quad (15)$$

Fig. 8 plots the characteristics corresponding to these three basic components. It is interesting to point out that these elements are similar in form to those in [10] except for the presence of a discontinuity in the PCSC and the NCSC. Allowing this discontinuity improves the element's versatility from a design point of view.

It should be clear that every term in (12) may be identified as one of the basic elements just introduced. Obviously, any PL SC-resistor may then be designed by connecting in parallel as many elements of the basic set as required. The problem yet to be solved is how to design these basic elements using SC's. Solutions corresponding to both one-step algorithms chosen in Section 3.1 are given in the next subsections.

3.3. Design Technique Based on the BE Algorithm

Fig. 9 shows the circuit realization of the basic elements using switched capacitor techniques. The required threshold controlled switch has been built by the circuit in Fig. 10(a). This is not the only realization but the fastest and simplest one. Alternative procedures using special purpose A/D-like converters to generate several thresholds have also been studied by the authors and will be reported elsewhere [14]. Notice further that the active circuits shown in Fig. 11 are grounded SC-resistors. Floating realizations can also be obtained by using appropriate converters [10], [11].

Let us describe first the PCSC shown in Fig. 9(a). The switch named S_E^e is controlled by implementing the AND operation of the even clock phase and the comparator output. During the odd phase this switch remains open and the capacitor C is charged to a voltage equal to $E - \delta/C$. During the even phase, the switch S_E^e closes when $V > E$, resulting in $\hat{I}T_c = C(V-E)+\delta$. Otherwise, $(V < E)$, the switch remains open, thereby giving $\hat{I} = 0$. The slope of the characteristics is controlled by the value of C. Capacitor C_h is used to emphasize that the voltage sources will be derived from a common dc source for the different cells of the same system. A practical implementation of these voltages is given in Appendix A.

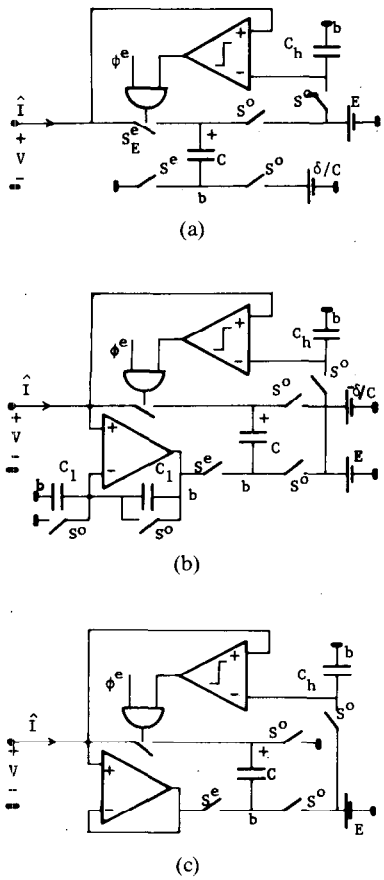


Fig. 9. (a)–(c) Circuit diagrams for the BE realizations of the basic PL SC-resistors: (a) BE-PCSC. (b) BE-NCSC. (c) Step-charge source.

Consider next the NCSC shown in Fig. 9(b). Let us assume that the comparator output is in the ON state ($V > E$). Then, during the odd phase capacitor C is charged to a voltage equal to $-E-\delta/C$ and both capacitors C_1 are discharged. During the even phase, the equivalent circuit of Fig. 10(b) is valid with $V_1 = 2$ V and the average current is $\hat{I} = (-C(V-E)+\delta)/T_c$.

Finally, let us consider the step-charge source shown in Fig. 9(c). Its functional description is similar to that of the NCSC, the main difference being that the voltage-controlled source associated with the equivalent circuit during the even phase (Fig. 10(b)) is $V_1 = V$. As a consequence, the average current during that phase for $V > E$ is CE/T_c.

3.4. *Design Technique Based on the FE Algorithm*

Fig. 11 shows the circuit implementation of both the PCSC and the NCSC grounded elements. The step-source characteristic does not depend on the port voltage and, therefore, its circuit realizations for BE and FE are similar. Notice that the circuits in Fig. 11 are mainly based on the use of unity-gain buffers. This fact is interesting, because the buffer has a rather quite simple structure from the integration point of view.

The operating principles of both networks in Fig. 11 are very similar. During any odd phase, capacitor C_h is charged to E and capacitor C is charged to

$$V_C^o = \mp (V_1^o - E) \tag{16}$$

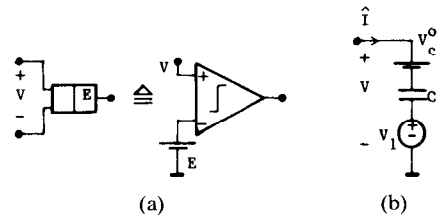


Fig. 10. (a) Design of a threshold function using a comparator. (b) Equivalent topology for both BE–NCSC and step-charge source during the even clock phase.

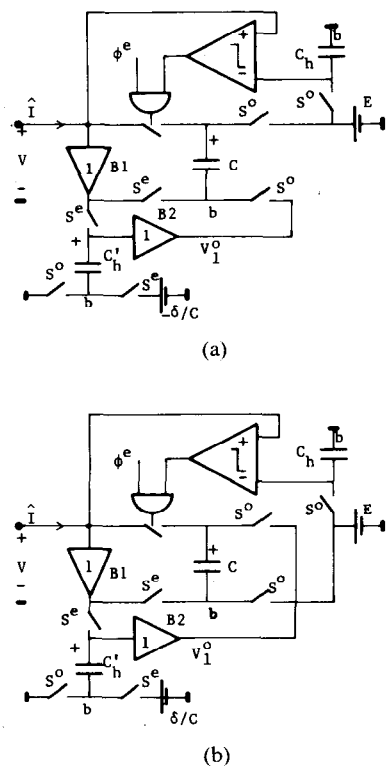


Fig. 11. Circuit diagrams for the FE realizations of the basic PL SC-resistors. (a) FE-PCSC. (b) FE-NCSC.

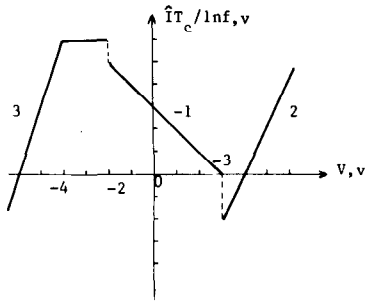
where the upper sign stands for the PCSC and the lower one for the NCSC. During the even phase, capacitor C_h' is charged to

$$V_{C_h'}^e = V_1^o = (V \pm \delta/C) \tag{17}$$

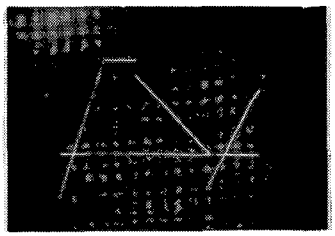
while capacitor C discharges on the input port if $V > E$, resulting in

$$\hat{I}T_c = -CV_C^o, \qquad \text{for } V > E. \tag{18}$$

By combining (16), (17), and (18), we obtain the expected PCSC (alternatively NCSC) characteristics. Furthermore, it should be noticed that the average current at any period does not depend upon the port voltage at the same period; instead, it depends on the port voltage at the previous clock period. This is a consequence of the timing associated with the FE algorithm, as shown by expression (7).



(a)



(b)

Fig. 12. (a) PL SC-resistor to be synthesized using basic elements. (b) Experimental result for the PL SC-resistor in Fig. 12(a). horizontal signal; V, scale: 2 V/dv vertical signal; $\hat{I}T_c$, scale: 2 V/dv.

3.5. *Experimental Results*

All of the proposed circuits have been built in the laboratory and satisfactorily tested. As an example we show the experimental results corresponding to the realization of the PL SC-resistor shown in Fig. 12(a). Fig. 12(b) shows the measured result. The synthesis procedure consists of decomposing the prescribed PL characteristics as the sum of the four basic PL curves shown in Fig. 13(a)–(d). The corresponding basic elements have been implemented by using the FE–PCSC and the FE–NCSC circuits.

3.6. *Static Limitations*

When dealing with the synthesis of nonlinear networks, it is very important to study the dynamic range of the circuit realization of the basic components used in the realization. By dynamic range we mean the port voltage interval inside which the linear operation is guaranteed for all the active elements. Since we are considering low-frequency excitations, linear operation is mainly restricted by the saturation mechanism of the op amps and unity-gain buffers. In what follows we shall assume a voltage saturation roll-off for the active elements, as shown in Fig. 14. Thus determining the dynamic range for any of the circuits in Figs. 9 and 11 is equivalent to finding the conditions relating the input voltage to the saturation level, V_{sat}. Such conditions are shown in Table I.

In addition to calculating the dynamic range limits, it is usually important also to model the network behavior when it is excited by a voltage that forces the circuit to operate outside the dynamic region, since many important dynamic properties depend on that behavior [15].

The way to handle this problem is well illustrated by the circuit in Fig. 15. There we have represented the different

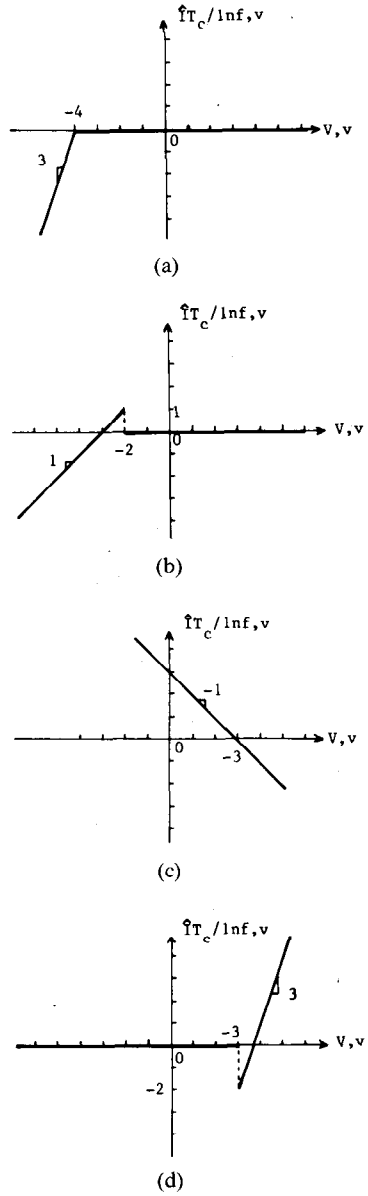


Fig. 13. (a)–(d) Component curves for synthesising the PL SC-resistor in Fig. 12(a) via basic elements.

possibilities for out-of-range operations for the FE–PCSC, assuming $V > E$. Routine analysis gives

$$\hat{I} = \frac{C}{T_c}\left(V - E + \frac{\delta}{C}\right) \tag{19.a}$$

$$\hat{I} = \frac{C}{T_c}(V_{sat} - E) \tag{19.b}$$

$$\hat{I} = \frac{C}{T_c}(V - E) \tag{19.c}$$

which correspond, respectively, to Fig. 15(a), (b), and (c).

The actual DP plot for the different saturation conditions can be determined by carefully analyzing the network behaviors in Fig. 15 when we force the input voltage beyond the saturation limits. In the case of Fig. 15, only two situations exist in practice, depending on which condi-

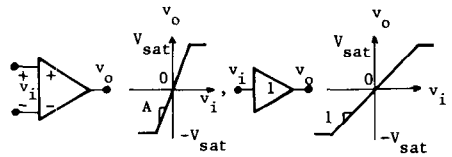


Fig. 14. Voltage saturation characteristics for the op amps and unity gain buffers used in the realization of the basic elements.

TABLE I
CONDITIONS GIVING THE DYNAMIC RANGE OF THE PL SC-RESISTORS

BENCSC	step charge	FEPCSC	FENCSC
$\lvert 2V\rvert \leq V_{sat}$	$\lvert V\rvert \leq V_{sat}$	$\sup\{\lvert V\rvert, \lvert V+\frac{\delta}{C}\rvert\} \leq V_{sat}$	$\sup\{\lvert V\rvert, \lvert V-\frac{\delta}{C}\rvert\} \leq V_{sat}$

tion in Table I is the most restrictive one; the corresponding DP plots are depicted in Fig. 16.

A similar analysis procedure has been applied to the remaining circuit realizations in Figs. 9 and 11. The corresponding models obtained are shown in Fig. 17 for both the BE and the FE elements [14]. In that figure the BE–PCSC is missing, since there is no controlled source directly governing the capacitor C.

Knowing the actual DP plots for BE and FE components gives us a comparative criterion for selecting an implementation style. Look for instance at both realizations of an NCSC. It should be clear that if $\delta/C > -V_{sat}/2$, the dynamic range of the FE circuit is greater than the one corresponding to the BE. Another interesting consequence is that the global DP plots for every circuit realization admits a *canonical PL representation*, as it was shown in [14].

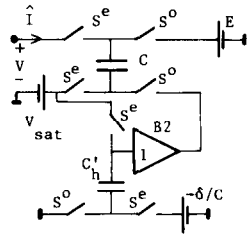
IV. STABILITY PROPERTIES

The basic building blocks introduced in Section III require active components and are, therefore, potentially unstable. In order to perform a detailed stability study, a previous knowledge of the dynamic behavior of each SC-resistor is necessary. That behavior is essentially determined by two different factors. First, by the reactive parasitics associated with the active components in Figs. 9 and 11. Second, by the discrete parasitics introduced by the numerical integration algorithm associated with each discretized model. The overall behaviors of both kinds of parasitics are quite different and it is appropriate to consider them separately. On the other hand, since a general treatment is rather cumbersome, we will only show the most important dynamic effects via a few examples.

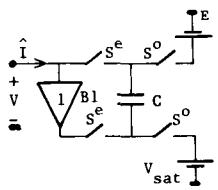
4.1. Continuous Parasitics

Let us consider the circuit in Fig. 18, where we have represented the interconnection of a generic PL basic element to a one-port network, N, containing only linear BE SC-resistors and dc sources. Furthermore, N is represented by its Thevenin equivalent.

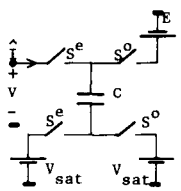
If we assume that: 1) every element in Fig. 18 is ideal and; 2) the system has reached the steady state, we may



(a)

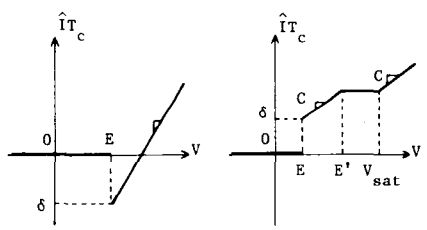


(b)



(c)

Fig. 15. (a)–(c) Equivalent circuits showing the different possibilities for out-of-range operation for a FE-PCSC: (a) Buffer B1 in Fig. 11(a) saturated. (b) Buffer B2 in Fig. 11(a) saturated. (c) Buffers B1 and B2 in Fig. 11(a) saturated.



(a) (b)

Fig. 16. Global characteristics for a FE–PCSC including out-of-range operation for different design values: (a) $V_{sat} < E' = V_{sat} - \delta/C$. (b) $V_{sat} > E'$.

obtain the following time representation for the current i flowing through the SC-resistor during the even clock phase:

$$i(t) = C \sum_{-\infty}^{\infty} \{1+\operatorname{sgn}(V-E)\}\{V(1-a)-\hat{V}\}\delta(t-nT_c). \tag{20}$$

Thus $i(t)$ is an ideal pulse train of period T_c, as shown by the discontinuous trace in Fig. 19.

However, the actual implementation of the PL SC-resistor in Fig. 18 is influenced by several factors which affect our previous assumptions. On one hand, there is a delay, T_D, associated with the physical realization of the threshold function (comparator delay in Figs. 9 and 11). On the other hand, there is a transient behavior due to the combined

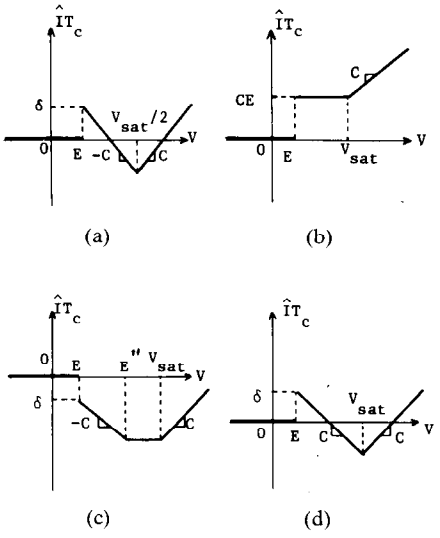


Fig. 17. (a) Global characteristics for a BE–NCSC. (b) Global characteristics for the step charge source. (c),(d) Global characteristics for the FE–NCSC: (c) $E'' = (V_{sat} + \delta/C) < V_{sat}$. (d) $E'' > V_{sat}$.

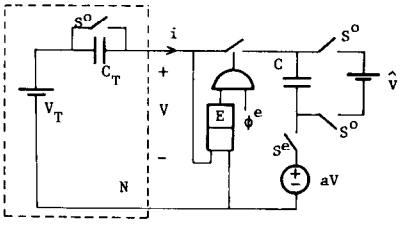


Fig. 18. SC voltage divider used for illustrating instability troubles in nonlinear SC networks due to continuous parasitics.

action of the parasitics associated with the controlled-sources and of the ON resistance of the analog switches. Hence, expression (20) must be modified to include these effects; namely,

$$i(t) = C \sum_{-\infty}^{\infty} \{1 + \operatorname{sgn}(V - E)\}\{V(1-a) - \hat{V}\} \cdot \delta(t - T_D - nT_c) * p(t) \quad (21)$$

where $*$ denotes the convolution operation and $p(t)$ denotes the second effect discussed above. Continuous tracing in Fig. 19 shows a pictorial representation of the actual value for $i(t)$. It must be pointed out that both T_D and $p(t)$ may cause instability problems and must be considered separately.

Let us focus our attention on the influence of $p(t)$. Since in a purely SC network the variables (voltage and charge) are defined only when no current flows inside the network, it should be obvious that a necessary and sufficient condition for stability is that the transient response reaches zero. Of course, it is advantageous to obtain such a condition as a function of the circuit element values. This is illustrated for the circuit in Fig. 18 via the circuit in Fig. 20. There we have represented the even topology of Fig. 18 for $V > E$, assuming that the PL SC-resistor is a BE–NCSC with $\delta = E = 0$. Moreover, we will disregard the ON resistance of the switches and consider the controlled source implemented by an op amp. Then, the controlled source transfer function is

$$a(s) = \frac{w_t}{s + \frac{w_t}{2}} \quad (22)$$

where w_t is the gain–bandwidth product of the op amp.

Routine calculations on the circuit in Fig. 20 gives the following characteristic frequency of the network:

$$w_o = \frac{w_t}{2} \frac{C_T - C}{C_T + C}. \quad (23)$$

Clearly, this circuit is stable only if $C_T > C$. In a similar way, stability conditions may be derived for each basic building block [14]. Table II is intended as a summary of such conditions for one-segment PL SC-resistors.

Now, let us concentrate on determining the influence of T_D. We will consider the example shown in Fig. 21, where the network N is connected to a 3-segment PL SC-resistor. Fig. 22(a) plots V versus V_T as is ideally implemented by the circuit in Fig. 21 (full trace). Suppose that an input value V_{T1}, as shown in Fig. 22(a), is applied during the clock phase nT_c. Point I on the characteristic corresponds to that excitation. Evidently, since I lies between the thresholds, only S_1^e must be closed, with S_2^e remaining open during the whole clock interval. However, this is not what really happens. Taking into account the delay (T_D), S_1^e and S_2^e will remain open until the instant $nT_c + T_D$. Hence, during that time the voltage V corresponds to point A in Fig. 22(a). Since this voltage is higher than both thresholds (E_1 and E_2) it will cause a circuit malfunction, since both switches will be initially closed when $t > nT_c + T_D$. The consequence of this malfunctioning is that the system tends to reach point B instead of point I as its final state. Fig. 22(b) shows the empirical V–V_T characteristics obtained for the network in Fig. 22(a) by taking

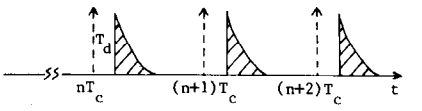


Fig. 19. Discontinuous trace: ideal current waveform flowing through the network N in Fig. 18; continuous trace: actual current waveform.

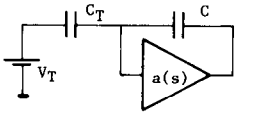


Fig. 20. Even phase equivalent circuit for a BE–NCSC connected across a linear BE SC-resistor.

TABLE II
STABILITY CONDITIONS DUE TO THE INFLUENCE OF REACTIVE PARASITICS INTO THE PERFORMANCE OF THE BASIC PL SC-RESISTORS

	NCSC	PCSC
BE	$C_T > C$	No restriction
FE	$C_T > 0$	$C_T > 0$

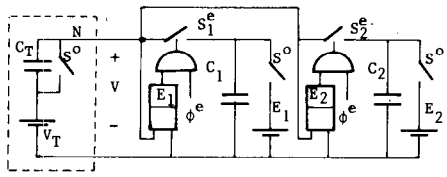
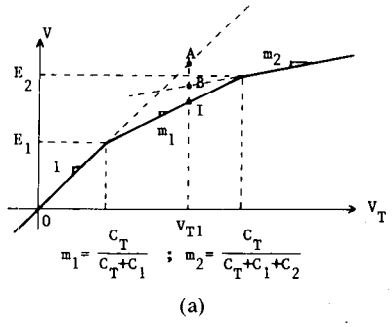
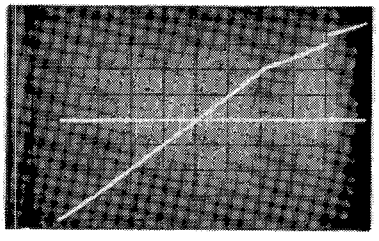


Fig. 21. SC voltage divider used for illustrating the instability troubles in nonlinear SC networks due to a delay in the threshold function.



(a)



(b)

Fig. 22. (a) TC characteristics for the network in Fig. 21. (b) Experimental TC plots for the network in Fig. 21 with $E_1 = 2$ V, $E_2 = 4$ V, $C_T = C_1 = C_2 = 1$ nF; horizontal signal; V_T, scale: 1 V/dv; vertical signal; V, scale: 1 V/dv.

$E_1 = 2$ V, $E_2 = 4$ V, and $C_T = C_1 = C_2 = 1$ nF. On this oscillogram it is seen that the actual breakpoints are displaced with respect to the ideal ones (to be located at $V_T = 2$ V and 6 V, respectively). Moreover, a discontinuous jump appears in the characteristics for $V_T = 4v$. These results are in agreement with the theoretical predictions and illustrate the instability troubles due to T_D.

Although our phenomenological treatment makes evident the effects that one may expect from the influence of T_D, it is very hard to derive closed form conditions related to the circuit element values for each PL SC-resistor. In any case, for our purposes here, it is enough to conclude that T_D gives rise to malfunctioning unless we excite the SC-resistor by a voltage source connected between its terminals. In fact, the experimental result detailed in Section III was obtained upon fulfilling this condition.

Apparently, the constraint imposed above in order to avoid malfunctioning is too restrictive and may render our design approach impractical. Fortunately, this constraint may be removed by including a memory device that makes the threshold function "remember" during a cycle what its state was during the preceding one. Fig. 23 depicts a practical way to do that, including the required timing.

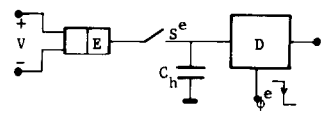


Fig. 23. Example of TCS with memory.

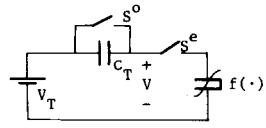


Fig. 24. SC voltage divider used for illustrating the instability troubles in nonlinear SC networks due to discrete parasitics.

TABLE III
STABILITY CONDITIONS DUE TO THE INFLUENCE OF DISCRETE PARASITICS

	NCSC	PCSC
BE	No restriction	No restriction
FE	$C_T > C$	$C_T > C$

4.2. Discrete Parasitics

As a result of the numerical algorithm associated with the chosen discretized model, there are instability problems that do not depend on a particular implementation but rather on the general properties of the algorithm. In order to investigate such problems, let us consider the simple circuit in Fig. 24. When the nonlinear SC-resistor is BE, we get for that circuit

$$V(n) = V_T - \frac{f\{V(n)\}}{C_T} \tag{24}$$

and when the SC-resistor is FE, we obtain

$$V(n) = V_T - \frac{f\{V(n-1)\}}{C_T}. \tag{25}$$

Clearly, expression (24) is algebraic and does not present instability troubles. However, such troubles may arise in (25), making an analysis of its locally asymptotic stability worthwhile. To perform an adequate study, we may begin by analyzing the behaviour of that equation linearized around an equilibrium point, V_Q

$$V(n) = V_T - \frac{1}{C_T}\left.\frac{df}{dv}\right|_{V_Q} V(n-1). \tag{26}$$

Taking the z-transform of that expression, the result is

$$V(z) = \frac{zV_T}{z + \frac{1}{C_T}\left.\frac{df}{dv}\right|_{V_Q}}. \tag{27}$$

In order for the equilibrium point to be stable, the associated "pole" must be inside the unit circle; namely,

$$-1 < \frac{1}{C_T}\left.\frac{df}{dv}\right|_{V_Q} < 1. \tag{28}$$

This condition is usually simple to check because we only need to evaluate the slope at the equilibrium point.

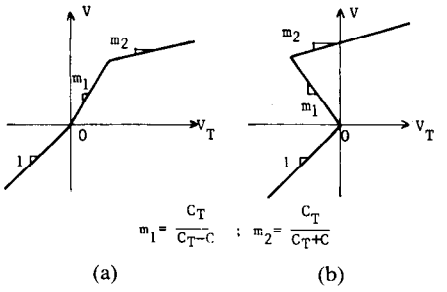


Fig. 25. TC characteristics for the network in Fig. 24 assuming that the nonlinear SC-resistor is a NCSC with slope C. (a) $C < C_T$. (b) $C > C_T$.

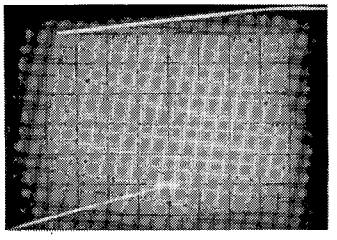


Fig. 26. Experimental verification of the hysteretic behaviour predicted in Fig. 25(b); horizontal signal; V_T, scale: 0.25 V/dv; vertical signal; V, scale: 1 V/dv.

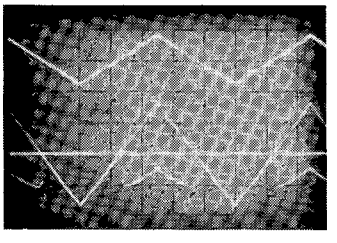


Fig. 27. Experimental verification of the oscillatory behaviour for the network in Fig. 24; horizontal scale: 500 μs/dv; top vertical signal; V_T, scale: 2 V/dv; bottom vertical signal; V, scale: 1 V/dv.

For instance, when an FE–NCSC is concerned, this slope has a value C; then, the stability condition may be expressed as $C_T > C$. Table III gives this condition for each one-segment PL SC-resistor.

4.3. Practical Results

From the preceding discussions we can make two important conclusions:

1) The influence of T_D is very restrictive, but may be eliminated by a small change in the implementation of each basic SC component.
2) For each basic building block we may derive explicit stability conditions relating the element values.

However, it is worthwhile to know not only the limits of stable operation but the kind of instability mechanisms which appear in practice. Furthermore, it is interesting to relate these mechanisms to the global static characteristics. We will try to illustrate such a relationship here assuming practical elements that incorporate the memory device from Fig. 23.

Let us consider again the general situation depicted in Fig. 24. Let us further assume that the PL SC-resistor is an NCSC with $E = \delta = 0$. Then two different situations arise

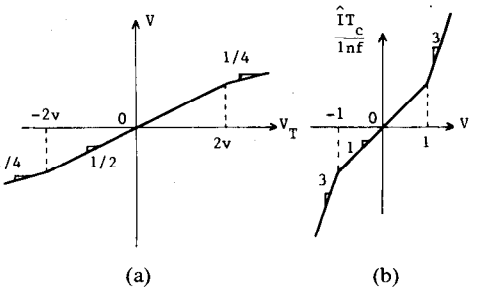


Fig. 28. (a) TC characteristics to be implemented via the SC voltage divider in Fig. 24. (b) SC-resistor required to synthesize the TC in Fig. 28(a).

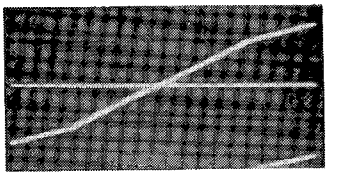


Fig. 29. Experimental TC plot obtained by using the SC-resistor in Fig. 28(b) into the voltage divider in Fig. 24 with $C_T = 1$ nF; horizontal signal; V_T, scale: 1 V/dv; vertical signal; V, scale: 1 V/dv.

for $C_T > 0$, which are plotted in Fig. 25. When $C_T > C$ (Fig. 25(a)), the characteristic is single valued and the stability condition implied from Tables II and III is fulfilled. However, when $C_T < C$ (Fig. 25(b)), the characteristic is a multiple-valued function of V_T and the predicted instability is translated into a hysteretic behavior. Fig. 26 presents an experimental plot showing the predicted hysteresis for a case in which $C = 1.2$ nF and $C_T = 1$ nF. Also, from Tables II and III, we may infer that for PCSC there are stability problems only if FE is used. However, the instability mechanism cannot be hysteretic, since the global characteristic is always single-valued. Fig. 27 shows the actual instability mechanism for this case. It was obtained from the circuit in Fig. 24 when the PL SC-resistor was a FE–PCSC with $E = \delta = 0$ and by taking $C = 1.2$ nF, $C_T = 1$ nF. On this oscillogram we note the existence of oscillations for $V > 0$.

V. Synthesis of PL Voltage TC's

It is a routine matter to use the PL SC-resistor to implement PL TC plots. In fact, as it was shown in Section II, a general method may be devised by substituting each resistor in a continuous prototype by an associated SC-resistor. Thus, we may use a SC voltage divider counterpart [15], as illustrated by the following example. Let us design the TC plot in Fig. 28(a) by using the circuit from Fig. 24. The corresponding PL SC-resistor is seen in Fig. 28(b). After synthesizing such a resistor following the techniques developed in Section III, we got the experimental TC plot shown in Fig. 29. The nonlinear component was designed using the BE realization.

An alternative to the SC voltage divider is to resort to some kind of transformation circuits. The basic scheme can be seen in Fig. 30. It represents an SC implementation of a DP–TC converter [11]. An arbitrary PL SC-resistor described by $\hat{I} = f(V)/T_c$ is connected to the negative input

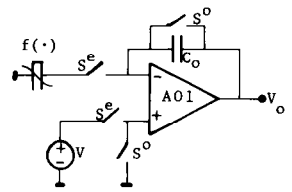
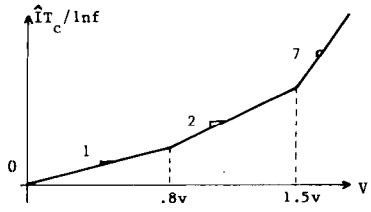
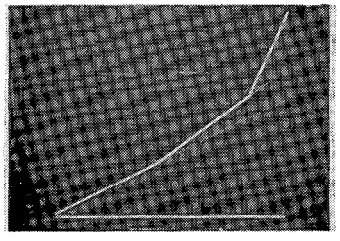


Fig. 30. SC-resistor to TC transformer.



(a)



(b)

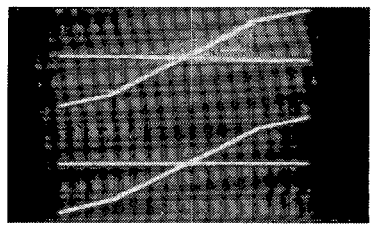
Fig. 31. (a) SC-resistor characteristic to be transformed using the network in Fig. 30. (b) Experimental TC plot obtained with $C_o = 1$ nF; horizontal signal; V, scale: 0.25 V/dv; vertical signal; V_o, scale: 1 V/dv.

of A01. Then, we obtain the following input/output function between V and V_o:

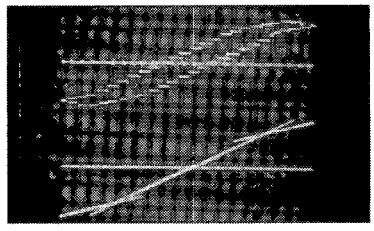
$$V_o = V + \frac{f(V)}{C_o} \tag{29}$$

This last expression may be used as a design equation to calculate the function $f(\cdot)$ required for realizing a prescribed TC plot. Fig. 31(b) shows the use of the circuit in Fig. 30. It depicts the experimental TC plot obtained after transforming the DP plot shown in Fig. 31(a). This latter plot has been implemented using BE components.

An important point to be considered here is the maximum bandwidth of the input signals. This bandwidth is constrained by the discrete parasitics we have considered above and by the maximum clock frequency allowed. In turn, the maximum clock frequency is limited by the nonideal behavior of the active components, mainly by the slew-rate of the opamps. For the actual circuit we have built and tested, we have attained a maximum clock frequency of 85 kHz. For this frequency, the allowed bandwidth is between 500 Hz and 5 kHz, depending on the type of element under consideration (either BE or FE). Whether or not this limits the usability of these circuits in a practical application will depend on the application itself and cannot be considered in a general context. However, we can illustrate how this frequency limitation affects a transfer characteristic using Fig. 32(a) and (b). These figures are oscillograms showing a transfer characteristic for



(a)



(b)

Fig. 32. Experimental TC plots for a sinusoidal input signal and differents frequencies. (a) frequency = 500 Hz.; (b) frequency = 5 kHz; horizontal signal; input, scale: 1 V/dv; top vertical signal; output using FE components, scale: 1 V/dv; bottom vertical signal: output using BE components, scale: 1 V/dv.

an input frequency of 500 Hz and 5 kHz, respectively. In both oscillograms the upper trace corresponds to the use of FE elements and the bottom trace corresponds to BE elements. The clock frequency was 83 kHz. It should be clear from these figures that the frequency performance of BE SC-resistors is superior.

VI. Modeling of Continuous Resistors

As it was seen in Section II, a continuous resistor may be designed using an SC transfer characteristic connected to a DT-converter [11]. The present Section will discuss the dynamic performance of that design technique. In order to obtain a significant model in the frequency domain, we will limit ourselves to considering the realization of a continuous linear resistor. The results obtained for the linear case may be extended to the qualitative analysis of more general nonlinear resistors. In any case, they illustrate the main dynamic effects which appear as a consequence of the implementation technique.

Fig. 33 shows the basic circuit diagram of a continuous resistor using SC techniques. The block labeled TC is a transfer characteristic implemented with SC-resistors following the methods discussed in Section V. The summer may be implemented using either R-active or C-active [16] circuit techniques. Since the summer weights are unity, the dynamic response of this element may be assumed to be negligible when compared with that corresponding to the sample-hold (S/H) block. Therefore, the dynamic behavior of the resistor in Fig. 33 is mainly influenced by three factors: 1) the sample-hold frequency response; 2) the processing delay introduced by the block TC; and 3) the settling time prior to reaching the steady state at the TC output. Each factor may be independently modeled. Thus for the S/H influence, the controlled port variable may be

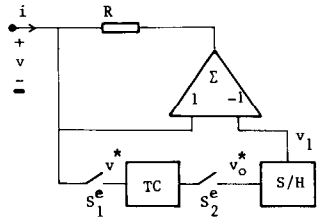


Fig. 33. Circuit diagram for a SC mutator.

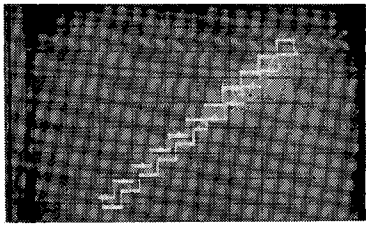


Fig. 34. Experimental result showing the hysteresis in the DP plot measured across the terminals of the mutator in Fig. 33; horizontal signal; $v(t)$, scale: 1 V/dv; vertical signal; $i(t)$, scale: 2 mA/dv.

represented by

$$I(s)=\frac{1}{R}\,\frac{1-\exp(-sT_c)}{s}\,V_o^*(s) \tag{30}$$

where $I(s)$ and $V_o^*(s)$ are, respectively, the Laplace transforms of $i(t)$ and $v_o^*(t)$.

On the other hand, the processing delay in TC may be represented by using the z-transform technique to obtain

$$V_o^*(z)=H(z)V^*(z). \tag{31}$$

Finally, the third effect corresponds to the fact that the TC output sample, $V_o^*(nT_c)$, is not available until after the steady state is reached. We may model it by a time delay, T_s, with reference to nT_c. Hence, we may write

$$V_o^*(s)=\exp(-sT_s)\sum_{-\infty}^{\infty}V_o^*(nT_c)\exp(-snT_c). \tag{32}$$

Combining all of these factors, we obtain finally an expression for the current at the external port

$$I(s)=\frac{1}{R}\exp(-sT_s)H(z)\frac{1-\exp(-sT_c)}{sT_c}\sum_{-\infty}^{\infty}V(s-nw_c) \tag{33}$$

where $z=\exp(-sT_c)$.

It is worth specifying (33) in case all of the components used in implementing the TC are of the BE type. So $H(z)=k$ and the result is

$$I(s)=\frac{k}{R}\exp(-sT_s)\frac{1-\exp(-sT_c)}{sT_c}\sum_{-\infty}^{\infty}V(s-nw_c). \tag{34}$$

Taking $s=jw$, we may define an equivalent admittance at the fundamental frequency

$$Y(w)=\frac{I(w)}{V(w)}=\frac{k}{R}\,\frac{1-\exp(-jwT_c)}{jwT_c}\exp(-jwT_s). \tag{35}$$

Fow low frequency ($wT_c\ll 1$), (35) simplifies to

$$Y(w)\simeq\frac{k}{R}\{1-jw(T_c+T_s)\}. \tag{36}$$

The preceding equation may be represented by a conductance in parallel with a negative capacitor. This suggests that we can interconnect a positive capacitor of value $k(T_c+T_s)/R$ across the resistor terminals to compensate the parasitic dynamic effects introduced by our design technique. Also, the phase error may be evaluated as

$$\phi\simeq -w(T_c+T_s). \tag{37}$$

This last expression may be considered as a tool for estimating the maximum input frequency.

If all of the components used in the TC block are FE, the evaluation of the equivalent admittance depends on the topology used. In the least favorable situation, it may be calculated as

$$Y(w)=\frac{k}{R}\,\frac{1-\exp(-jwT_c)}{jwT_c}\exp\{-jw(T_c+T_s)\} \tag{38}$$

which, for low frequency, can be simplified as follows:

$$Y(w)\simeq\frac{k}{R}\{1-jw(2T_c+T_s)\}. \tag{39}$$

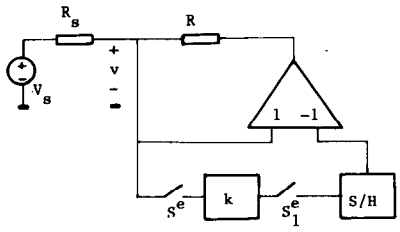
Fig. 34 plots an oscillogram showing the hysteresis in the characteristics of a linear resistor due to the phase shift introduced by the circuit of Fig. 33. We have used $k=2$, $R=1$ kΩ, and $f_c=19533$ Hz. The excitation signal was a triangular voltage waveform of f = 900 Hz. The oscillogram in Fig. 35(b) represents the instability behavior observed in the circuit of Fig. 35(a) for $R_s=R=1$ kΩ and $k=2$. Correspondingly, Fig. 35(c) shows the response of the same circuit using a compensating positive capacitor with a value of 56 nF. As it can be seen, the oscillations have been completely eliminated, which confirms the theoretical results explained above.

VII. Conclusions

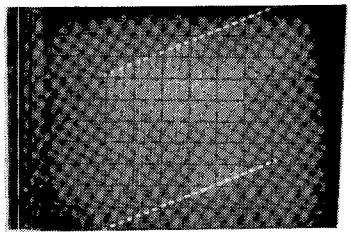
Design methods have been proposed for implementing nonlinear networks employing elements well suited for integrated circuit realization. The basic component (the SC-resistor) is an extension of the switched-capacitor used at present in linear filters. We have shown that SC-resistors allow for the design of either discrete-time or continuous-time resistive networks. In particular, components other than resistors may also be synthesized with only small changes in the mutator considered in Sections II and VI. Then, the technique can be extended to networks containing nonlinear capacitors, inductors, and higher order elements [18].

A detailed modeling of the proposed building block components as well as experimental data are included. They provide reasonable agreements between theoretical predictions and practical results.

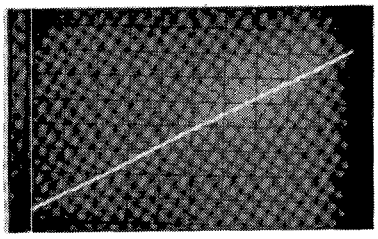
An interesting point that warrants attention is the influence of parasitic capacitances. The most important re-



(a)



(b)



(c)

Fig. 35. (a) Continuous voltage divider used for illustrating instability troubles associated with a SC mutator. (b) Experimental oscillatory behavior for the network in Fig. 34(a); horizontal signal; V_s, scale: 1 V/dv; vertical signal; V, scale: 1 V/dv. (c) Experimental TC plot obtained using a compensating capacitor for eliminating the oscillations observed in Fig. 34(b); horizontal signal; V_s, scale: 1 V/dv; vertical signal; V, scale: 0.5 V/dv.

sult is that each of the proposed circuits has been designed to be insensitive to the bottom stray capacitances. It can be seen from Figs. 9 and 11 that the terminal of each capacitor denoted by "b" is always connected to a voltage source or to the virtual ground.

APPENDIX A

All the reference voltages required in Figs. 9 and 11 can be derived from a single dc source by using appropriate SC gain stages. This is illustrated in Fig. 36 where we have shown the method for obtaining both a positive and a negative voltage. Notice further that both reference outputs in the previous figure are defined only during the even clock phase. In a similar way we can also obtain a reference defined during the odd phase. The corresponding circuits for the latter case can be obtained directly from Fig. 36 by changing the phasing of the different switches in that figure.

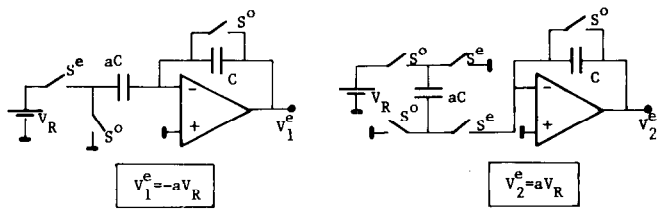


Fig. 36. SC voltage amplifiers.

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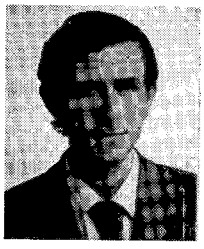

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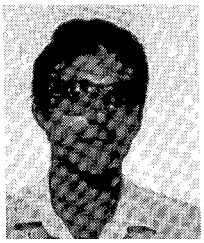

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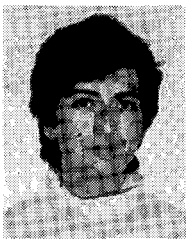

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