where

$$
\begin{equation*}
P=\operatorname{block} \text { diagonal }\left(I_{1}, I_{2}, \cdots, I_{i-1}, P_{i}, I_{i+1}, \cdots, I_{p}\right) \tag{12}
\end{equation*}
$$

where $I_{k}$ is $k \times k$ identity matrix, and $k$ is the dimension of component $\Sigma_{k}$.

Using the component connection approach, a model for the interconnected system $\Sigma$ is described with

$$
\begin{align*}
& \dot{z}=(F+G L H) z+G M u  \tag{13a}\\
& y=H z \tag{13b}
\end{align*}
$$

where

$$
\begin{equation*}
F=\operatorname{block} \text { diagonal }\left(A_{1}, A_{2}, \cdots, A_{i-1}, F_{i}, A_{i+1}, \cdots, A_{p}\right) \tag{13c}
\end{equation*}
$$

$G=$ block diagonal $\left(B_{1}, B_{2}, \cdots, B_{i-1}, G_{i}, B_{l+1}, \cdots, B_{p}\right)$

$$
\begin{equation*}
H=\text { block diagonal }\left(C_{1}, C_{2}, \cdots, C_{i-1}, H_{i}, C_{i+1}, \cdots, C_{p}\right) \tag{13d}
\end{equation*}
$$

Equations (3c), (10c), (12), and (13c) imply

$$
\begin{equation*}
F P=P A \tag{14a}
\end{equation*}
$$

Equations (3d), (3e), (10d), (10e), (12), and (13d) imply

$$
\begin{equation*}
(G L H) P=P B L C \tag{14b}
\end{equation*}
$$

Therefore, (14a) and (14b) imply

$$
\begin{equation*}
(F+G L H) P=P(A+B L C) \tag{15a}
\end{equation*}
$$

Similarly

$$
\begin{align*}
G & =P B  \tag{15b}\\
H P & =C . \tag{15c}
\end{align*}
$$

b) Necessity: The condition stated in the theorem results from the definition of the component connection model. In this framework the state vector of the composite system is obtained by stacking the state vectors of the individual components.
Remark: If ( 1 b ) is modified to

$$
y_{i}=C_{i} x_{i}+D_{i} v_{i}
$$

then, $(8 \mathrm{~b})$ needs to be modified to

$$
y=H z+. J u
$$

and conditions (9) will include

$$
\begin{equation*}
J=D \tag{9d}
\end{equation*}
$$

Consequently, the theorem still holds and the composite system model is described by [6]

$$
\begin{aligned}
& \dot{x}=(A+B Q L C) x+B Q M u \\
& y=(I+D Q L) C x+D Q M u
\end{aligned}
$$

where

$$
\begin{aligned}
& D=\text { block diagonal }\left(D_{1}, D_{2}, \cdots, D_{p}\right) \\
& Q=(I-L D)^{-1}
\end{aligned}
$$

The aggregate model for the composite system is described by

$$
\begin{aligned}
& \dot{z}=(F+G Q L H) z+G Q M u \\
& y=(I+D Q L) H z+D Q M u
\end{aligned}
$$

where the aggregate model state variables $z$ are as defined above.

## V. CONClusion

Whenever dealing with interconnected large-scale systems the size of the system becomes an issue. Model reduction techniques are used to allcviate these difficulties. Most of the techniques are applied to the linearized model of the composite system model. In this paper, it is shown that in the component connection model framework the composite system is aggregable if and only if at least one of its components is aggregable. Because of the relatively small size of the individual components, it is easier to aggregate the component model rather than the composite system model. The important consequence of this result is that when dealing with interconnected large scale systems in the component connection model framework one does not need to aggregate the large-scale composite system but rather can consider the aggregation of each, relatively smaller scale component, independently.

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## Chaos in a Switched-Capacitor Circuit

## ANGEL B. RODRIGUEZ-VAZQUEZ, JOSE L. HUERTAS, and LEON O. CHUA


#### Abstract

We report chaotic phenomena observed from a simple nonlinear switched-capacitor circuit. The experimentally measured bifurcation tree diagram reveals a period-doubling route to chaos. This circuit is described by a first-order discrete equation which can be transformed into the logistic map whose chaotic dynamics is well known.


Several nonlinear circuits which exhibit various types of chaotic phenomena have been reported recently [1]-[5]. Our objective in this letter is to report an experimental result showing the ubiquitous chaotic phenomena can also occur in a switchedcapacitor circuit. Since switched-capacitor circuits are important in VLSI technology, any potential anomaly or failure mechanisms

[^0]

Fig. 1. A nonlinear switched-capacitor circuit and its associated timing diagram.
due to the onset of chaos should be fully analyzed. This chaotic circuit is also of circuit-theoretic interest because its dynamic equation is equivalent to the well-known logistic map [6] whose chaotic dynamics have been extensively studied and is now well understood. Since the logistic map is the simplest chaotic polynomial discrete map, the chaotic circuit to be described below is the simplest chaotic circuit described by a first-order discrete map.

Consider the switched-capacitor circuit in Fig. 1(a): it is made of a battery $V_{s}$, a linear capacitor $C_{s}$, a nonlinear switched-capacitor component [7], [8], and three analog switches. The state (on or off) of the switches is controlled by a standard two-phase clock defined by the timing diagram shown in Fig. 1(b). The switches labeled $S^{e}$ (resp., $S^{o}$ ) turn on in synchronization with the rising edge of the clock signal $\phi^{e}$ (resp., $\phi^{o}$ ).

The nonlinear switched-capacitor component-henceforth called an FESC (forward Euler switched capacitor) resistor-is defined by

$$
\begin{equation*}
Q_{n}-Q_{n-1}=k V_{n-1}^{2} \triangleq \Delta Q_{n} \tag{1}
\end{equation*}
$$

where $\Delta Q_{n}$ is the net charge flowing into the FESC resistor during the $n$th clock period, $V_{n-1}$ is the voltage sampled across the FESC resistor during the $(n-1)$ th period, and $K$ is an arbitrary positive constant.

We have built the circuit in Fig. 1(a) with $C_{s}=1 \mathrm{nF}$ and $k=0.5 \mathrm{nF} / \mathrm{V}$ using off-the-shelf components and observed the steady-state voltage waveform samples $V$ for different values of the battery voltage $V_{s .}$. Contrary to our intuitive expectation for a single-valued relationship between $V$ and $V_{s}$, we found the relationship to be multiple-valued over some ranges of the "parameter" $V_{s}$, and undefined i.e., chaotic, for other ranges. This observation is summarized by the bifurcation tree measured experimentally from this circuit. The familiar cascades preceding the chaotic region implies a period-doubling route to chaos [6].

To derive a recursive relationship for $V_{n}$, we note that the net charge $\Delta Q_{n+1}$ flowing into the FESC resistor during the $(n+1)$ th clock period must be equal to the net charge flowing out of the linear capacitor $C_{s}$ (charge conservation principle), and hence:

$$
\begin{equation*}
V_{n+1}=V_{s}-\frac{k}{C_{s}} V_{n}^{2} . \tag{2}
\end{equation*}
$$

We can transform (2) into several more familiar cquivalent forms by defining

$$
\begin{equation*}
X_{n+1}=a V_{n+1}+b \tag{3}
\end{equation*}
$$

If we choose $a=1 / V_{s}$ and $b=0$, we would obtain

$$
\begin{equation*}
X_{n+1}=1-\lambda X_{n}^{2} \tag{4}
\end{equation*}
$$



Fig. 2. Bifurcation tree.


Fig. 3. Off-the-shelf realization of the FESC resistor in Fig. 1(a).
where

$$
\lambda=k V_{5} / C_{s}
$$

If we choose

$$
a=\frac{1}{4 V_{s}}\left(-1 \pm \sqrt{1+4 k \frac{V_{s}}{C_{s}}}\right)
$$

and $b=\frac{1}{2}$, we would obtain the well-known logistic map

$$
\begin{equation*}
X_{n+1}=4 \lambda X_{n}\left(1-X_{n}\right) \tag{5}
\end{equation*}
$$

where

$$
\lambda \triangleq \frac{k}{4 a C_{s}} .
$$

Both equations, (3) and (5) have been intensively studied [6] and their global qualitative behaviors are now well classified and understood. Consequently, Fig. 1(a) represents the first real physical circuit whose chaotic dynamics can be completely analyzed.
For readers interested in repeating our experiments, the FESC resistor in Fig. 1(a) can be realized by the circuit shown in Fig. 3.

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## Nodal Voltage Simulation of Active RC Networks

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Abstract - It is shown that the floating nodes present in active $R C$ networks can be eliminated by nodal voltage simulation, leading to new active $R C$ networks. The new active $R C$ networks thus generated can be easily used to realize stray-insensitive $S C$ networks. Equivalence of certain active $R C$ topologies, resulting from application of this method, is also demonstrated.

## I. Introduction

The theory and design techniques of active $R C$ filters are considerably mature at present. Integrated circuit implementation necessitated circuits using grounded capacitors, to eliminate the effect of bottom-plate parasitic capacitances [1]. With the advent of switched-capacitor technique, it has become necessary to eliminate the effect of parasitic capacitances altogether, since predistortion as well as trimming are unattractive [2]. It is natural, therefore, to attempt to derive stray-insensitive $S C$ topologies from active $R C$ filters using grounded capacitors. Three techniques viz., parasitic compensation [3], [4], nodal voltage simulation [5], [6], and stray-capacitance eliminating transformations [7] have been reported in the literature. In this letter, we examine the second approach in detail. It may be noted that this approach has been used in deriving bilinear SC ladder filters from doubly terminated $L C$ filters [8]. Other variations such as nodal transfer function simulation [9], [10] are also available in the literature.

## II. Nodal Voltage Simulation Method

We study the nodal voltage simulation technique with reference to specific active $R C$ networks, in what follows, in order to demonstrate its utility.

## A. Application to Multiple Feedback Type Single-Amplifier LowPass Filters

Consider the multiple-feedback active $R C$ low-pass filter of Fig. 1(a). The internal node $x$ in this network is described by KCL as

$$
\begin{equation*}
\frac{V_{i}}{R_{1}}+\frac{V_{0}}{R_{3}}=V_{x}\left[\frac{1}{R_{1}}+\frac{1}{R_{2}}+\frac{1}{R_{3}}+s C_{1}\right] \tag{1}
\end{equation*}
$$

It is easy to realize $V_{x}$ using OA's with grounded noninverting input as shown in Fig. 1(b), by the circuit within dotted lines. Augmenting this network by the remaining circuit consisting of

[^1]
(b)

Fig. 1. (a) Multiple feedback low-pass filter. (b) Active $R C$ network equivalent to Fig. 1(a).
$R_{2}, C_{2}$ and OA $A_{3}$ to realize $V_{0}$ from $V_{x}$, we obtain the network of Fig. 1(b), which interestingly, is the well-known Tow-Thomas biquad [11]. The availability of band-pass output at node $x$ and low-pass output at $V_{0}$ in the circuit of Fig. $1(a)$ is transferred to the network in Fig. l(b). Note that, both these circuits are based on inductance simulation [12], [13]. Further, we observe that the circuit of Fig. 1(a) is having damping due to resistors $R_{1}, R_{2}$, and $R_{3}$. This damping can be reduced by multiplying the effect of $R_{2}$ and $R_{3}$ through a negative resistance to ground at node $x$ [14]. The resulting active $R C$ filter is shown in Fig. 2(a). Proceeding in the same manner as in the case of Fig. 1(a), we obtain the equivalent $R C$ active filter of Fig. 2(b). The transfer function realized is given by

$$
\begin{equation*}
\frac{V_{0}}{V_{i}}=\frac{-1 / R_{1}}{s^{2} C_{1} C_{2} R_{4}+s C_{2} R_{4}\left(\frac{1}{R_{2}}-\frac{1}{R_{5}}\right)+\frac{1}{R_{3}}} \tag{2}
\end{equation*}
$$

Thus both low-pass and band-pass transfer functions are still available, while large $Q$ 's can be obtained through the use of nearly equal $R_{2}$ and $R_{5}$ values. The $Q$-sensitivities are thus large:

$$
S_{R_{5}}^{Q}=1+\frac{Q R_{3}}{R_{5}} \quad \text { and } \quad S_{R_{4}}^{Q}=1 \quad \frac{Q R_{3}}{R_{5}}
$$

Note that Fischer and Moschytz [15] used such a modification for Fleischer-Laker's biquad [16] for reducing the capacitance spread.

In applications where equal capacitor values are preferred in the circuit of Fig. 1(a), positive feedback can be applied [17]. This leads to the modification of the Tow-Thomas biquad, as shown in Fig. 3(a). The transfer function realized is

$$
\begin{equation*}
\frac{V_{0}}{V_{i}}=\frac{1 / R_{1}}{s^{2} C_{1} C_{2} R_{4}+s\left(\frac{C_{2} R_{4}}{R_{2}}-\frac{C_{1} R_{4}}{R_{5}}\right)+\left(\frac{1}{R_{3}}-\frac{R_{4}}{R_{2} R_{5}}\right)} \tag{3}
\end{equation*}
$$

Note, however, that the band-pass transfer function is not realizable at the outputs of the OA's $A_{1}$ and $A_{2}$. The design equations


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