The three resonant frequencies were specified close together. The resulting design had a large frequency range, 30–80kHz, over which resonant current had minimal phase difference with the inverter voltage and consequently the switching losses in the converter remained small. The component values were $L_s$ = 130μH, $C_s$ = 0.45μF, $C_p$ = 0.045μF, $L_L$ = 130μH, $C_L$ = 0.45μF and $R_L$ = 60Ω.

Fig. 2 shows how the characteristics of this design vary with frequency. The phase plot (Fig. 2*a*) remains near to zero for the range 30–80kHz, while the series-leg current (Fig. 2*b*) varies from 2.5 to 5.5A, indicating a significant power change in the circuit.

*Test results:* The design was constructed and tested in the half-bridge resonant converter. The load was a resistor and was placed on the output of a rectifier to remove the effect of load inductance. The DC supply voltage was 340V.

Fig. 3 shows the voltage across the bottom switch of the converter and the series-leg current at 50, 60, and 76kHz, frequencies between the resonant frequencies of the circuit. The circuit remains near to resonance throughout the whole frequency range, whilst the magnitude of the current and hence the power delivered to the load varies. The turn-off conditions are pseudo zero-current switching, owing to excitation of harmonics by the square-wave inverter voltage and operation of the circuit between the resonant frequencies of the circuit.

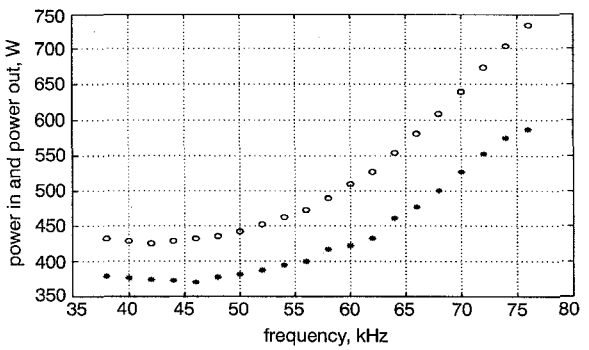


**Fig. 4** *Input power and output power of experiment converter from 35 to 80kHz*

○ DC power in
✳ power out

Fig. 4 shows the variation in the input and output power of the circuit with frequency. The efficiency of the converter varies from 88 to 80% over the frequency range 37–76kHz. The converter is most efficient at lower frequencies where both the circulating current and the output rectifier switching losses are smallest.

*Conclusion:* A series-parallel load-resonant converter with near to resonant operation over a wide frequency range has been demonstrated. The resonant circuit has been designed so that over this soft-switched frequency range there is a significant variation in the output power of the circuit.

The principle of the circuit will allow load-resonant circuits to be used in applications requiring continuously variable output power such as welding and laser power supplies. High frequency operation can be maintained, minimising the size and cost of the converter. Further enhancements to the design are being investigated to improve the efficiency of the circuit.


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# Robust high-accuracy high-speed continuous-time CMOS current comparator

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*Indexing terms: Current comparators, Analogue circuits, CMOS integrated circuits*

The authors present a CMOS current comparator which employs nonlinear negative feedback to obtain high-accuracy (down to 1.5pA) and high-speed for low input currents (8ns at 50nA). The new structure features a speed improvement of more than two orders of magnitude for a 1nA input current, when compared to the fastest reported to date.

*Introduction:* Current comparators consist of the cascade connection of a transimpedance amplifier to convert the input current into a voltage, and a voltage amplifier to provide gain [1]. The front-end transimpedance amplifier may be either capacitive (i.e. where there is no DC path from the input terminal of the device to ground), or resistive (where such a DC path exists). Analysis in [1] shows that capacitive-input comparators feature larger sensitivity, and faster operation for low currents, while resistive structures are faster for large currents. A hybrid CMOS structure that combines the advantages of resistive-input and capacitive-input comparators was proposed in [1, 2]. Such a structure, whose concept is depicted in Fig. 1*a*, uses nonlinear negative feedback to yield very large input impedance for low input currents and much lower input impedances for large currents. A 2μm CMOS prototype of this structure showed 10pAs sensitivity and virtually zero offset [1].

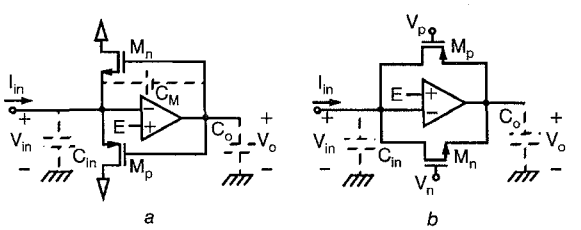


**Fig. 1** *Schematic diagrams of current switch comparator and current steering comparator*

*a* Current switch comparator
*b* Current steering comparator

Fig. 1*a* has, however, two major drawbacks limiting its application: its performance degrades significantly for low-voltage supplies; also its operation speed is constrained due to Miller effect on the MOST overlapping capacitors ($C_M$). It has recently been proposed that this second problem can be attenuated by reducing the output voltage excursions, through the addition of two voltage shifters to the basic comparator structure [3]. However, this yields a significant increase in the dependence on technological-parameter random fluctuations.

The CMOS current comparator presented in this Letter overcomes the two drawbacks of Fig. 1*a*, while keeping the operation virtually insensitive to these fluctuations. This is achieved by focusing on the improvement of the transient response without reducing the output voltage swing.

*Circuit behaviour:* The operation of Fig. 1*a* has already been described in [1]. Analysis of its transient response taking into account the capacitance $C_M$ obtains

$$\Delta V_{in} \simeq \frac{(C_o + C_M)}{C^2} I_{in} t \qquad \Delta V_o \simeq -\frac{C_M}{C^2} I_{in} t \quad (1)$$

where $C^2 = C_{in}C_o + C_{in}C_M + C_oC_M$. Note that the transient evolution of the output node is linear with $t$. This linear behaviour features a slow response for low input currents.

This problem is overcome by using the structure of Fig. 1*b*; first, we describe its DC operation. In the central point where:

$$V_{in} = V_o = E \qquad V_n \leq E + V_{tn} \qquad V_p \geq E - |V_{tp}| \quad (2)$$

transistors $M_n$ and $M_p$ are OFF, and the equivalent impedance at the input node is capacitive, hence yielding high resolution. As for Fig. 1*a*, positive (negative) input currents cause $V_{in}$ to increase (decrease) and $V_o$ to decrease (increase) driving $M_n$ ($M_p$) into the ON state, creating a negative feedback loop around the amplifier, thus obtaining resistive-input behaviour.

Consider now the transient response. Note that in the new structure the negative feedback mechanism is such that input and output nodes of the comparator are not directly coupled, thereby showing no Miller effect due to the overlapping capacitors. Then, analysis shows that the transient evolution is dominated by the capacitive-input behaviour, so that

$$\Delta V_{in} \simeq \frac{I_{in}}{C_{in}} t \qquad \Delta V_o \simeq -\frac{GB}{2} \frac{I_{in}}{C_{in}} t^2 \quad (3)$$

where $GB$ is the opamp gain-bandwidth product. It is seen that the transient evolution of the output node is no longer linear with $t$, as in previous structures [1 – 3], but quadratic. This feature makes the new comparator intrinsically faster for low currents without any reduction of the output swing being needed.

The response time of the new structure for an input current step from a negative overdrive level $-J$ up to a positive overdrive level $+J$ is calculated to obtain:

$$T_D \simeq \sqrt{\frac{2C_{in}}{GB} \frac{(V_p - V_n + V_{tn} + |V_{tp}|)}{J}} \quad (4)$$

This response time shows a speed improvement of more than two orders of magnitude for low currents ($J < 0.5$nA) when compared with the structure in Fig. 1*a*, even when the output voltage swing is reduced as in [3].

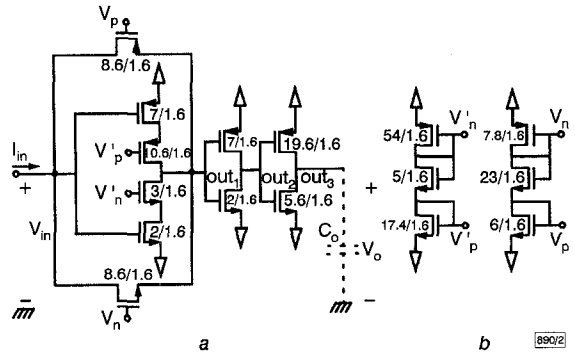


**Fig. 2** *New current comparator and biasing circuitry (in CMOS 1.6μm)*

*a* New current comparator
*b* Biasing circuitry

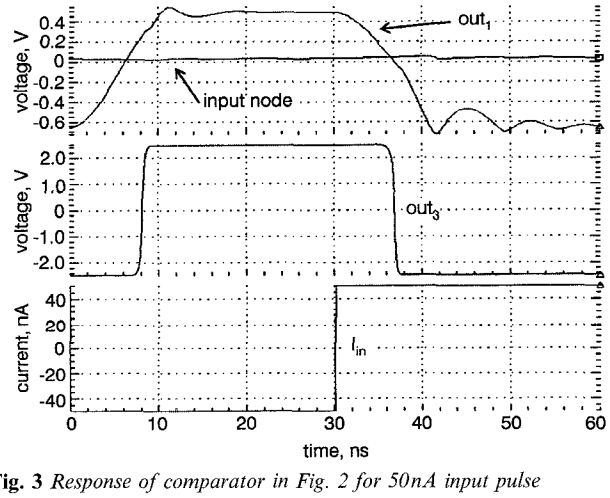


**Fig. 3** *Response of comparator in Fig. 2 for 50nA input pulse*

*Results:* Previous analysis has been validated by comparing the performance of the comparator in [3] with a prototype of the new comparator (see Fig. 2), both in a CMOS 1.6μm technology. All the evaluations are realised in transient mode, driving the comparator with a step signal (from a positive overdrive level $+J$ to a negative overdrive level $-J$) and covering a wide current range (1pA < $J$ < 100pA).

Fig. 3 illustrates the transient response of the new comparator for $J$ = 50nA, where the quadratic law evolution can be seen. Note that, in Fig. 2, cascode transistors are introduced to preclude direct capacitive coupling through the amplifier.

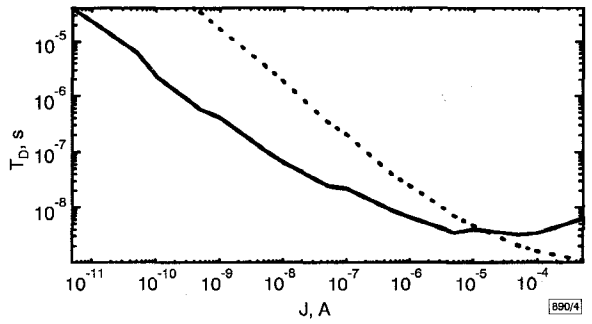


**Fig. 4** *Speed of new comparator and of that in [3] (both in CMOS 1.6μm)*

——— new comparator
– – – – comparator in [3]

Fig. 4 depicts the response times of the new structures and those in [3] for different input currents. These results, obtained by electrical simulation of the layout-extracted netlists, show that the new structure is much faster for low currents, and retains this speed advantage for currents up to 10μA.

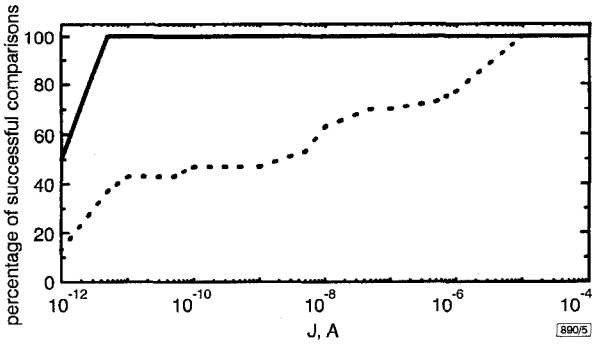


**Fig. 5** *Robustness of new comparator and that in [3]*

——— new comparator
– – – – comparator in [3]

Reducing voltage excursions at the amplifier output node, as applied in [3], improves comparison times. However, accuracy is degraded when technological-parameter random fluctuations are taken into account; a problem not present in the new structure. Fig. 5 summarises the results of statistical Monte Carlo simulations for different random samples of the MOST threshold voltage ($V_T$) and large-signal transconductance factor (β). Two current levels per decade have been considered. For each current level, 30 samples of $V_T$ and β have been generated, using the measured standard deviation for this technology, and a transient simulation has been performed for each sample. Fig. 5 shows the percentage of samples which perform correctly for each current level. It is seen that the new structure is much more robust than that in [3].

A second prototype of the comparator has been designed in a CMOS 0.8μm technology and features 23.7μs at 5pA, 11ns at 50nA, 1ns at 10μA with a 5V supply; 7.4μs at 5pA, 8ns at 50nA, 1ns at 10μA with a 3.3V supply. Also, after some modification of the amplifier and the biasing circuitry, the circuit can be made to operate down to a 1V supply.

To summarise, the comparator structure presented in this Letter shows superior timing performance and robustness compared to previous models, capable of operating accurately over very wide current ranges with a scaled-down voltage supply.

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# Single-switch AC/DC converter with power factor correction

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*Indexing terms: Power factor correction, AC-DC power converters*

A single-switch, one-stage power factor correction converter with output electrical isolation is proposed. To relieve the voltage spike caused by the leakage inductance of the power transformer, two bulk storage capacitors are used. The proposed converter has both a good power factor correction and excellent line and load regulation capabilities with an efficiency of 87%.

*Introduction:* Conventional single-phase power electronic circuits with a capacitive-rectifier input stage suffer from high total harmonic distortion (THD) and a poor power factor. A number of regulations and control techniques have been enacted recently to limit the harmonic content of the line current drawn by the electronic equipment by using high-frequency switching techniques to shape the input current waveform. This technique has been dominant in the design of power factor correction (PFC) circuits.

Several one-stage PFC circuits have been reported in open literature [1 – 3]. These circuits are especially attractive in low cost and low power applications, owing to the simplicity of their power stages and control circuits. However, one-stage PFC circuits have several drawbacks including: (i) owing to the unavoidable leakage inductance of their power transformers coupled with the improper sharing of the main power switch, high voltage spikes at the switching time are normally introduced. This results in a decreased overall converter efficiency; (ii) since the power switch performs both PFC and regulation tasks, their regulation capabilities are limited; (iii) under high current rating and low duty ratio operation, a high voltage stress normally results on the bulk capacitor, leading to an increased cost due to high capacitor voltage rating.

The new converter proposed in this Letter combines a boost circuit, a PFC circuit, and a forward circuit in one power stage. Two storage capacitors have been employed to relieve the voltage spike produced by the power transformer. The voltages across the storage capacitors are almost fixed at a lower level. Theoretical analysis and experimental results show that the converter has wide ranges of line regulation and load regulation capabilities and can be applied to a universal input.

*Basic circuit operation:* The basic circuit schematic diagram of the proposed single switch converter is shown in Fig. 1. It can be shown that in steady state the converter operates in four operation modes during one switching cycle. The converter key waveforms are shown in Fig. 2.

Mode 1 begins at $t = t_0$ when the power switch is turned ON. With diode $D_1$ conducting, energy transfers from the source to the choke inductor. Meanwhile, reverse biased by $2V_{Cs}$, diode $D_2$ is blocked. The forward transformer transfers energy from the storage capacitors to the load. During operation mode 2, the power switch is turned OFF and diode $D_2$ is turned ON. When the currents through inductors $L_1$ and $L_2$ decrease to zero, the operation mode enters mode 3.

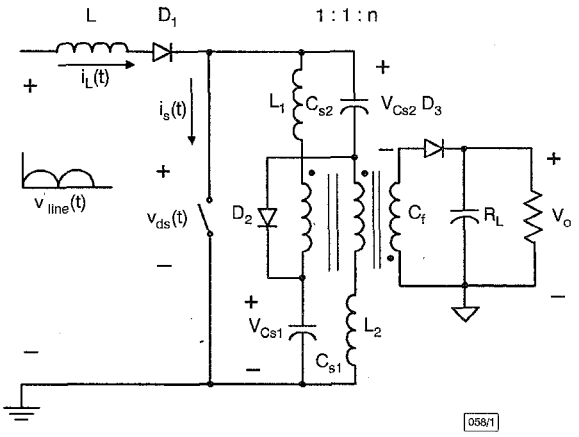


**Fig. 1** *Basic circuit schematic of proposed converter*

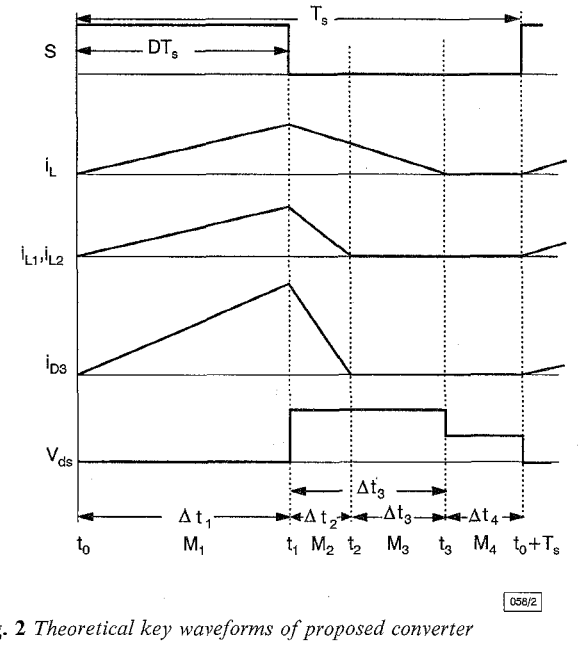


**Fig. 2** *Theoretical key waveforms of proposed converter*

In mode 3, the choke inductor current $i_L$ continues to decrease linearly. This mode ends when the choke inductor current reaches zero. Mode 4 is a free-wheeling stage of operation. When the power switch is turned ON again at $t = T_s + t_0$, the converter operation goes into the next cycle.

*Steady state analysis:* To simplify the steady state analysis, the following assumptions have been made:
(i) Capacitors $C_{S1}$ and $C_{S2}$ are designed to be large and equal;
(ii) All the switches (the transistor and the diodes) are ideal;
(iii) The forward transformer is ideal.
Using the above assumptions, we found that the voltages across capacitors $C_{s1}$ and $C_{s2}$ are given by

$$m = \frac{1}{2}\left[\frac{1}{n} + \frac{kn\tau_n}{2D_{ac}^2} + \sqrt{\left(\frac{1}{n} + \frac{kn\tau_n}{2D_{ac}^2}\right)^2 + \frac{2k\tau_n}{D_{ac}^2}}\right] \quad (1)$$

where $m \triangleq V_{Cs1}/V_o = V_{Cs2}/V_o = V_{Cs}/V_o$, $k = L_1/L = L_2/L$, $D_{ac}$ is AC/DC duty ratio, $\tau_n = L/T_sR_L$ is normalised load and $n$ is transformer turn ratio.

The AC/DC conversion ratio of this converter was found to be:

$$M_{ac} \triangleq \frac{V_o}{V_{line,rms}} = \frac{1}{4}\left(\frac{1}{m} + \sqrt{\frac{1}{m^2} + 8\frac{D_{ac}^2}{\tau_n}}\right) \quad (2)$$