FVF-Based Low-Dropout Voltage Regulator with Fast Charging/Discharging Paths for Fast Line and Load Regulation

José María Hinojo, Clara Luján-Martínez, Antonio Torralba, and Jaime Ramírez-Angulo

A new internally compensated low drop-out voltage regulator based on the cascoded flipped voltage follower is presented in this paper. Adaptive biasing current and fast charging/discharging paths have been added to rapidly charge and discharge the parasitic capacitance of the pass transistor gate, thus improving the transient response. The proposed regulator was designed with standard 65-nm CMOS technology. Measurements show load and line regulations of 433.80 µV/mA and 5.61 mV/V, respectively. Furthermore, the output voltage spikes are kept under 76 mV for 0.1 mA to 100 mA load variations and 0.9 V to 1.2 V line variations with rise and fall times of 1 µs. The total current consumption is 17.88 µA (for a 0.9 V supply voltage).

Keywords: Low drop-out (LDO), Voltage regulator, Flipped voltage follower (FVF).

I. Introduction

The system-on-chip (SoC) paradigm, motivated by a high demand in the industrial and multimedia markets for portable and battery-powered devices, has raised significant challenges in analog design. SoCs integrate a large number of electronic components into a single chip, thus reducing the number of interconnections, total power consumption, silicon area, and consequently, the total cost of the system. This approach implies that digital, analog, and RF circuits must coexist in the same die, although they have different supply requirements (concerning noise, voltage, and maximum current). Therefore, powering the different blocks of a SoC from a single battery requires the conversion and adaption of the supply signal.

This makes power management one of the major issues in SoC design. Internally compensated low drop-out (LDO) voltage regulators have proven to be essential blocks because they generate an accurate regulated voltage with high efficiency under large variations in load current and input voltage without the addition of external components.

Several techniques [1]–[7] have been proposed to improve the transient response of internally compensated LDO regulators at the cost of increasing their quiescent power consumption or degrading the rest of their performance (load and line regulations and the power supply ripple rejection ratio [PSRR]). Many of the techniques in these references use the classical LDO topology. However, Carvajal and others [8] and Ramirez-Angulo and others [9] chose the flipped voltage follower (FVF) cell as an alternative topology. This cell, shown in Fig. 1(a), offers simplicity in addition to low output impedance and good performance acting as a current buffer, which makes it a highly efficient LDO regulator. In addition, according to [10], FVF-based LDOs are more power efficient than the classical LDO topology for similar transient performance. However, despite this enhancement in efficiency,

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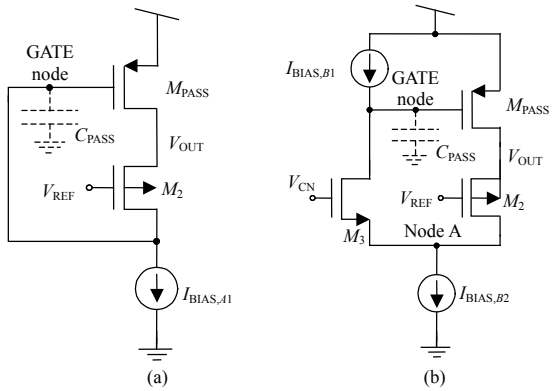

Fig. 1. (a) FVF cell configuration and (b) CAFVF cell.

the transient response of FVF-based LDOs still needs to be improved to reduce voltage spikes at the output node under the constraint of low quiescent power consumption.

Currently, many schemes to improve the load regulation and transient response of this structure can be found in the literature [11]–[19]. In [11], Man and others take advantage of FVF properties to implement a simple LDO regulator for different values of the output capacitor, equivalent series resistance, and load current. However, this provides a low open-loop gain, and therefore, a high quiescent power consumption is necessary to achieve the required gain to provide a reasonable load regulation. Blakiewicz and others [12] show some improvement by cascading the $I_{BIAS,A1}$ current source with an additional transistor in order to obtain a higher equivalent resistance at the "GATE node," as shown in Fig. 1(a). This arrangement increases the open-loop gain. In addition, a capacitive coupling of V_{OUT} to the source of the cascode transistor is introduced to increase the current that discharges the parasitic capacitance at the gate of the pass transistor M_{PASS} (C_{PASS}). However, a higher minimum input voltage and a large on-chip capacitor are required to properly operate this LDO regulator.

Further improvements regarding the open-loop gain have been achieved using a cascode flipped voltage follower (CAFVF) cell [13]–[16]. As shown in Fig. 1(b), the CAFVF cell consists of two common-gate amplifiers implemented as M_2 and M_3. In [13], a regulator with fast load regulation is proposed, where the output node is driven by multiple in-parallel CAFVF-based buffers. In order to maintain output voltage peaks under 10% of their nominal value for a 0 mA to 100 mA load current change, a large on-chip decoupling capacitor is required, which leads to a large silicon area. In [14] and [15], the transient response is improved by using RC couplings, which sense the output variations and change the $I_{BIAS,B1}$ and $I_{BIAS,B2}$ values accordingly. Nevertheless, these RC couplings do not react to line voltage variations, which could produce large voltage spikes at the output. An alternative way to implement a dynamic biasing circuit is presented in [16], where RC coupling is substituted with a digital circuit to increase the charging/discharging current of C_{PASS}. This technique speeds up the transient response, allowing a reduction in the area consumed by the passive components required for load voltage regulation. However, no information is provided in [16] regarding the performance of that structure under large line voltage variations.

Another technique proposed to improve the transient response of FVF-based LDOs is presented in [17]–[19]. A noninverting gain stage is inserted to drive the gate of the pass transistor, enhancing the slew rate (SR) and the open-loop gain. In [17], a gain-enhanced CAFVF-based LDO is presented. However, despite the increase in the open-loop gain, the circuit is only stable for a minimum output current of 3 mA, and the line transient response has a long settling time. Tan and others [18] additionally use a dual-summed Miller compensation to stabilize the regulator for a minimum load current of 0 mA. In [19], a buffered FVF with a triple-path input error amplifier (EA) is used to improve the PSRR. However, the maximum load current is limited to 10 mA, and a high quiescent consumption is required. From [17]–[19], it can be concluded that inserting a gain stage in the feedback loop of an FVF enhances the load regulation, but a careful study of the frequency response is required because the classical Miller compensation is not applicable.

In this paper, a low-power LDO regulator based on the CAFVF is proposed. This regulator exhibits a good transient response for extreme load and line variations.

The rest of this paper is organized as follows: Section II describes the structure and principle of operation of the proposed LDO regulator. In Section III, frequency response and stability issues are discussed. The measurements of the proposed LDO regulator are provided in Section IV. Finally, in Section V, some conclusions are drawn.

II. Structure and Principle of Operation

The core of the proposed LDO regulator is the CAFVF cell, as shown in Fig. 1(b). In particular, M_{PASS} is the pass transistor, which is responsible for providing the current to the load. In the same figure, M_2 is a common gate amplifier acting as an EA: it compares the output of the LDO with a reference voltage V_{SG_M2}, which is connected to its gate (1), and couples the variations of V_{OUT}, amplified by its gain, to "node A," as shown in Fig. 1(b). Finally, M_3 is a second common gate amplifier, which increases the open-loop gain. In this structure, C_{PASS} is charged or discharged by adjusting the gate voltage of M_{PASS}, the "GATE node" in Fig. 1(b), to the required value that sets V_{OUT} to its nominal value. This is achieved owing to the

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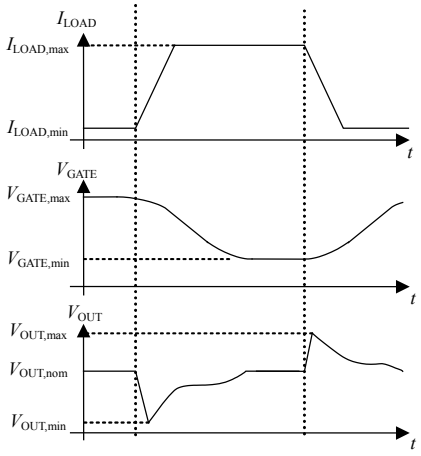

Fig. 2. Example of signal evolution for I_{LOAD} variation for internally compensated Low Dropout voltage regulator under Slew-Rate constraints.

folded cascode amplifier formed by M_2, M_3, and the current sources $I_{BIAS,B1}$ (the active load) and $I_{BIAS,B2}$ (the current source used for folding).

$$V_{REF} = V_{OUT} - V_{SG,M2}. \quad (1)$$

The CAFVF structure has its transient response limited by $I_{BIAS,B1}$ and $I_{BIAS,B2}$. In order to tackle this limitation, a thorough study on the transient response of an LDO regulator is needed. Indeed, it can be demonstrated that the SR at the gate of the pass transistor limits the settling time [20]. This is because the EA is responsible for charging and discharging C_{PASS}, and consequently, for decreasing or increasing the pass transistor gate voltage. In conclusion, if its SR is not high enough, the error at the output voltage will persist for a long settling time. Figure 2 depicts an example of such a situation for a case where the load current abruptly changes from $I_{LOAD,min}$ to $I_{LOAD,max}$.

1. Proposed Architecture with Fast Settling Schemes

In order to compensate for the poor settling time of the CAFVF under low-power constraints, this paper proposes an alternative version of this cell that enhances the transient response for both load and line variations without negative effects on the quiescent power consumption or the stability of the circuit. Figure 3 depicts the complete scheme of the proposed LDO, where the gain of the regulation loop is increased by means of the gain-boosting amplifier A_0 [21] without degrading the speed of the circuit. In order to avoid instability, this auxiliary amplifier was designed according to the method explained in [22]. A compensation capacitor for A_0 is not required because the parasitic gate-source capacitance is large enough and is approximately constant.

In addition, the line and load transient responses were improved by dynamically increasing the currents responsible for charging/discharging C_{PASS}. In particular, $I_{BIAS,B1}$ was replaced by a charge-fast settling path (C-FSP) that is formed by a dynamic current source that increases the charging current of C_{PASS} when the input or output voltage increases. This block was implemented by transistors M_7 to M_{14} and the gain-boosting amplifier A_1. For A_1, the design considerations were similar to those used for A_0. As mentioned in Section II, when the voltage V_{IN} rises, V_{OUT} instantaneously tends to grow. Thus, V_{GATE} must be rapidly increased to recover the nominal value of the output voltage. To this end, a high transient current $I_{BIAS,B1}$ is provided by means of RC coupling (R_1–C_1) to increase the positive SR (SR+) at the gate of M_{PASS}. Moreover, the output voltage is also coupled (through C_2) to magnify this effect because magnitudes V_{IN} and V_{OUT} tend to exhibit similar behavior.

A symmetrical discharge-fast settling path (D-FSP) was included to dynamically increase the discharging current of C_{PASS} when the input or output voltages decrease. Note that, in this case, an additional inverting amplifier (A_2) is required. This is implemented with a simple, low-power differential pair.

In order to reduce static power consumption, A_2 is biased in the subthreshold region and M_{38} is biased in the edge from saturation to the linear region. When V_{IN} or V_{OUT} decreases, the current through transistor M_{38} rapidly increases owing to a change in its operating region from saturation to the linear region, as described in [23]. This effect, as well as the effect of the multiplying factor K = 1:5.5 of the current mirror (which is composed of M_{37} through M_{38} [W/L = 20 μm/0.12 μm] and M_{39} through M_{40} [W/L = 110 μm/0.12 μm]), generate a high transient current in the V_{GATE} branch, and consequently produce a large negative SR (SR−) at the gate of M_{PASS}. Figures 4 and 5 depict the large transient charging and discharging currents that enhance the SR. In these figures, $I_{AB} = I_{BIAS,B1} - I_B$, and I_B is the total current that flows through M_3 and M_{40}.

Finally, in order to reduce the overshoot when the load current is switched from a heavy load to a light load, capacitor C_3, resistor R_2, and transistor M_4 are added. Note that under steady state conditions, M_4 is in the cut-off region, but when I_{LOAD} decreases, R_2 and C_3 (Table 1) sense the voltage spikes from V_A (Fig. 3) and couple them to the gate of M_4. This momentarily increases the discharging current. As a consequence, the magnitude of the overshoot is reduced, and the transient response is enhanced.

In order to achieve an effective overshoot reduction, transistor M_4 is sized to sink enough current and maintain the overshoot under 10% of the nominal output voltage value without degrading the total area of the proposed LDO.

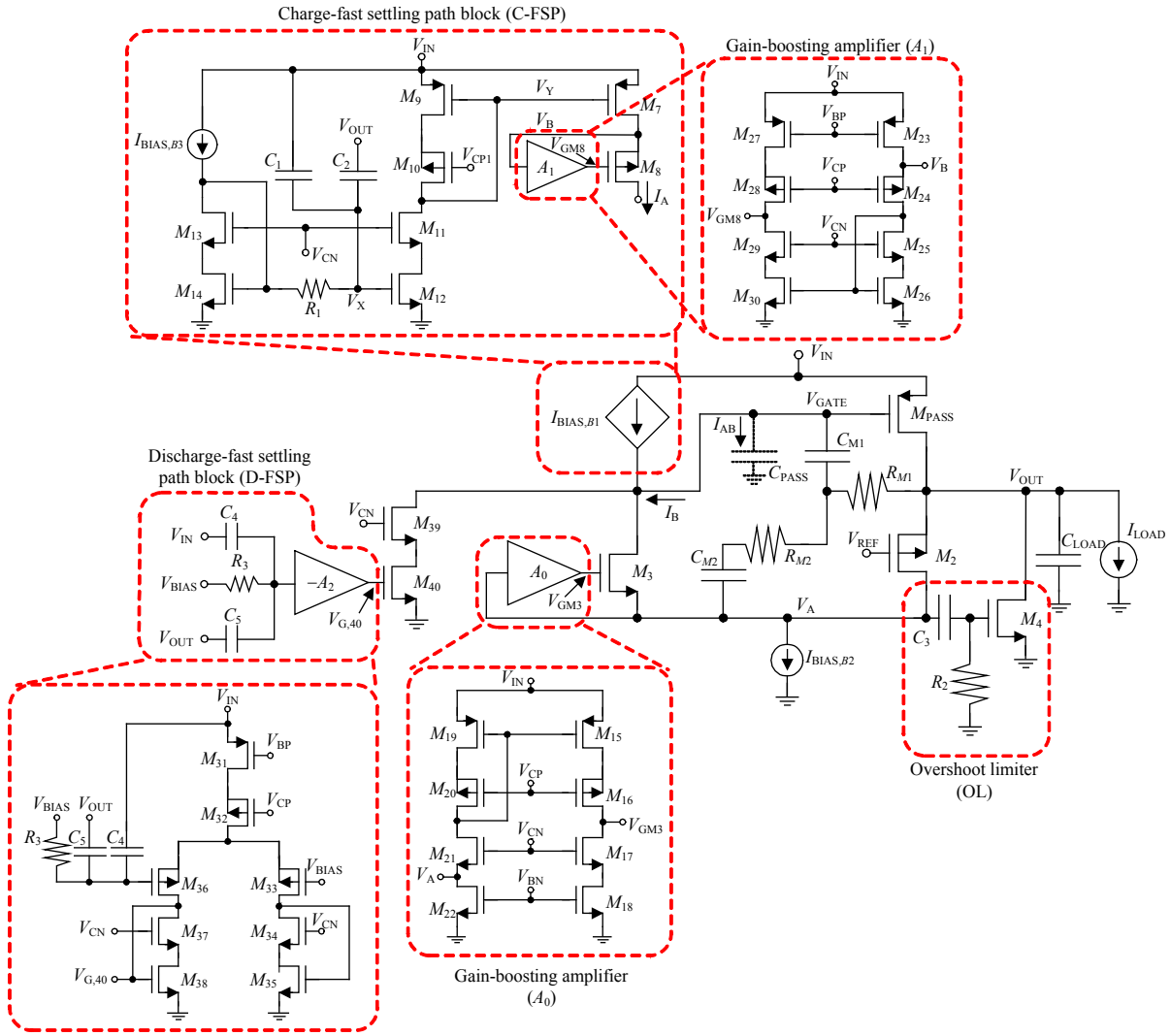

Fig. 3. Structure of proposed LDO: Circuit core showing blocks that improve settling time and limit overshoot. Detailed view of implementation of amplifiers A_0, A_1 and A_2 is also included.

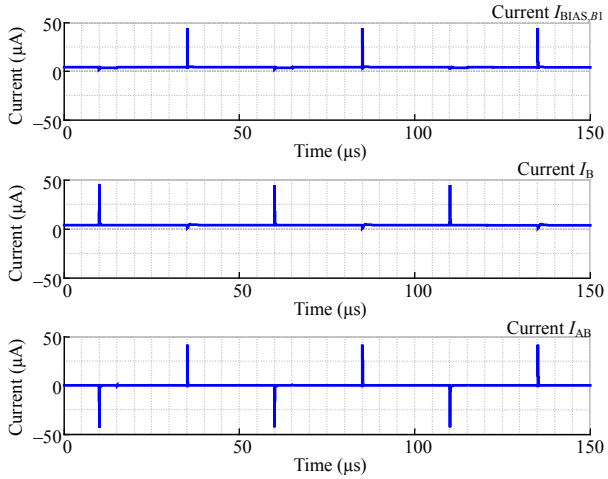

Fig. 4. Dynamic behavior of currents (Fig. 3) when I_{LOAD} changes in a square wave between its minimum (0.1 mA) and maximum (100 mA) with rising and falling time of 1 μs.

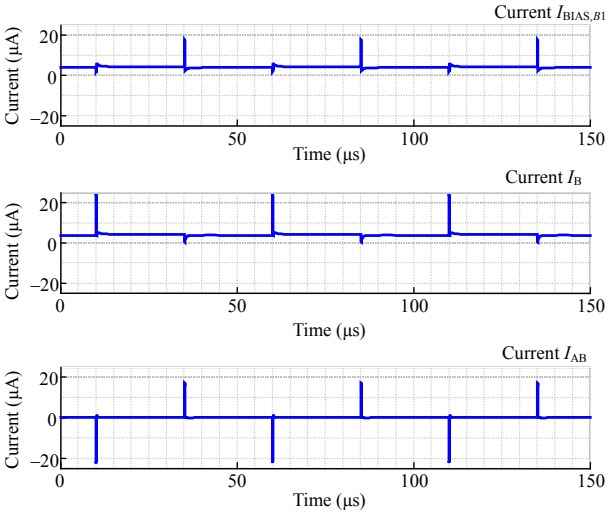

Fig. 5. Dynamic behavior of currents (Fig. 3) when V_{IN} changes in a square wave between its minimum (0.9 V) and maximum (1.2 V) with rising and falling time of 1 μs.

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Table 1. Selected values used for RC couplings.

Device	Value	Device	Value
R_1	100 (kΩ)	C_2	1.25 (pF)
R_2	335 (kΩ)	C_3	5 (pF)
R_3	100 (kΩ)	C_4	0.125 (pF)
C_1	0.125 (pF)	C_5	1.25 (pF)

Table 2. Multiplying factors and aspect ratios for transistors in biasing circuit.

Transistor	Aspect ratio (width (μm)/length (μm))	Current ratio	Value
$M_{N1,VCN}$	0.14/1.39	M_0	4
$M_{P1,VCP}$	0.12/1.49	N_0	4
$M_{BN1}-M_{BN2}$	0.14/0.12	N/A	N/A
$M_{BP1}-M_{BP2}$	0.30/0.12	N/A	N/A

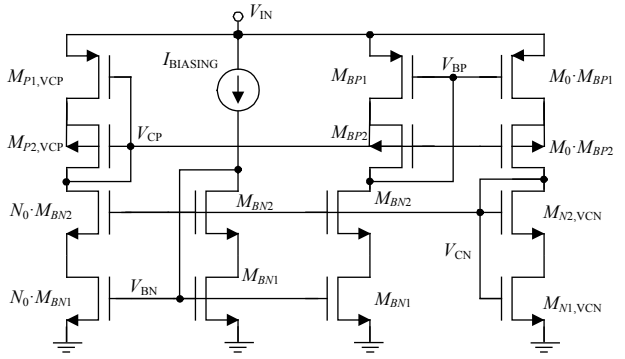


Fig. 6. Cascode and V_{BIAS} voltage biasing circuits.

According to this trade-off, the aspect ratio of transistor M_4 is 300 μm/0.06 μm.

Note that the resistor values (R_1 to R_3) were chosen to move the RC coupling effects toward a high frequency. For these values of the resistors, capacitors C_1 to C_5 are calculated to achieve the appropriate increment of V_{GATE} (2) in order to provide the required current. Table 1 lists the values of these components.

$$C = -\frac{R}{\Delta t}\ln\left[1-\frac{\Delta V_{GATE}\Delta t}{\Delta V_{IN}}\right]. \quad (2)$$

Biasing voltages are generated by the circuit shown in Fig. 6. Each branch is formed by transistors in a single-diode connection ($M_{P1,VCP}$ and $M_{P2,VCP}$ or $M_{N1,CN}$ and $M_{N2,CN}$ for PMOS and NMOS versions, respectively), and by a cascode current source (M_{BP1} or M_{BN1}). Specifically, the aspect ratios of $M_{P1,VCP}$ or $M_{N1,VCN}$, which operate in the triode region, are chosen to be lower than those of $M_{P2,VCP}$ or $M_{N2,VCN}$ in order to create the required gate voltage to supply the cascode transistor. V_{BIAS} in Fig. 3 is an external source. The current consumption of the biasing circuitry is 3.6 μA, as $I_{BIASING}$ is chosen to be 100 nA. Table 2 lists the sizes of the transistors and the current ratios for the circuit in Fig. 6.

III. Stability Analysis

In this section, the stability analysis of the proposed LDO is studied. The major concern for stability in the case of internally compensated LDOs is in their load current variations. Small-signal parameters are significantly modified, and this affects the locations of poles and zeros. This is not the case for line voltage variations.

A simplified small-signal model of the proposed structure is depicted in Fig. 7, where $g_{m,i}$ and $r_{o,i}$ are the transconductance and output resistance of transistor M_i, respectively. Note that the poles and zeros derived from the RC couplings are neglected because they are located at a very high frequency.

$$H(s) = A_{OL}\frac{1+a_1s+a_2s^2+a_3s^3+a_4s^4+a_5s^5+a_6s^6}{1+b_1s+b_2s^2+b_3s^3+b_4s^4+b_5s^5+b_6s^6+b_7s^7}, \quad (3)$$

$$A_{OL} = g_{m2}g_{mp}R_L \parallel r_{op}R_{out,D\text{-}FSP}, \quad (4)$$

$$\omega_{p1} = \frac{1}{\left(g_{mp}R_{out,D\text{-}FSP}R_L \parallel r_{op}\right)\left[C_{M1}+C_{M2}+C_{gdp}\right]}. \quad (5)$$

Concerning the transfer function in (3), the DC gain is approached by (4) and the dominant pole is given by (5). $R_{out,D\text{-}FSP}$ is the output impedance of the D-FSP block, and the nondominant pole is fixed by the output resistance and C_{LOAD}. Approximate values for the transfer function (TF) coefficients are given in (7) to (13) and (16) to (25). A reduction in the load current, I_{LOAD}, will bring the nondominant pole closer to the Unity Gain Frequency (UGF), thus degrading the stability. This behavior is represented by the pole-zero map in Fig. 8. For the sake of clarity, only poles and zeros below 100 MHz are included in the figure. Nested Miller compensation (NMC), consisting of components R_{M1}, C_{M1}, R_{M2}, and C_{M2}, was used to achieve a proper phase margin in an output current range of

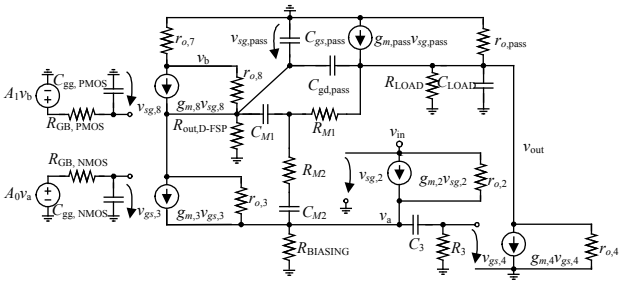


Fig. 7. Small-signal model of proposed LDO.

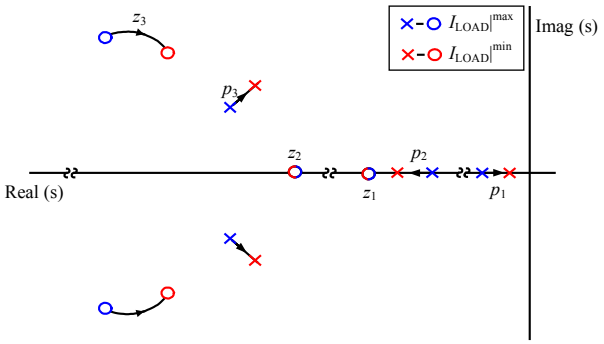


Fig. 8. Simplified pole-zero map for poles and zeros below 100 MHz.

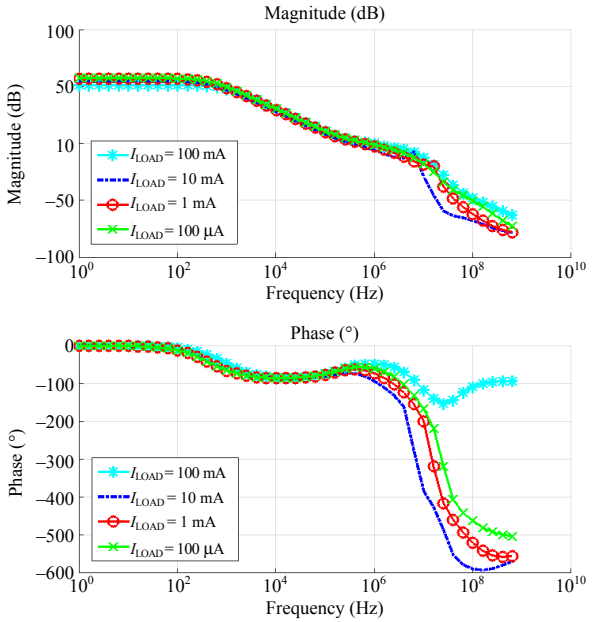


Fig. 9. Simulated post-layout open-loop gain of circuit in Fig. 3(a).

Table 3. Simulated post-layout gain and phase margin values for different load conditions.

I_{LOAD} (mA)	Gain (dB)	PM (°)	I_{LOAD} (mA)	Gain (dB)	PM (°)
100	51.30	132.0	1	56.65	115.7
10	57.24	122.2	0.1	54.38	107.2

0.1 mA to 100 mA. This resulted in R_{M1} = 1 kΩ, C_{M1} = 5 pF, R_{M2} = 10 kΩ, and C_{M2} = 8 pF.

Post-layout simulations of the open-loop gain are shown in Fig. 9 at different load conditions (100 µA, 1 mA, 10 mA, and 100 mA). Table 3 summarizes the simulated post-layout gain and phase margin values. In every case, the load capacitor is 100 pF, which is the worst-case scenario. Note that the proposed LDO is stable across the entire range of operation.

IV. Experimental Results

The proposed circuit was designed and implemented using standard 65-nm CMOS technology. Figure 10 shows a chip microphotograph next to the layout of the circuit, where the area denoted by the number 1 indicates the pass transistor M_{PASS}, and number 2 is the core of the circuit and the fast settling blocks. Number 3 corresponds to the overshoot limiter implemented by M_4, R_2, and C_3, whereas number 4 is associated with the biasing circuit. The total area is 340.8 µm × 135.5 µm. The core of the circuit occupies an area of 90.2 µm × 135.5 µm.

The LDO was designed to drive a maximum load current of 100 mA with a variable C_{LOAD} in the range 0 pF to 100 pF.

$$a_1 = R_3 C_3, \tag{6}$$

$$a_2 = R_3 C_3 \left[R_{M2} C_{M2} + R_{M1} C_{M1} \right], \tag{7}$$

$$a_3 = R_3 R_{M2} C_3 C_{M2} \left[R_{M1} C_{M1} + \frac{R_{gGB,NMOS} C_{gg,NMOS}}{A_0} + \frac{R_{gGB,PMOS} C_{gg,PMOS}}{A_1} \right], \tag{8}$$

$$a_4 = \alpha \left[\frac{1}{g_{m3}} + R_{M2} \right], \tag{9}$$

$$\alpha = \frac{R_{M1} R_3 R_{GB,NMOS} C_{M1} C_{M2} C_3 C_{gg,NMOS}}{A_0}, \tag{10}$$

$$a_5 = \beta \left[\frac{1}{g_{m,3}} + \frac{R_{M2}}{g_{m,3} r_{o,3}} + R_{M2} + \frac{1}{g_{m,8} g_{m,3} r_{o,7}} \right], \tag{11}$$

$$\beta = \alpha \frac{R_{GB,PMOS} C_{gg,PMOS}}{A_1}, \tag{12}$$

$$a_6 = \beta C_{gdp} \left[\frac{R_{M2}}{g_{mp}} + \frac{1}{g_{mp} g_{m,3}} + \frac{1}{g_{m,8} g_{m,3}} \left[\frac{1}{r_{o,8}} + \frac{1}{r_{o,7}} \right] \right]. \tag{13}$$

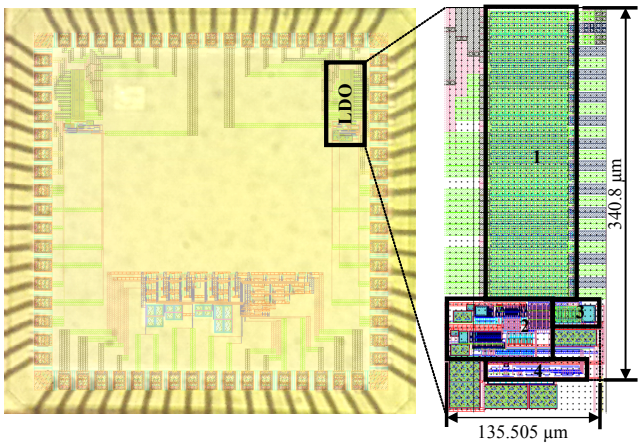
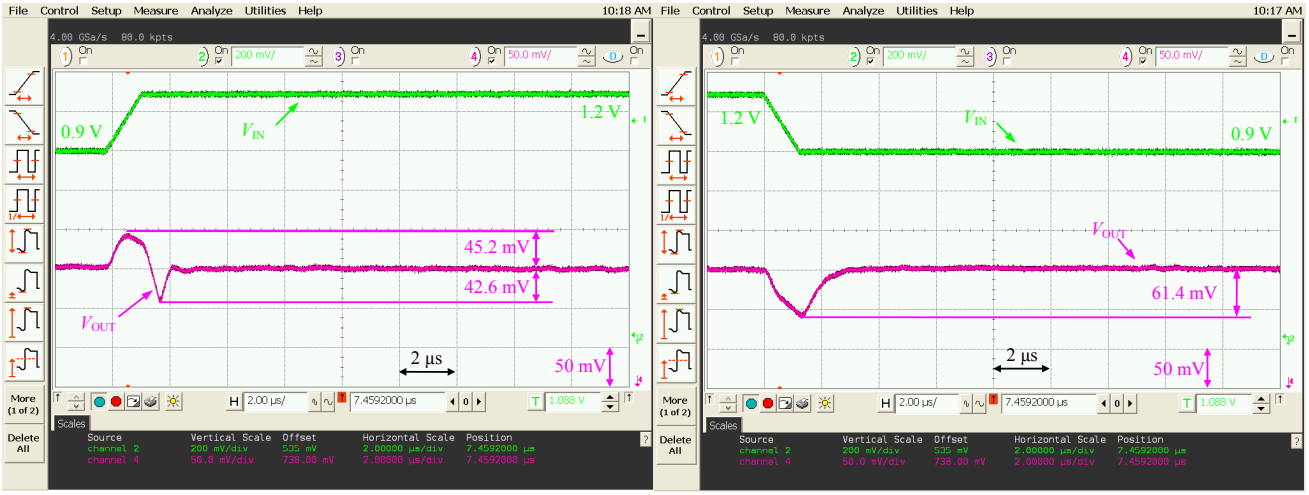
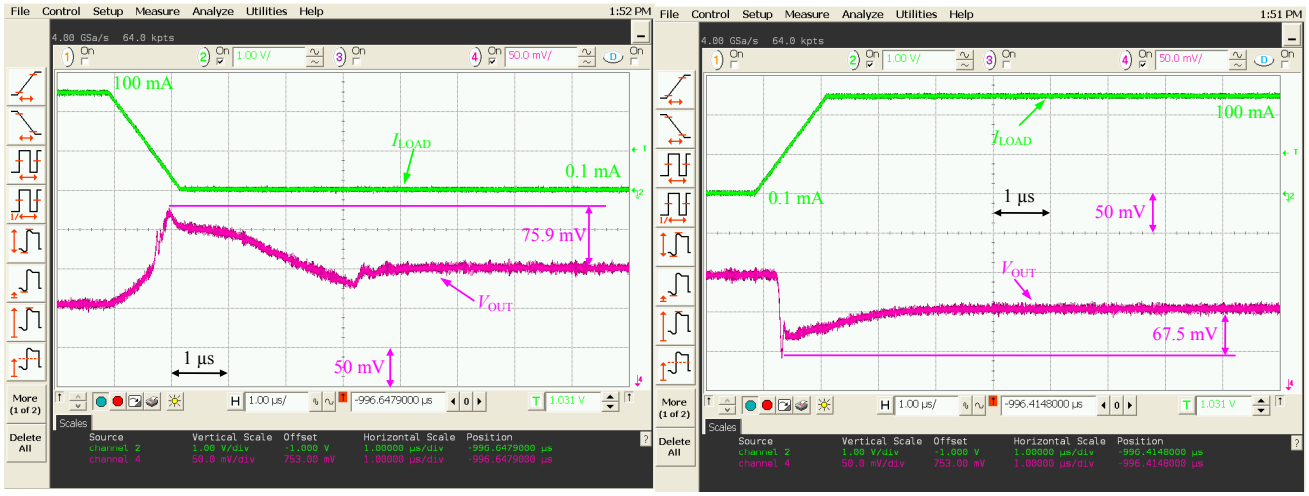


Fig. 10. LDO layout superimposed on chip microphotograph.



(a) (b)

Fig. 11. Measured line response with C_L = 100 pF and I_{LOAD} = 100 mA. (a) From 0.9 V to 1.2 V; and (b) from 1.2 V to 0.9 V with rise and fall times of 1 µs.



(a) (b)

Fig. 12. Measured load transient response with C_L = 100 pF and V_{IN} = 0.9 V. (a) From 100 mA to 0.1 mA; and (b) from 0.1 mA to 100 mA with rise and fall times of 1 µs.

Experimental results are shown in Figs. 11 and 12 for the worst-case scenario of C_{LOAD}, that is, 100 pF. Figure 11 depicts the line transient response for V_{OUT} = 0.7 V and I_{LOAD} = 100 mA, with V_{IN} changing from 0.9 V to 1.2 V and vice versa. In both cases, the rise and fall times of V_{IN} are 1 µs. Under these conditions, the output voltage shows an overshoot of 45.2 mV and an undershoot of −61.4 mV. In addition, the worst settling time, which was calculated as the time to reach 1% of steady-state V_{OUT}, is 5.17 µs. Figure 12 shows the load transient response for rise and fall times of 1 µs when V_{IN} = 0.9 V and the load current changes from 0.1 mA to 100 mA and vice versa. The voltage V_{OUT} shows a maximum variation of +75.9 mV / −67.5 mV with respect to the nominal voltage V_{OUT} = 0.7 V. Under these conditions, the worst settling time is 4.64 µs. From Figs. 11 and 12, it can be deduced that the proposed architecture exhibits a fast transient response for changes in both V_{IN} and I_{LOAD}.

Table 4 compares the performances of the proposed implementation to other reported LDO regulators. The results presented here correspond to the worst-case scenario (according to the respective authors), measured when I_{LOAD} and V_{IN} are changed between their extreme values.

$$FOM = T_r \frac{I_q}{I_{LOAD,max}}, \tag{14}$$

$$T_r = \frac{C_{OUT} \Delta V_{OUT}}{I_{LOAD,max}}, \tag{15}$$

Table 4. Comparison of recently published LDO regulators.

Parameters	[2]	[10][a]	[12]	[13]	[14]	[15]	[17]	[18][a]	**This work**
Topology	Classical	CAFVF	FVF	CAFVF	CAFVF	CAFVF	CAFVF	FVF	**CAFVF**
Technology (μm)	0.065	0.028	0.35	0.09	0.35	0.35	0.09	0.065	**0.065**
V_{IN} (V)	1.2	1.0	1.4–3.3	1.2	1.4	1.28–3.3	0.75–1.2	1.2	**0.9–1.2**
V_{OUT} (V)	1	0.8	1.2	0.9	1.2	1.1	0.5–1	1	**0.7**
Dropout (V)	0.2	0.2	0.2	0.3	0.2	0.18	0.2–0.25	0.2	**0.2**
I_{LOAD} range (mA)	0–100	0.1–100	0.1–50	0–100	1–100	0–100	1.5–100	0–50	**0.1–100**
Quiescent current consumption (μA)	0.9–82.4	100	34.6	6,000	43	25	8	23.7	**17.38–17.88**
Current efficiency at $I_{LOAD,max}$ (%)[b]	99.9177	99.0099	99.9654	94.396	99.5718	99.9750	99.9920	99.9763	**99.9823**
C_{LOAD} (pF)	100	100	0–200	600	1,000	100	50	10,000	**100**
Area (mm^2)	0.017	N/A	0.08	0.098	0.15522	0.126	0.019	N/A	**0.0292**
Settling time (μs)	~6	N/A	~1.4	~0.015	~3	~1.4	~3.75	1.65	**5.17**
ΔV_{OUT} by varying V_{IN}									
Maximum (mV)	8.91	N/A	20	N/A	N/A	20	40	N/A	**45.2**
Minimum (mV)	−10.63	N/A	−28	N/A	N/A	0	−33	N/A	**−61.4**
(ΔV_{OUT}/excitation rise time) (V/μs)	0.2/10	N/A	0.2/0.3	N/A	N/A	1/100	0.42/10	N/A	**0.3/1**
ΔV_{OUT} by varying I_{LOAD}									
Maximum (mV)	0	21	46	45	70	31	114	19	**75.9**
Minimum (mV)	−68.8	−26	−75	−45	−70	−80	−73	−58	**−67.5**
(ΔI_{LOAD}/excitation rise time) (mA/μs)	100/0.3	9.9/30e−6	49.9/0.3	100/0.0001	99/1	100/0.5	98.5/0.1	49/0.1	**99.9/1**
Line regulation (mV/V)	4.7	N/A	8.8	N/A	N/A	N/A	3.78	8.89	**5.61**
Load regulation (μV/mA)	300	N/A	3,000	900	N/A	190	100	34	**433.80**
FOM (fs)	56.69	3,120	334.93	32,400	3,311	27.75	7.48	7,299.60	**25.64**

[a] Simulation results
[b] Estimated using the maximum value of quiescent consumption

In order to compare different LDO regulators, the figure of merit (FOM) of (14), used in [13], is adopted here. T_r is the response time, and it is defined in (15).

Based on (14) and (15), the smaller the regulator FOM, the better its performance. Only the regulator of [17] outperforms the present structure. However, the classical FOM does not take into account the rise and fall times of the stimulus used to measure the transient response. Based on this observation, the regulator proposed in [17] has a poor line transient response because it cannot handle rise and fall times shorter than 10 μs of the input voltage. This is not the case for the proposed LDO, which is able to handle rise and fall times of 1 μs. In addition, a minimum load current of 1.5 mA is required for [17] to ensure stability when C_{OUT} and V_{IN} take their maximum and minimum values, respectively. This current is increased to 3 mA when C_{OUT} and V_{IN} are at their maximum values. On the other hand, the structure proposed in this work remains stable for a minimum current of 0.1 mA, regardless of the C_{OUT} and

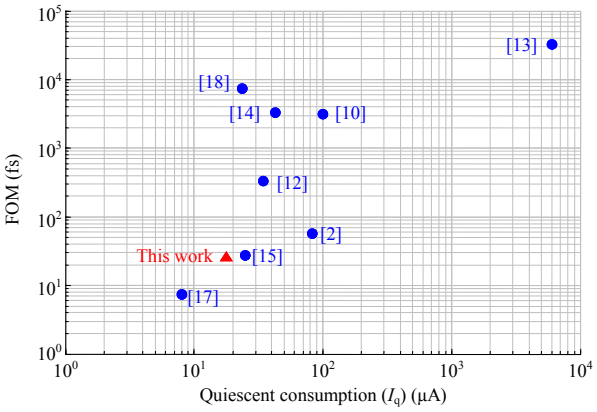


Fig. 13. Graphical comparison of recently published LDO regulators according to FOM proposed in [13].

V_{IN} values. A similar reasoning applies to [15], where the experimental results demonstrate that the circuit cannot handle line transient variations of V_{IN} faster than 100 μs. Moreover,

it requires almost 50% more power consumption than the LDO presented in this paper. Figure 13 shows a graphical comparison of recently published LDOs.

$$\gamma = g_{mp} R_{out,D\text{-}FSP} R_L \parallel r_{op}, \tag{16}$$

$$b_1 = \gamma \left[C_{M1} + C_{M2} + C_{gdp} \right], \tag{17}$$

$$b_2 = \gamma R_3 C_3 \left[C_{M1} \left[1 + \frac{1}{g_{mp} R_L \parallel r_{op}} \right] + C_{M2} + C_{gdp} \right], \tag{18}$$

$$\delta = \gamma R_3 R_{M2} C_3 C_{M2}, \tag{19}$$

$$b_3 = \delta \left[C_{M1} + C_{gdp} + \frac{R_{GB,NMOS} C_{gg,NMOS}}{A_0 R_{M2}} + \frac{C_{M1}}{g_{mp} r_{op}} \right], \tag{20}$$

$$b_4 = \delta \left[\begin{array}{l} \left[R_{GB,NMOS} C_{gg,NMOS} \left[\frac{C_{M1}}{A_0} \left[1 + \frac{1}{g_{m,3} r_{o,3}} \right] + \frac{C_{M1} + C_{gdp}}{g_{m,3} R_{M2} A_0} \right] \right] \\ + \frac{R_{GB,PMOS} C_{M1} C_{gg,PMOS}}{A_1} \\ + \frac{C_{M1}}{g_{mp}} \left[C_{LOAD} + \frac{R_{GB,NMOS} C_{gb,NMOS}}{g_{m,3} r_{op} R_{M2} K_1} \right] \end{array} \right], \tag{21}$$

$$\epsilon = \delta \frac{R_{GB,NMOS} C_{M1} C_{gg,NMOS}}{K_1}, \tag{22}$$

$$b_5 = \epsilon \left[R_{GB,PMOS} \left[\begin{array}{l} \frac{C_{gg,PMOS}}{A_1} \left[1 + \frac{1}{g_{m,3} R_{M2}} \right] \\ + \frac{C_L}{g_{mp}} \left[1 + \frac{1}{g_{m,3} R_{M2}} + \frac{C_{gsp}}{g_{m,3} C_{M1}} \right] \end{array} \right] + \frac{R_{M1} C_{gdp}}{g_{m,3} R_{M2}} \right], \tag{23}$$

$$b_6 = \epsilon \frac{R_{GB,PMOS} C_{gg,PMOS}}{A_1 R_{M2}} \left[R_{M2} + \frac{1}{g_{m,3}} + \frac{1}{g_{mp} g_{m,3}} \left[C_L \left[C_{M1} + C_{gsp} \right] + \frac{R_{M1} C_{M1} C_{gsp}}{R_L \parallel r_{op}} \right] \right] + \epsilon \frac{1}{g_{mp} R_{M2}} \left[\frac{R_{M1} R_{M2} C_{gsp} C_{gg,PMOS}}{g_{m,8} r_{o,8} A_1} + \frac{R_{M1} C_L C_{gsp}}{g_{m,3}} + \frac{R_{GB,PMOS} R_{M2} C_L C_{gg,PMOS}}{A_1} \right], \tag{24}$$

$$b_7 = \epsilon \frac{R_{GB,PMOS} R_{M1} C_L C_{gg,PMOS}}{A_1 g_{mp} R_{M2}} \left[\begin{array}{l} \frac{C_{gsp} + C_{gdp}}{g_{m,3}} + R_{M2} \left[C_{gsp} + C_{gdp} \right] \\ + \frac{C_{gsp}}{g_{m,3} g_{m,8} r_{o,7}} \end{array} \right]. \tag{25}$$

V. Conclusions

This paper proposes a new LDO regulator based on the CAFVF cell. The structure, designed with standard 65-nm CMOS technology, uses a gain-boosting technique, adaptive biasing, and fast settling paths to increase the regulation loop gain and rapidly charge/discharge the parasitic capacitance of the pass transistor gate. This leads to a fast transient response with a low power quiescent consumption. An analysis of the small-signal behavior of the proposed structure, which uses NMC, demonstrates its adequate stability in the worst case. Experimental results show small voltage spikes and short settling time for large line and load transient variations, even when the rising and falling times decrease to 1 µs. Finally, the proposed LDO regulator is shown to be a state-of-the-art device.

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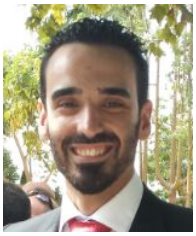

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