rate to within one node (decade) in 53% of the faults, with 100% accuracy for only 33% of the faults. However, for some transistors both resistance and location were plotted to high accuracy. The relative inaccuracy for the resistance values is due to the following:

(i) relatively large differences in resistance sometimes result in negligible changes in supply current

(ii) increasing resistance sometimes results in non-monotonic changes in supply current

(iii) two or more of the Euclidean distances may be comparable resulting in identification of the wrong winner during testing.

The proposed method is shown in Fig. 2.

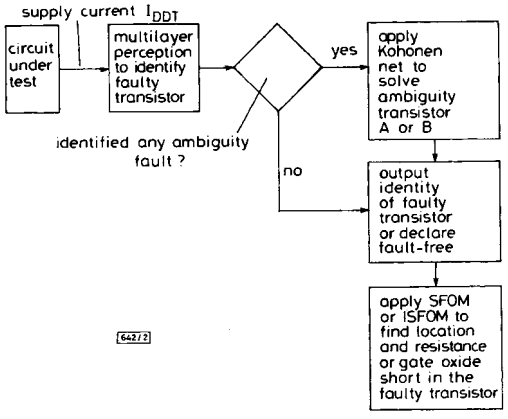

Fig. 2 *Proposed diagnostic method*

Interpolated supervised forced organisation map, ISFOM: Inspection of the weights of the intermediate nodes of the SFOM showed them to be intermediate in value between those of the trained nodes. It was therefore possible to replace the relatively lengthy procedure of training all the output nodes by interpolating the known weights of the training nodes to obtain the weights of the intermediate nodes. This considerably speeded up the training of the map. The results for the resistance values obtained were the same as for the SFOM but the location values were a little less accurate at 89% accuracy for 82% of the faults.

Conclusions:

(i) 100% accurate faulty transistor diagnosis in a CMOS opamp with gate oxide shorts is possible by pattern recognition of the supply current response to a ramp input signal in a two-stage process using first multilayer perceptrons and secondly a Kohonen unsupervised self-organising map.

(ii) Given suitable data, a supervised forced organisation map (SFOM) can be developed in which two parameters may be plotted against each other in the output map.

(iii) Extension of an SFOM to an interpolated SFOM (ISFOM) is possible in which training is avoided by calculating the weights of the intermediate nodes.

(iv) It is possible to use the output map of an SFOM or ISFOM to plot fault location against fault resistance to identify gate oxide shorts in MOSFETs in a CMOS opamp by recognising the supply current responses to ramp test stimuli.

(v) The fault locations may be determined more accurately than their resistances, e.g. 89% accuracy and one decade accuracy, respectively. In some transistors, however, both may be measured to high accuracy.

(vi) SFOMs require an order-of-magnitude less training time than Kohonen maps, while ISFOMs require no training and may be even more quickly developed.

14 September 1994
Electronics Letters Online No: 19941281

P. Collins, S. Yu and B. W. Jervis (*School of Engineering Information Technology, Sheffield Hallam University, City Campus, Pond Street, Sheffield S1 1WB, United Kingdom*)

K. R. Eckersall, I. M. Bell and G. E. Taylor (*VLSI Design & Test Group, School of Engineering and Computing, University of Hull, Cottingham Road, Hull HU6 7RX, United Kingdom*)

References

1 YU, S., JERVIS, B.W., ECKERSALL, K.R., BELL, I.M., HALL, A.G., and TAYLOR, G.E.: 'Neural network approach to fault diagnosis in CMOS opamps with gate oxide short faults', *Electron. Lett.*, 1994, **30**, (9), pp. 695–696

2 KOHONEN, T.: 'The self-organising map', *Proc. IEEE*, 1990, **78**, (9), pp. 1464–1480

CMOS optical-sensor array with high output current levels and automatic signal-range centring

S. Espejo, R. Domínguez-Castro, R. Carmona and A. Rodríguez-Vázquez

Indexing terms: CMOS integrated circuits, Photodetectors, Image sensors

A CMOS compatible photosensor with high output current levels, and an area-efficient scheme for automatic signal-range centring according to illumination conditions are presented. The high output current levels allow the use of these devices in continuous-time asynchronous imagers, as well as in high-sampling-frequency applications.

Introduction: Light transduction is required for electronic image-recording and monitoring [1]. It is also a basic feature for the emerging class of highly-parallel image-processing electronic systems, with potential application in artificial neuro-vision, pattern recognition, alert and control, etc. [2, 3]. For these latter applications, CMOS imagers enable the realisation of parallel-processing vision chips in the standard and cheapest VLSI technologies.

Conventional CMOS imagers use reverse-biased diodes as light-controlled current sources to discharge previously charged capacitors during a prescribed time interval [1]. This Letter proposes the use of two or more vertical BJTs in a Darlington configuration as photoactive devices. These photosensors, which seem to be especially adequate for binary images, exhibit a large output-current to device-area ratio, allowing their use in continuous-time applications.

Typical imagers consist of a two-dimensional sensor array, which encodes the input image into a matrix of electrical values (pixels). For any given scene, the average pixel value is a strong function of the environment luminosity. For this reason, mechanical and/or electrical adaptation are required to adjust the sensitivity of the imager. This Letter proposes a real-time collective computation circuit to represent the image by the deviation of the individual pixels with respect to their mean value. The proposed photosensors and signal-centring circuitry have been tested on a 15μm *n*-well CMOS process.

Darlington photosensor: Fig. 1*a* illustrates a cross-section of a CMOS photodiode. The reverse current I_J in the diode is approximately given by [4]

$$I_J = \alpha A_W L \qquad (1)$$

where α is a proportionality factor, A_W is the well region area, and L is the light intensity. Referring to the technology used and normal laboratory illumination, the product αL is 4.5pA/μm². Clearly, unless large devices are used, the resulting current levels are too low to be direclly used as input to typical processing circuits.

A well-known altemative [5] is the use of a vertical BJT, as

shown in Fig. 1*b*. The reverse-bias current of the well-substrate (base-collector) junction constitutes a base current, which is amplified at the emitter by the usual relationship in the active-forward region

$$I_T = (\beta_F + 1)I_J = (\beta_F + 1)\alpha A_W L \qquad (2)$$

The measured value of β_F is 39, giving a photocurrent to well-area ratio of 180pA/μm². Current levels are still too low for direct use in most practical cases. Further amplification can be achieved by using two (or more) vertical BJTs in a Darlington configuration, as shown in Fig. 1*c*. The resulting current is given by

$$I_D = (\beta_F + 1)^2 \alpha A_{WS} L + (\beta_F + 1)\alpha A_{WA} L \qquad (3)$$

where subscripts S and A refer to transistors Q_S and Q_A in Fig. 1*c*, respectively. Maximum area efficiency is obtained using amplifying transistors (Q_A) with minimum geometries, and designing the well region of the sensing transistor (Q_S) to achieve the required sensitivity. Neglecting the second term in eqn. 3, and approximating the photosensor area by A_{WS}, the photocurrent to area ratio of the device is 7nA/μm², which is sufficiently high for typical applications.

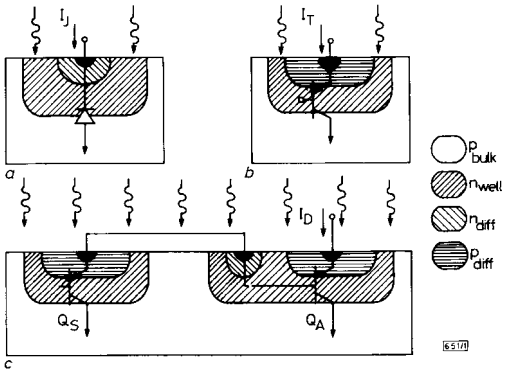

Fig. 1 *CMOS compatible photosensors*

a Diode
b Vertical BJT
c Two vertical BJTs in Darlington configuration

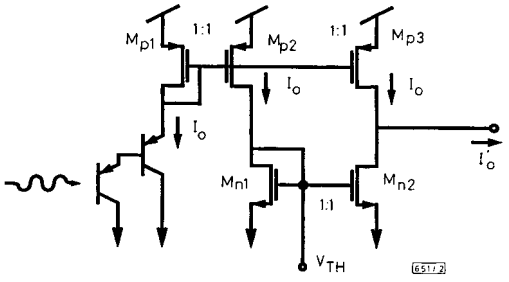

Fig. 2 *Signal-range centring circuitry used at each sensor location*

Signal-range centring: The circuit in Fig. 2 modifies the image representation replacing the current at each sensor by its deviation with respect to their instantaneous mean value. This circuitry must be replicated at every sensor location, and node V_{TH} must be common to every sensor. Then, at each individual sensor i, the photogenerated current $I_o(i)$ is replicated twice by means of the double-output current mirror composed of transistors $M_{p1}(i)$, $M_{p2}(i)$, and $M_{p3}(i)$. The number of sensors in the array is denoted by N. Because node V_{TH} is common to every sensor in the array, the individual transistors $M_{n1}(i)$ are all ($i = 1, \ldots, N$) connected in parallel, and hence constitute a single spatially-distributed transistor, which we denote M_{N1}. The equivalent aspect ratio W/L of this transistor is clearly N times larger than that of any $M_{n1}(i)$ or $M_{n2}(i)$. Because node V_{TH} is a global node, the individual currents $I_o(i)$ flowing through transistors $M_{p2}(i)$ are added at node V_{TH}, and the sum flows through the distributed transistor M_{N1}:

$$I_{M_{N1}} = \sum_{i=1}^{N} I_o(i) \qquad (4)$$

Every transistor $M_{n2}(i)$ forms a current mirror with M_{N1}, the current-gain being $1/N$. Thus,

$$I_{M_{n2}}(i) = \frac{I_{M_{N1}}}{N} = \frac{1}{N}\sum_{i=1}^{N} I_o(i) = \overline{I}_o \quad \forall i \qquad (5)$$

Finally, it is clear from Fig. 2 that

$$I'_o(i) = I_o(i) - I_{M_{n2}}(i) = I_o(i) - \overline{I}_o \quad \forall i \qquad (6)$$

which is the required transformation. Note that, if required, the average photocurrent value can be recovered from the voltage level at node V_{TH}, for instance using a current mirror. Hence, the transformation represents no loss of information.

A small-signal analysis of the finite-impedance effect at node V_{TH} results in

$$I_{M_{n2}}(i) = \frac{N g_{mn}}{N g_{mn} + N\overline{g_{dsp}}}\overline{I}_o = \frac{g_{mn}}{g_{mn} + \overline{g_{dsp}}}\overline{I}_o \quad \forall i \qquad (7)$$

where g_{mn} is the small-signal transconductance of transistors $M_{n1}(i)$, and $\overline{g_{dsp}}$ is the average output conductance of $M_{p2}(i)$. Typically, $g_{mn} > \overline{g_{dsp}}$ and hence, eqn. 5 is a good approximation of eqn. 7, as expected. The important issue is that the finite-impedance error reflected in eqn. 7 is invariant with the number of sensors in the array, because both the equivalent g_{dsp} and g_{mn} are multiplied by N.

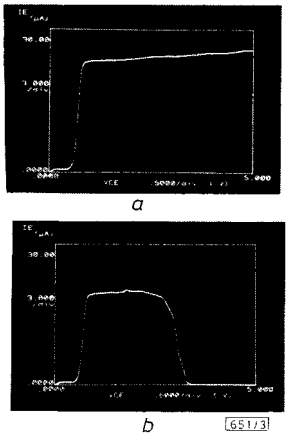

Fig. 3 *Measured I-V response of Darlington photosensor*

a Constant illumination
b Illumination reduction during voltage sweep

Horizontal scale: 0.5V/division
Vertical scale: 3μA/division

Experiment: The Darlington photosensor and the image-centring circuitry have been tested using several prototypes manufactured using 1.5μm *n*-well CMOS digital technology.

Fig. 3*a* shows the measured I-V characteristic of a Darlington photosensor with A_{WS} = 3600μm², under constant laboratory illumination; Fig. 3*b* shows the result obtained when light intensity is gradually reduced during the voltage sweep.

The signal-range centring circuitry has been successfully used, together with minimum geometry Darlington photosensors (A_{WS} = 185μm²), in several highly-parallel image-processing chips [6]. The image-acquisition circuitry was evaluated under different illumination conditions, corresponding to light-source dissipation within a two-decade range.

21 September 1994
Electronics Letters Online No: 19941287

S. Espejo, R. Dominguez-Castro, R. Carmona and A. Rodríguez-Vázquez (*Centro Nacional de Microelectrónica, Universidad de Sevilla, Avda. Reina Mercedes s/n. E-41012 Sevilla, Spain*)

References

1 Proc. SPIE: Imaging Technologies and Applications. Vol. 1778. 1992

2 GUPTA, M.M., and KNOPF, G.K. (Ed.): 'Neuro-vision systems, principles and applications' (IEEE Press, 1994)

3 DELBRÜCK, T.: 'Silicon retina with correlation-based, velocity tuned pixels', *IEEE Trans.*, 1993, **NN-4**, (3), pp. 529–541

4 SOCLOF, S.: 'Applications of analog integrated circuits' (Prentice Hall Inc., 1985)

5 VIDAL, M.P., BAFLEUR, M., BUXO, J., and SARRABAYROURE, G.: 'A bipolar photodetector compatible with standard CMOS technology', *Solid State Electron.*, 1991, **34**, (8), pp. 809–814

6 ESPEJO, S., RODRÍGUEZ-VÁZQUEZ, A., DOMÍNGUEZ-CASTRO, R., HUERTAS, J.L., and SÁNCHEZ-SINENCIO, E.: 'An analog design technique for smart-pixel CMOS chips'. Proc. 1993 ESSCIRC, September 1993, (Sevilla), pp. 78–81

Low voltage BiCMOS dynamic logic gates

H.P. Chen and Y.P. Wu

Indexing terms: BiCMOS integrated circuits, Logic gates

A low-supply-voltage BiCMOS logic gate is presented which can be used to form a pipelined system using the two-phase non-overlapping clocks. The new BiCMOS dynamic logic gates have no DC power dissipations and they have full voltage swings. It has been shown that the use of the described feedback technique provides a lower gate delay than previously reported low-voltage designs.

Introduction: Performance degradation at low voltage is verified to be a major limiting factor for BiCMOS circuits. The reduced swing degrades the speed of the driven gates, especially when the supply voltage is scaled down. Another disadvantage of the reduced swing is the noise margin reduction. To overcome the drawback, full-swing complementary designs using complementary bipolar device have been recently reported [1]. However, the advantages of the C-BiCMOS are considerably offset by the additional process complexity and cost for the *pnp* bipolar fabrication. In this Letter, a circuit technique using a feedback inverter to improve the BiCMOS logic swing and allow low voltage operation is proposed. This design offers an effective speed improvement over other existing designs, such as merged BiCMOS (M-BiCMOS) [2] and quasi-complementary BiCMOS (QC-BiCMOS) [3], without using extra processing steps in an *npn*-only BiCMOS process.

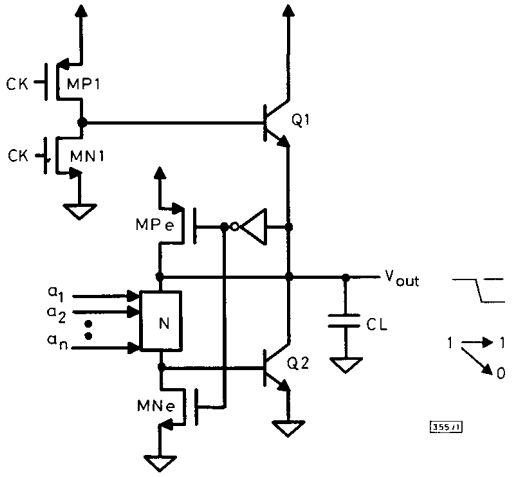

Fig. 1 *Proposed BiCMOS dynamic N-cell*

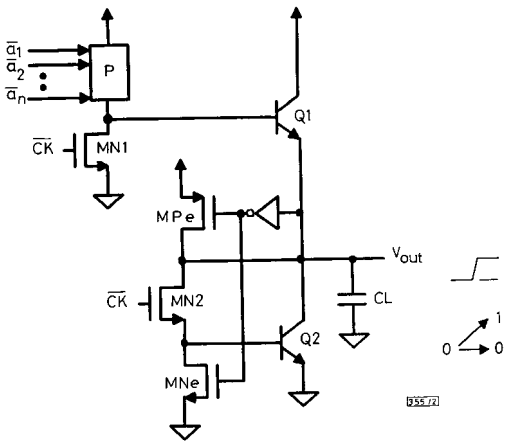

Fig. 2 *Proposed BiCMOS dynamic P-cell*

Circuit: The full-swing operation can be realised by using a feedback inverter as shown in Figs. 1 and 2. To organise to form a dynamic pipelined system [4], the logic gates can be divided into two types, the *N*-cell and *P*-cell. The operation of these two gates is as follows. As shown in Fig. 1, the *N*-cell has two operation phases, that is, precharge phase and evaluation phase. During the precharge period when the *CK* signal is low, *MN*1 is turned off, and the current supplied by *MP*1 is fully used to drive *Q*1. The output node is charged quickly to a value higher than $V_{dd} - V_{BE}$. Using the feedback inverter, the output node is pulled up to V_{dd} through *MPe*. After the precharge period when the *CK* signal goes high, *MNe* is turned off and the base of *Q*1 is discharged through *MN*1. Hence, short circuit current in *Q*1 and *Q*2 can be avoided during the next pull-down thereby reducing unnecessary power dissipation. The output logic value is determined by the logic circuit block N, which is composed of *n*MOS transistors. Assuming a high-to-low transition at the output node due to the logic value, the output voltage decreases until it reaches V_{BE}. *MNe* is turned on in this time. This could lead to the saturation of *Q*2 causing the output voltage to fall to V_{CE}, close to 0V. As shown in Fig. 2, the operation of the *P*-cell can be similarly explained as follows. During the predischarge phase when $\overline{CK}$ is high, *Q*1 is turned off due to the turned on *MN*1 and the output node is discharged to set up to low level, close to 0 V. During the evaluation phase when $\overline{CK}$ is low, *MN*1 is turned off and the base of *Q*2 is discharged by *MNe*. The output logic value is determined by the logic circuit block *P*, which is composed of *p*MOS transistors.

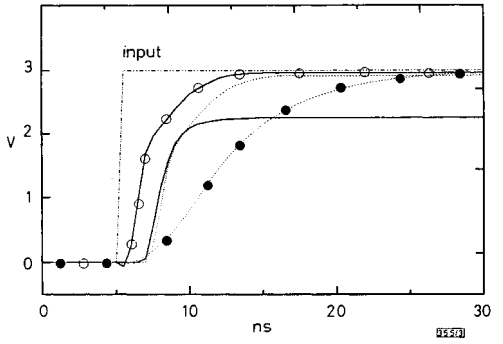

Fig. 3 *Transient waveforms of the four inverters*

- - ● - - CMOS
——— M-BiCMOS [1]
- - - - QC-BiCMOS [2]
- - ○ - - proposed BiCMOS (*N*-cell + *P*-cell)

Comparisons: To compare the performance of the proposed BiCMOS circuit with those of CMOS, M-BiCMOS, and QC-BiCMOS circuits, the series of two inverters of each BiCMOS circuit is sim-