rate to within one node (decade) in 53% of the faults, with 100% accuracy for only 33% of the faults. However, for some transistors both resistance and location were plotted to high accuracy. The relative inaccuracy for the resistance values is due to the following:

(i) relatively large differences in resistance sometimes result in negligible changes in supply current

(ii) increasing resistance sometimes results in non-monotonic changes in supply current

(iii) two or more of the Euclidean distances may be comparable

The proposed method is shown in Fig. 2.

Interpolated supervised forced organisation map, ISFOM: Inspection of the weights of the intermediate nodes of the SFOM showed them to be intermediate in value between those of the trained nodes. It was therefore possible to replace the relatively lengthy procedure of training all the output nodes by interpolating the known weights of the training nodes to obtain the weights of the intermediate nodes. This considerably speeded up the training of the map. The results for the resistance values obtained were the same as for the SFOM but the location values were a little less accurate at 89% accuracy for 82% of the faults.

Conclusions:

(i) 100% accurate faulty transistor diagnosis in a CMOS opamp with gate oxide shorts is possible by pattern recognition of the supply current response to a ramp input signal in a two-stage process using first multilayer perceptions and secondly a Kohonen unsupervised self-organising map.

(ii) Given suitable data, a supervised forced organisation map (SFOM) can be developed in which two parameters may be plotted against each other in the output map.

(iii) Extension of an SFOM to an interpolated SFOM (ISFOM) is possible in which training is avoided by calculating the weights of the intermediate nodes.

(iv) It is possible to use the output map of an SFOM or ISFOM to plot fault location against fault resistance to identify gate oxide shorts in MOSFETs in a CMOS opamp by recognising the supply current responses to ramp test stimuli.

(v) The fault locations may be determined more accurately than their resistances, e.g. 89% accuracy and one decade accuracy, respectively. In some transistors, however, both may be measured to high accuracy.

(vi) SFOMs require an order-of-magnitude less training time than Kohonen maps, while ISFOMs require no training and may be even more quickly developed.

CMOS optical-sensor array with high output current levels and automatic signal-range centring

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Indexing terms: CMOS integrated circuits, Photodetectors, Image sensors

A CMOS compatible photosensor with high output current levels, and an area-efficient scheme for automatic signal-range centring according to illumination conditions are presented. The high output current levels allow the use of these devices in continuous-time asynchronous imagers, as well as in high-sampling-frequency applications.

Introduction: Light transduction is required for electronic image-recording and monitoring [1]. It is also a basic feature for the emerging class of highly-parallel image-processing electronic systems, with potential application in artificial neuro-vision, pattern recognition, alert and control, etc. [2, 3]. For these latter applications, CMOS imagers enable the realisation of parallel-processing vision chips in the standard and cheapest VLSI technologies.

Conventional CMOS imagers use reverse-biased diodes as light-controlled current sources to discharge previously charged capacitors during a prescribed time interval [1]. This Letter proposes the use of two or more vertical BJTs in a Darlington configuration as photactive devices. These photosensors, which seem to be especially adequate for binary images, exhibit a large output-current to device-area ratio, allowing their use in continuous-time applications.

Typical imagers consist of a two-dimensional sensor array, which encodes the input image into a matrix of electrical values (pixels). For any given scene, the average pixel value is a strong function of the environment luminosity. For this reason, mechanical and/or electrical adaptations are required to adjust the sensitivity of the imager. This Letter proposes a real-time collective computation circuit to represent the image by the deviation of the individual pixels with respect to their mean value. The proposed photosensors and signal-centring circuitry have been tested on a 15μm n-well CMOS process.

Darlington photosensor: Fig. 1a illustrates a cross-section of a CMOS photodiode. The reverse current $I_r$ in the diode is approximately given by [4]

$$\text{(1)} I_r = K \cdot A_W \cdot L$$

where $K$ is a proportionality factor, $A_W$ is the well region area, and $L$ is the light intensity. Referring to the technology used and normal laboratory illumination, the product $A_W L$ is 4.5pAμm².

Clearly, unless large devices are used, the resulting current levels are too low to be directly used as input to typical processing circuits.

A well-known alternative [5] is the use of a vertical BJT, as...
shown in Fig. 1b. The reverse-bias current of the well-substrate (base-collector) junction constitutes a base current, which is amplified at the emitter by the usual relationship in the active-forward region

\[ I_P = (\beta_P + 1)I_D = (\beta_P + 1) \alpha A_W L \]  

(2)

The measured value of \( \beta_P \) is 39, giving a photocurrent to well-area ratio of 180pA/\mu m². Current levels are still too low for direct use in most practical cases. Further amplification can be achieved by using two (or more) vertical BJTs in a Darlington configuration, as shown in Fig. 1c. The resulting current is given by

\[ I_D = (\beta_P + 1) \beta_P A_W L = (\beta_P + 1) \alpha A_W L \]  

(3)

where subscripts \( S \) and \( A \) refer to transistors \( Q_S \) and \( Q_A \) in Fig. 1c, respectively. Maximum area efficiency is obtained using amplifying transistors \( Q_S \) with minimum geometries, and designing the well region of the sensing transistor \( Q_A \) to achieve the required sensitivity. Neglecting the second term in eqn. 3, and approximating the photosensor area by \( A_{\text{eq}} \), the photocurrent to area ratio of the device is 7nA/\mu m², which is sufficiently high for typical applications.

Signal-range centring: The circuit in Fig. 2 modifies the image representation at each sensor location, and node \( V_{TM} \) must be common to every sensor. Then, at each individual sensor \( i \), the photo-generated current \( I_{S}(i) \) is replicated twice by means of the double-output current mirror composed of transistors \( M_{P2}(i), M_{P3}(i), \) and \( M_{S}(i) \). The number of sensors in the array is denoted by \( N \). Because node \( V_{TM} \) is common to every sensor in the array, the individual transistors \( M_{P2}(i) \) are all \( (i = 1, ..., N) \) connected in parallel, and hence constitute a single spatially-distributed transistor, which we denote \( M_{P2} \). The equivalent aspect ratio \( W/L \) of this transistor is clearly \( N \) times larger than that of any \( M_{P2}(i) \) or \( M_{P3}(i) \). Because node \( V_{TM} \) is a global node, the individual currents \( I_{S}(i) \) flowing through transistors \( M_{P2}(i), M_{P3}(i) \) are added at node \( V_{TM} \), and the sum flows through the distributed transistor \( M_{P2} \).

Every transistor \( M_{P2}(i) \) forms a current mirror with \( M_{S}(i) \), the current-gain being \( 1/N \). Thus,

\[ I_{M_{P2}} = \frac{1}{N} \sum_{i=1}^{N} I_{S}(i) \]  

(4)

which is required transformation. Note that, if required, the average photocurrent value can be recovered from the voltage level at node \( V_{TM} \), for instance using a current mirror. Hence, the transformation represents no loss of information.

A small-signal analysis of the finite-impedance effect at node \( V_{TM} \) results in

\[ I_{M_{P2}}(i) = \frac{N g_{m}}{N g_{m} + N g_{sp}} I_{S}(i) = \frac{g_{m}}{g_{m} + g_{sp}} I_{S}(i) \]  

\[ \forall i \]  

(5)

where \( g_{m} \) is the small-signal transconductance of transistors \( M_{P2}(i), \) and \( g_{sp} \) is the average output conductance of \( M_{P2}(i) \). Typically, \( g_{m} > g_{sp} \) and hence, eqn. 5 is a good approximation of eqn. 7, as expected. The important issue is that the finite-impedance error reflected in eqn. 7 is invariant with the number of sensors in the array, because both the equivalent \( g_{m} \) and \( g_{sp} \) are multiplied by \( 1/N \).

Signal-range centring: The circuit in Fig. 2 modifies the image representation at each sensor location, and node \( V_{TM} \) must be common to every sensor. Then, at each individual sensor \( i \), the photo-generated current \( I_{S}(i) \) is replicated twice by means of the double-output current mirror composed of transistors \( M_{P2}(i), M_{P3}(i), \) and \( M_{S}(i) \). The number of sensors in the array is denoted by \( N \). Because node \( V_{TM} \) is common to every sensor in the array, the individual transistors \( M_{P2}(i) \) are all \( (i = 1, ..., N) \) connected in parallel, and hence constitute a single spatially-distributed transistor, which we denote \( M_{P2} \). The equivalent aspect ratio \( W/L \) of this transistor is clearly \( N \) times larger than that of any \( M_{P2}(i) \) or \( M_{P3}(i) \). Because node \( V_{TM} \) is a global node, the individual currents \( I_{S}(i) \) flowing through transistors \( M_{P2}(i), M_{P3}(i) \) are added at node \( V_{TM} \), and the sum flows through the distributed transistor \( M_{P2} \).
Low voltage BiCMOS dynamic logic gates

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Indexing terms: BiCMOS integrated circuits, Logic gates

A low-supply-voltage BiCMOS logic gate is presented which can be used to form a pipelined system using the two-phase non-overlapping clocks. The new BiCMOS dynamic logic gates have an AC power dissipations and they have full voltage swings. It has been shown that the use of the described feedback technique provides a lower gate delay than previously reported low-voltage designs.

Introduction: Performance degradation at low voltage is verified to be a major limiting factor for BiCMOS circuits. The reduced swing degrades the speed of the driven gates, especially when the supply voltage is scaled down. Another disadvantage of the reduced swing is the noise margin reduction. To overcome the bipolar device have been recently reported [1]. However, the drawback, full-swing complementary designs using complementary MOS) [2] and quasi-complementary BiCMOS (QC-BiCMOS) [3], without using extra processing steps in an npn-only BiCMOS process.

Fig. 1 Proposed BiCMOS dynamic N-cell

Fig. 2 Proposed BiCMOS dynamic P-cell

Circuit: The full-swing operation can be realised by using a feedback inverter as shown in Figs. 1 and 2. To organise to form a dynamic pipelined system [4], the logic gates can be divided into two types, the N-cell and P-cell. The operation of these two gates is as follows. As shown in Fig. 1, the N-cell has two operation phases, that is, precharge phase and evaluation phase. During the precharge period when the CK signal is low, MN1 is turned off, and the current supplied by MP1 is fully used to drive Q1. The output node is charged quickly to a value higher than Vss - VBE. Using the feedback inverter, the output node is pulled up to VDD through MPe. After the precharge phase when the CK signal goes high, MNe is turned off and the base of Q1 is discharged through MN1. Hence, short circuit current in Q1 and Q2 can be avoided during the next pull-down thereby reducing unnecessary power dissipation. The output logic value is determined by the logic circuit block N, which is composed of pMOS transistors. Assuming a high-to-low transition at the output node due to the logic value, the output voltage decreases until it reaches Vss. MNe is turned on in this time. This could lead to the saturation of Q2 causing the output voltage to fall to VBE close to 0V. As shown in Fig. 2, the operation of the P-cell can be similarly explained as follows. During the predischARGE phase when CK is high, Q1 is turned off due to the turned on MN1 and the output node is discharged to set up to low level, close to 0V. During the evaluation phase when CK is low, MN1 is turned off and the base of Q2 is discharged by MNe. The output logic value is determined by the logic circuit block P, which is composed of pMOS transistors.

Comparisons: To compare the performance of the proposed BiCMOS circuit with those of CMOS, M-BiCMOS, and QC-BiCMOS circuits, the series of two inverters of each BiCMOS circuit is sim-