A 13-bit, 2.2-MS/s, 55-mW Multibit Cascade $\Sigma\Delta$ Modulator in CMOS 0.7-μm Single-Poly Technology

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***Abstract*—This paper presents a CMOS 0.7-μm $\Sigma\Delta$ modulator IC that achieves 13-bit dynamic range at 2.2 MS/s with an oversampling ratio of 16. It uses fully differential switched-capacitor circuits with a clock frequency of 35.2 MHz, and has a power consumption of 55 mW. Such a low oversampling ratio has been achieved through the combined usage of fourth-order filtering and multibit quantization. To guarantee stable operation for any input signal and/or initial condition, the fourth-order shaping function has been realized using a cascade architecture with three stages; the first stage is a second-order modulator, while the others are first-order modulators—referred to as a 2-1-$1_{\rm mb}$ architecture. The quantizer of the last stage is 3 bits, while the other quantizers are single bit. The modulator architecture and coefficients have been optimized for reduced sensitivity to the errors in the 3-bit quantization process. Specifically, the 3-bit digital-to-analog converter tolerates 2.8% FS nonlinearity without significant degradation of the modulator performance. This makes the use of digital calibration unnecessary, which is a key point for reduced power consumption. We show that, for a given oversampling ratio and in the presence of 0.5% mismatch, the proposed modulator obtains a larger signal-to-noise-plus-distortion ratio than previous multibit cascade architectures. On the other hand, as compared to a 2-1-$1_{\rm single\text{-}bit}$ modulator previously designed for a mixed-signal asymmetrical digital subscriber line modem in the same technology [1], the modulator in this paper obtains one more bit resolution, enhances the operating frequency by a factor of two, and reduces the power consumption by a factor of four.**

***Index Terms*—Analog-to-digital conversion, sigma–delta modulation, switched-capacitor circuits.**

I. Introduction

During the last few years, oversampling $\Sigma\Delta$ converters have been demonstrated that are very well suited for on-chip design of the analog-to-digital interfaces of modern mixed-signal CMOS application-specific integrated circuit (ASIC's) [2], [3]. Today, they constitute a convenient architectural choice for applications requiring more than 12-bit resolution and a signal frequency below 1 MHz [1], [4]–[6], and several attempts have been made to use them above 1 MHz as well [7]–[9]. Such attempts have been prompted by the current strong interest in the design of mixed-signal ASIC's for telecom applications, particularly on the design of cable modems for future digital subscriber loops (xDSL) [10].

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As compared to Nyquist converters, $\Sigma\Delta$ converters feature smaller sensitivity to the imperfections of the analog circuitry—a consequence of the time averaging inherent to the oversampling converter operation. It is advantageous for mixed-signal system realizations using the most dense, and cheapest, mainstream CMOS technologies instead of the better performing, but less dense and more expensive, analog-oriented technologies. However, for oversampling $\Sigma\Delta$ converters to be feasible within the telecom range, new architectures and techniques have to be devised in order to reduce the *oversampling ratio* (M) needed to obtain a given *dynamic range* (DR) at the modulator front end.

The DR of $\Sigma\Delta$ modulators is directly proportional, on the one hand, to $(2^b-1)^2$, where b is the resolution (in bits) of the internal quantizer, and, on the other hand, to $M^{(2L+1)}$, where L is the order of the modulator filter [2]. Consequently, to improve DR without increasing the oversampling ratio, two complementary strategies can be adopted, namely, a) using multibit (mb) quantization and b) using high-order filtering. Each of these strategies exhibits problems that must be addressed for practical applications. The main problem of high-order filters, particularly those realized through a single-loop architecture [2], is that they do not guarantee stable operation for any input signal and/or initial condition. On the other hand, a problem of mb quantization is that the linearity of the internal mb digital-to-analog converter (DAC) may constrain the linearity of the overall modulator [2]. Partial solutions to these problems have been reported elsewhere. For instance, single-loop, high-order filters can be stabilized through proper choice of the scaling factors [3], the use of multipath feed-forward structures [11], or resetting of the internal variables when an unstable operation is detected [12]. Also, the internal DAC nonlinearity can be corrected through calibration, either in the analog domain [13], [14] or in the digital domain [4], [15]. The analog-domain correction technique has been recently used in [9], which proposes the interesting use of a low-order mb$\Sigma\Delta$ modulator in cascade with a pipelined analog-to-digital converter (ADC). However, as shown later, the use of rather complex subblocks in the reported IC (a second-order, 5-bit, pipelined cascade) results in a large power dissipation. As an alternative to these approaches, the modulator architecture used in this paper overcomes the problems of high-order filters and mb quantizers without either calibration or resetting required. The basic idea consists of first, performing the high-order filtering through a cascade structure to guarantee unconditional stability for any input level and initial condition; and second, using mb

quantization only at the last stage of the cascade to attenuate the influence of the DAC nonlinearity [7], [16].

Previous mb cascade $\Sigma\Delta$ modulators reported in literature attenuate the in-band DAC nonlinearity error by M^5 under ideal operating conditions [7], [16]. However, in the presence of circuit imperfections, these architectures require $M = 24$ to feature 13 bits—similar to the single-bit architecture used in previous asymmetrical digital subscriber line (ADSL) chips [1]. The architecture in this paper attenuates the in-band DAC error power by M^7 and thus is capable of obtaining 13-bit resolution with $M = 16$. Such a low oversampling ratio has a significant impact on power consumption and operating frequency. Actually, the modulator in this paper obtains one more bit resolution than that in [1] (both are in the same 0.7-μm CMOS technology), enhances the operating frequency by a factor of two, and reduces the power consumption by a factor of four.

This paper is organized as follows. The novel architecture and its behavior in the presence of circuit imperfections are analyzed in Section II. Section III describes a switched-capacitor implementation of such an architecture to be used in an ADSL modem requiring more than effective resolution at 2.2 MS/s. Last, the measurements taken from the modulator prototype fabricated in a 0.7-μm CMOS technology are summarized in Section IV.

II. Architectural Considerations

A. Modulator Architecture

The architecture in this paper belongs to the general class of the so-called *dual-quantization cascade* $\Sigma\Delta$ modulators [17]. Fig. 1 shows a conceptual block diagram for these modulators, where x is the overall analog input, x_j (for $2 \le j \le N$) is the input of the jth stage, e_j and y_j (for $1 \le j \le N$) represent the additive quantization error of the jth stage and the digital output signal of the jth quantizer, respectively, and y is the overall digital output. Note that the quantizers of the first $N-1$ stages are single bit, while the last-stage quantizer is multibit—a significant difference as compared to classical cascade architecture, where all quantizers are single bit [18]. To guarantee unconditional stability, each modulator in this general block diagram must be of either first-order or second-order type; the variables L_j (for $1 \le j \le N$) enclosed in the modulator blocks are used to indicate the order of the stages.

Fig. 1 shares the operating principle with classical cascade modulators. On the one hand, the quantization error generated at each stage is remodulated by the next one in the cascade. On the other hand, the quantization errors of the first $N-1$ stages are cancelled out through proper combination of the outputs y_j (for $1 \le j \le N$), exploiting the fact that these digital outputs contain a digital representation of the corresponding quantization error. After such cancellation, the output signal z-transform is given by

$$Y(z) = z^{-L_T}X(z) + d(1-z^{-1})^{L_T}E_N(z) - d(1-z^{-1})^{(L_T-L_N)}E_D(z) \quad (1)$$

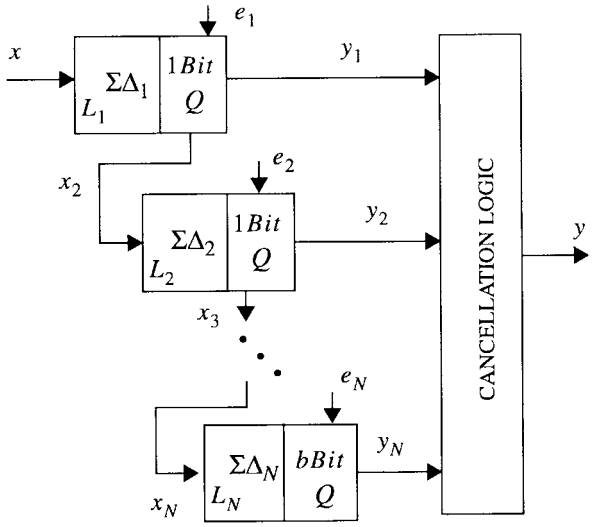


Fig. 1. Generic dual-quantization N-stage cascade $\Sigma\Delta$ modulator.

where $L_T \equiv L_1 + \cdots + L_N$. d is a number larger than unity—needed to compensate the scaling of the signal transferred from each stage to the next one—$E_N(z)$ is the last-stage quantization error, and $E_D(z)$ is the error induced by the last-stage DAC. Note that these errors cannot be cancelled out and hence influence the output. However, as (1) shows, their influence is attenuated by high-order filtering functions. In the case of the quantization noise, the order of such function is L_T—making its in-band error power inversely proportional to $M^{(2L_T+1)}$. In the case of the DAC error, the filter order is $(L_T - L_N)$—making its in-band error power inversely proportional to $M^{(2(L_T-L_N)+1)}$.

The latter feature has been exploited to relax the DAC linearity specification with neither correction nor calibration required, using a moderate oversampling ratio. In fact, based on the topology of Fig. 1, two dual-quantization $\Sigma\Delta$ modulator architectures have been already proposed in the literature [7], [16]. That proposed in [7], shown in Fig. 2(a) and referred to as 2-1$_{\rm mb}$, has $L_1 = 2$ and $L_2 = 1$, while the architecture proposed in [16], called 2-2$_{\rm mb}$, has $L_1 = 2$ and $L_2 = 2$. Their respective ideal expressions for the in-band error power are given by

$$P_{\text{2-1mb}} \cong d^2\left(\sigma_Q^2\frac{\pi^6}{7\text{M}^7} + \sigma_D^2\frac{\pi^4}{5\text{M}^5}\right)$$
$$P_{\text{2-2mb}} \cong d^2\left(\sigma_Q^2\frac{\pi^8}{9\text{M}^9} + \sigma_D^2\frac{\pi^4}{5\text{M}^5}\right). \quad (2a)$$

There, σ_Q^2 and σ_D^2 represent the total quantization error power and the DAC-induced error power, given respectively as

$$\sigma_Q^2 \cong \frac{1}{12}\left[\frac{\Delta}{(2^b-1)}\right]^2$$
$$\sigma_D^2 \cong \left(\frac{\Delta^2}{2}\right)\left(\frac{\text{INL}}{100}\right)^2 \quad (2b)$$

where Δ is the full-scale output range of the last-stage DAC and INL is the last-stage DAC integral nonlinearity expressed in % FS [19]. Note from (2a) that the DAC-induced error is ideally attenuated by M^5 in both cases. However, as will be

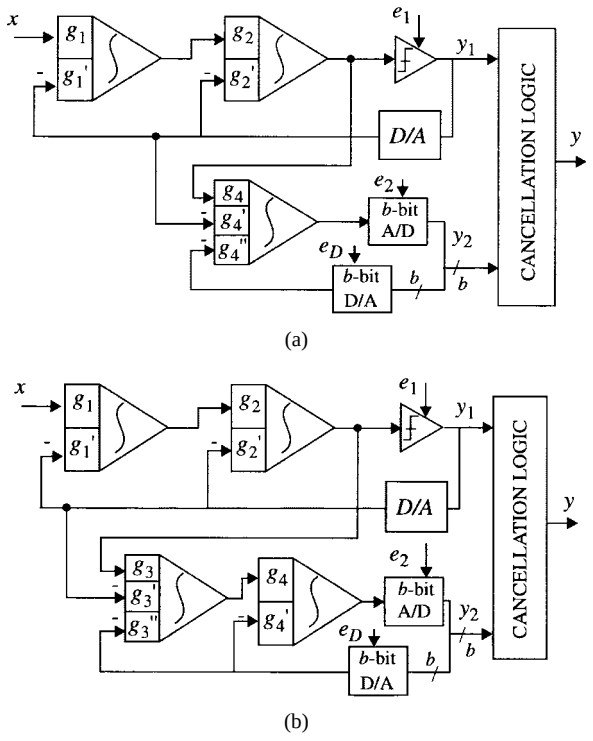


Fig. 2. Dual-quantization cascade $\Sigma\Delta$ modulators: (a) with the topology 2-1$_{\rm mb}$ and (b) with the topology 2-2$_{\rm mb}$.

shown later, this is not enough to obtain 13-bit resolution with M smaller than 24 in the targeted technology.

Fig. 3 shows the architecture used in this paper, which consists of a cascade of three stages (second order, first order, and first order) with multibit quantization in the third stage—henceforth referred to as 2-1-1$_{\rm mb}$. Note that the cancellation logic block (enclosed in the dashed rectangle) includes digital filters $H_k(z)$ (for $k = 1, 2, 3$) and scaling coefficients. Table I shows the transfer functions of these filters and the required relationships among the digital coefficients and analog integrator weights. These relationships have been obtained by imposing several conditions on the signal and the quantization error transfer functions, as it is needed to get the performance of a fourth-order $\Sigma\Delta$ modulator. First, the module of the signal transfer functions must be equal to unity; second, that of the last-stage quantization error must be proportional to $(1-z^{-1})^4$; third, those for the quantization errors in the first and the second stage must be equal to zero.

Assume that the relationships in Table I hold, and that the quantizer transfer functions are linearized so that every stage loop gain equals unity; the latter results in a quantizer gain of $1/(g_1'g_2)$ for the first stage, $1/g_3''$ for the second stage, and $1/g_4''$ for the third stage. Then, analysis yields the following expression for the z-transform of the output signal in Fig. 3:

$$Y(z) = z^{-4}X(z) + d_3\left(1-z^{-1}\right)^4 \cdot E_3(z) - d_3\left(1-z^{-1}\right)^3 E_D(z). \quad (3)$$

From here, the in-band error power is calculated as

$$P_{\text{2-1-1mb}} \cong d_3^2\left(\sigma_Q^2\,\frac{\pi^8}{9\text{M}^9} + \sigma_D^2\,\frac{\pi^6}{7\text{M}^7}\right). \quad (4)$$

Expression (3) shows the DAC error shaped by a third-order filtering function—a consequence of the presence of three integrators before the point where this error is injected. Consequently, the DAC in-band error power exhibits an inverse dependence on M^7—the key to maintaining relaxed DAC specifications with a low oversampling ratio. However, notice that this error power is amplified by the square of the digital coefficient d_3. Since the value of d_3 is determined by those of the analog coefficients g_1, g_2, g_3, g_4, and g_4'', the proper selection of the latter becomes crucial to realizing the potential advantages of the proposed architecture.

B. Selection of the Analog Coefficients

Every valid analog coefficient set must fulfill the relationships in Table I. Also, for feasible implementation, the following considerations must be taken into account.

- The level of the signal transferred interstages must be small enough to avoid overloading. These levels are equal to the reference voltages for a first-order modulator and approximately 90% of the reference voltages for a second-order modulator [2].
- The output swing of every integrator must be physically achievable. For switched-capacitor circuits, it means that the output swings, given as functions of the corresponding integrator weights and input level, must be inside the interval defined by the supply voltages.
- The value of the digital coefficient d_3, which amplifies the last-stage quantization error, must be minimized in order to maximize the DR.

Other practical considerations that help obtaining simpler circuits include the following.

- The digital coefficients should be 0, ± 1, or a multiple of 2 in order to simplify the circuitry for digital arithmetic.
- The gain of the last-stage quantizer—equal to $1/g_4''$, as previously mentioned—should not be larger than one to simplify the realization of the mb quantizer.

Taking into account the constraints imposed by the considerations above, optimum values of the analog coefficients have been obtained and are shown in Table II. With these values, the integrator output swing requirement is reduced to only the reference voltages. In addition, the input of the last stage, given by $g_4I_3(z) - g_4'Y_2(z)$ (see Fig. 3), is just $E_2(z)$. This means that the input of the last stage does not contain any trace of the modulator input signal and hence that the error due to the last-stage DAC nonlinearity does not distort the modulated signal.

C. About the Influence of Capacitor Mismatch and Finite Op-Amp Gain

In actual switched-capacitor (SC) implementations of Fig. 3, capacitor mismatch precludes exact realization of the analog coefficient values. Also, the actual SC integrator transfer function differs from the ideal one, given by $z^{-1}/(1-z^{-1})$, due to the effect of the finite op-amp gain. These nonideal mechanisms produce an incomplete cancellation of the first- and second-stage quantization errors, which hence manifest at

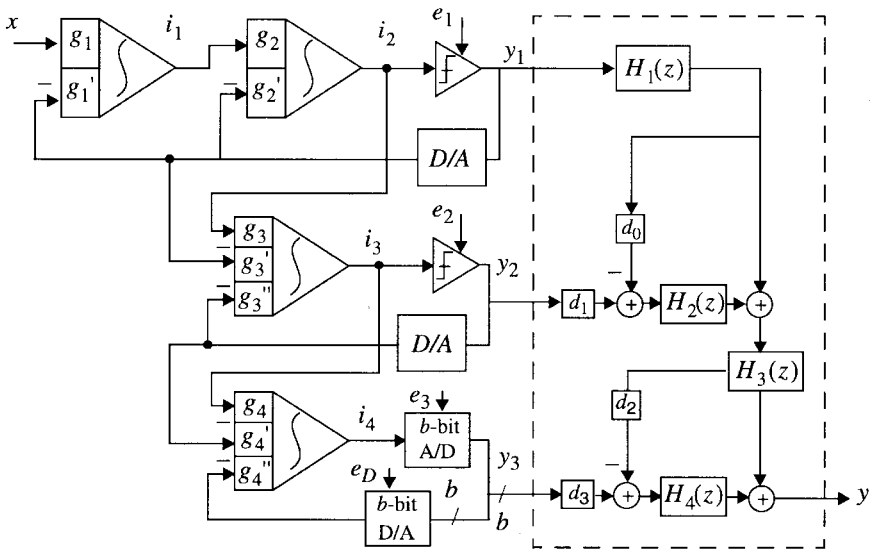


Fig. 3. Fourth-order, three-stage multibit (2-1-1_{mb}) $\Sigma\Delta$ modulator.

TABLE I
DIGITAL TRANSFER FUNCTIONS AND RELATIONSHIPS AMONG COEFFICIENTS IN FIG. 3

Digital	Digital/Analog	Analog
$H_1(z) = z^{-1}$	$d_0 = 1 - g_3'/(g_1g_2g_3)$	$g_1' = g_1$
$H_2(z) = (1-z^{-1})^2$	$d_1 = g_3''/(g_1g_2g_3)$	$g_2' = 2g_1'g_2$
$H_3(z) = z^{-1}$	$d_2 = \left(1 - \frac{g_3'}{g_1g_2g_3}\right)\left(1 - \frac{g_4'}{g_3''g_4}\right) \equiv 0$	$g_4' = g_3''g_4$
$H_4(z) = (1-z^{-1})^3$	$d_3 = g_4''/(g_1g_2g_3g_4)$	

TABLE II
ANALOG AND DIGITAL COEFFICIENTS IN FIG. 3

g_1	0.25	g_3'	0.375	d_0	-2
g_1'	0.25	g_3''	0.25	d_1	2
g_2	0.5	g_4	4	d_2	0
g_2'	0.25	g_4'	1	d_3	2
g_3	1	g_4''	1		

the modulator output, and place a practical constraint on the mb quantizer resolution. Thus, increasing such a resolution above the limit where the in-band error is dominated by the uncanceled quantization errors does not improve the overall modulator performance. The value of this limit, which depends on the circuit imperfections, can be evaluated using behavioral simulation [19].

Fig. 4 shows the simulated signal-to-(noise + distortion) ratio (SNDR) of the 2-1-1_{mb} modulator as a function of the number of bits in the last quantizer for half-scale input amplitude. The figure includes the ideal curve and four nonideal curves obtained for different values of the standard deviation of the integrator weight (sigma); these nonideal curves correspond to the worst case performance, obtained as mean $-$ 3-sigma. The values of the integrator weights that lead

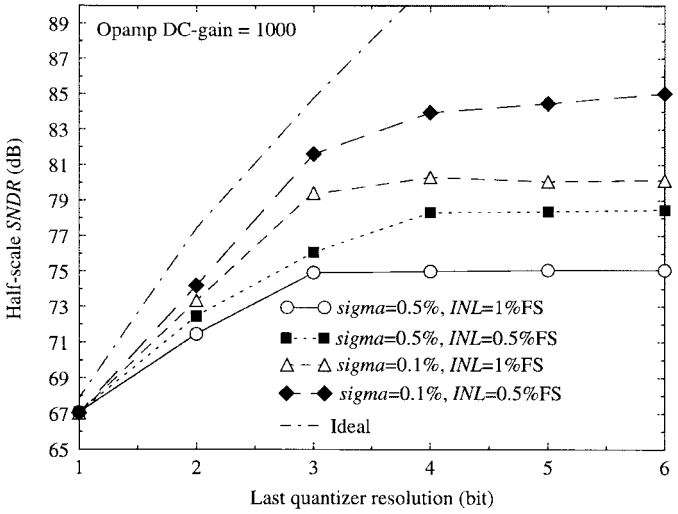


Fig. 4. SNDR versus last quantizer resolution in presence of nonidealities for the 2-1-1_{mb} modulator.

to the presented results were obtained through Monte Carlo simulation with the tool in [19]. Other simulation conditions are: op-amp dc gain = 1000, $M = 16$, and last-stage DAC nonlinearity (INL) = 0.5 and 1% FS. Note that all the nonideal curves saturate at around three bits. Hence, further increasing the last-quantizer resolution beyond this limit does not result in significant improvement of the overall modulator resolution. Based on that, the chip proposed herein employs a 3-bit quantizer in the last stage of the modulator.

Using a 3-bit quantizer permits us to attain 79-dB SNDR with $M = 16$ (for sigma = 0.1%, INL = 1% FS), which renders the performance of the proposed architecture superior to those of previous cascade dual-quantization modulators. To show that, in Fig. 5 we have depicted the half-scale SNDR (for sigma = 0.1%, op-amp dc gain = 1000, and INL = 1% FS) as a function of the oversampling ratio for the 2-1-$1_{3\text{-bit}}\Sigma\Delta$ modulator. Also depicted are the corresponding curves for

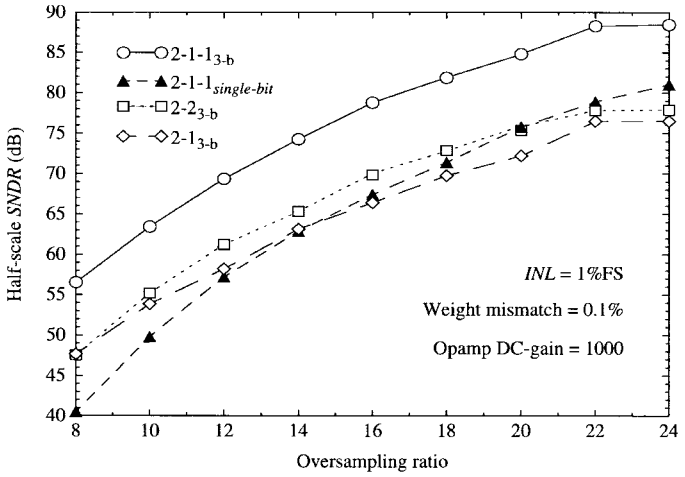


Fig. 5. Half-scale SNDR as a function of the oversampling ratio in the presence of circuit imperfections.

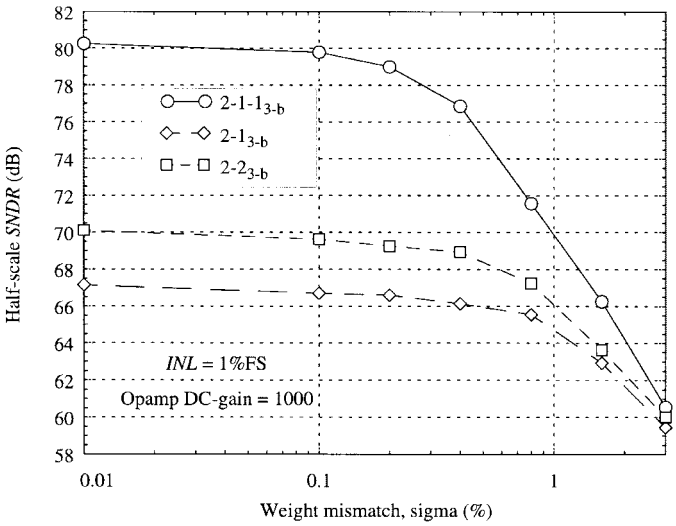


Fig. 6. Half-scale SNDR versus weight mismatch including 1% FS INL and op-amp dc gain $= 1000$.

the 2-1$_{3\text{-bit}}$ modulator [7] and the 2-2$_{3\text{-bit}}$ modulator [16].[1] For completeness, the curve for the 2-1-1$_{\text{single-bit}}$ modulator [8], [20] has been also added. As can be seen, the proposed architecture outperforms previous ones. Particularly, note that the 2-1-1$_{\text{single-bit}}$ modulator requires $M \geq 24$ to attain performance similar to the new one. It can be designed with $M = 24$; however, apart from the increased sampling frequency, such a nonpower-of-two oversampling may complicate the design of the digital filtering, thus increasing the overall power consumption.

For further illustration of the advantages of the new architecture, Fig. 6 depicts the half-scale SNDR of the 2-1-1$_{3\text{-bit}}$, 2-2$_{3\text{-bit}}$, and 2-1$_{3\text{-bit}}$ modulators as a function of the weight mismatch for $M = 16$ and including circuit imperfections. Note that the three curves converge as the mismatch increases. However, even for sigma $= 0.5\%$, the SNDR of the 2-1-1$_{3\text{-bit}}$ is 6.5 and 9 dB larger than that of the 2-2$_{3\text{-bit}}$ and 2-1$_{3\text{-bit}}$ modulators, respectively.

III. Switched-Capacitor Implementation

Choosing the modulator architecture is the first step of the modulator design process. Starting from this step, the design proceeds first through the calculation of specifications for the building blocks (modulator sizing), then through the calculation of the sizes of transistors and passive components within these blocks (cell sizing), and finally through the drawing of a layout. In our case, the phases of modulator sizing and cell sizing have been completed with the help of a set of computer-aided design tools specific for the design of SC $\Sigma\Delta$ modulators [19].

A. Modulator Sizing

The procedure used for modulator sizing involves seeking an optimum configuration that, on the one hand, fulfills the intended specifications and, on the other, complies with the error contributions of the SC circuitry (i.e., defective settling, nonlinearity, thermal noise, etc.) [19]. Table III shows the results obtained for 12.5-bit, 2.2-MS/s, 4-V input full scale. Besides the building block specifications, the most significant in-band noise and distortion contributions are summarized at the bottom of Table III. Note that, as a result of the optimization procedure, the effective resolution obtained fits well with the specification.

The following observations can be made by looking at Table III.

- Because of the large insensitiveness to the mb DAC error, the DAC linearity requirement is only 2.8% FS [equivalent to 0.2 least significant bit (LSB) of three bits]—achievable using simple circuitry for the 3-bit ADC and DAC.
- The low oversampling ratio results in a clock frequency of only 35.2 MHz and hence in a moderate op-amp transconductance of 4.2 mA/V[2]—much smaller than that required for the 2-1-1$_{\text{single-bit}}$ architecture, where the clock frequency must be of at least 52.8 MHz ($M = 24$). Because of the square-root dependence of transconductance on the bias current, the smaller transconductance is expected to encompass a significant reduction of power consumption as compared with the 2-1-1$_{\text{single-bit}}$—confirmed by our experimental results.
- Besides quantization noise, the main error source is due to clock jitter. This is foreseeable because jitter noise depends on the signal frequency [21] and becomes more important as the frequency increases. Here, we have assumed that the standard deviation of the clock period is 0.1 ns (see Table III). Nevertheless, this estimation is, to a point, arbitrary because such value strongly depends on how the clock signal is generated. In the final prototype, the clock signal is externally supplied through a high-quality source, so we do not expect the jitter to be so

[1] The set of integrator weights used in these architectures is optimized for maximum DR. These optimized coefficients feature larger DR than those proposed by the authors in [7] and [16].

[2] We use this instead of the op-amp gain-bandwidth product because the load capacitor changes depending on the operating conditions. With this transconductance and assuming 6.1-pF equivalent load (the maximum that op-amps OA1 and OA2 may have), the gain-bandwidth product is 109.6 MHz.

TABLE III
MODULATOR SIZING RESULTS

OPTIMIZED SPECS FOR:		12.5-b@2.2MS/s
Modulator	Topology	2-1-1$_{mb}$
	Sampling frequency	35.2MHz
	Oversampling ratio	16
	Reference voltages	positive +2V, negative −2V
Integrators	Sampling capacitor	0.5pF
	Unitary capacitor	0.5pF
	Load capacitor	≤ 2.5pF
	Capacitor non-linearity	≤ 25p.p.m/V *
	MOS switch-ON resistance	700Ω
	Jitter (sigma of the clock period)	≤ 0.1ns
Opamps	DC-gain	≥ 60dB
	DC-gain non-linearity	≤ 25%V^{-2}
	Transconductance	4.2mA/V
	Maximum output current	≥ 0.63mA
	Differential output swing	≥ 4.0Vpp
	Input noise	≤ 3nV/Hz$^{1/2}$
	Parasitic input capacitor	≤ 1.5pF
Comparators	Hysteresis	≤ 50mV
	Resolution time	≤ 7ns
D/A converter	Resolution	3 bit
	Non-linearity (*INL*)	≤ 2.8%FS (0.2LSB_{3B})
RESOLUTION & NOISE POWER CONTRIBUTIONS		
Dynamic range:		78.65dB (12.77b)
Quantization noise		-78.1dB
Thermal noise		-92.4dB
Incomplete settling noise		-88.7dB
Jitter noise		-80.7dB
Harmonic distortion		-88.6dB

*. Significant only for single-ended implementations

large. In that case, if we neglect the influence of the jitter noise contribution, the attainable DR is 80.3 dB (13 bit).

- Because thermal noise is not the dominant noise contribution, it is possible to reduce the value of the sampling capacitor in the first integrator, which has significant influence on the reduction of the op-amp transconductance requirement. Our optimization procedure returned a value 0.5 pF for this capacitor; the same value was used for the unitary capacitor used to layout the capacitor ratios in a common centroid structure.
- The contributions of other error mechanisms, as incomplete integrator settling, or distortion caused by either the op-amp open-loop gain nonlinearity or the capacitor nonlinearity (grouped into harmonic distortion contribution), are well below the limit imposed by the effective modulator resolution.

B. Switched-Capacitor Schematic

Fig. 7 shows the fully differential SC schematic for the analog part of the modulator. The first stage is obtained by connecting two SC integrators: the first one with a single input branch and the second one with two input branches. The single-bit quantizer is realized by a differential comparator based on a regenerative latch (described later). The feedback signal is built by two AND gates that connect the sampling capacitor of each integrator to either $+1$ or -1 V depending on the comparator output. Since the circuit is fully differential, the resulting reference voltage is ± 2 V.

The second stage incorporates an integrator with three input branches, required to implement the three different weights: g_3, g_3', and g_3''. The same architecture is used for the third-stage integrator whose output drives a full-flash 3-bit ADC. The third-stage loop is closed through a 3-bit DAC implemented with a resistive ladder. To reduce the equivalent load of the op-amps labeled OA2, OA3, and OA4 in Fig. 7 and hence their power consumptions, the weights g_2, g_3, and g_4 have been distributed among two or three branches.

The modulator operation is controlled by two nonoverlapped clock phases. The integrator input signals are sampled during phase ϕ_1. Then the algebraic operations are performed during phase ϕ_2, and the results are accumulated in the feedback capacitor of each integrator. The comparator and flash ADC are activated just at the end of phase ϕ_2 (controlling the strobe

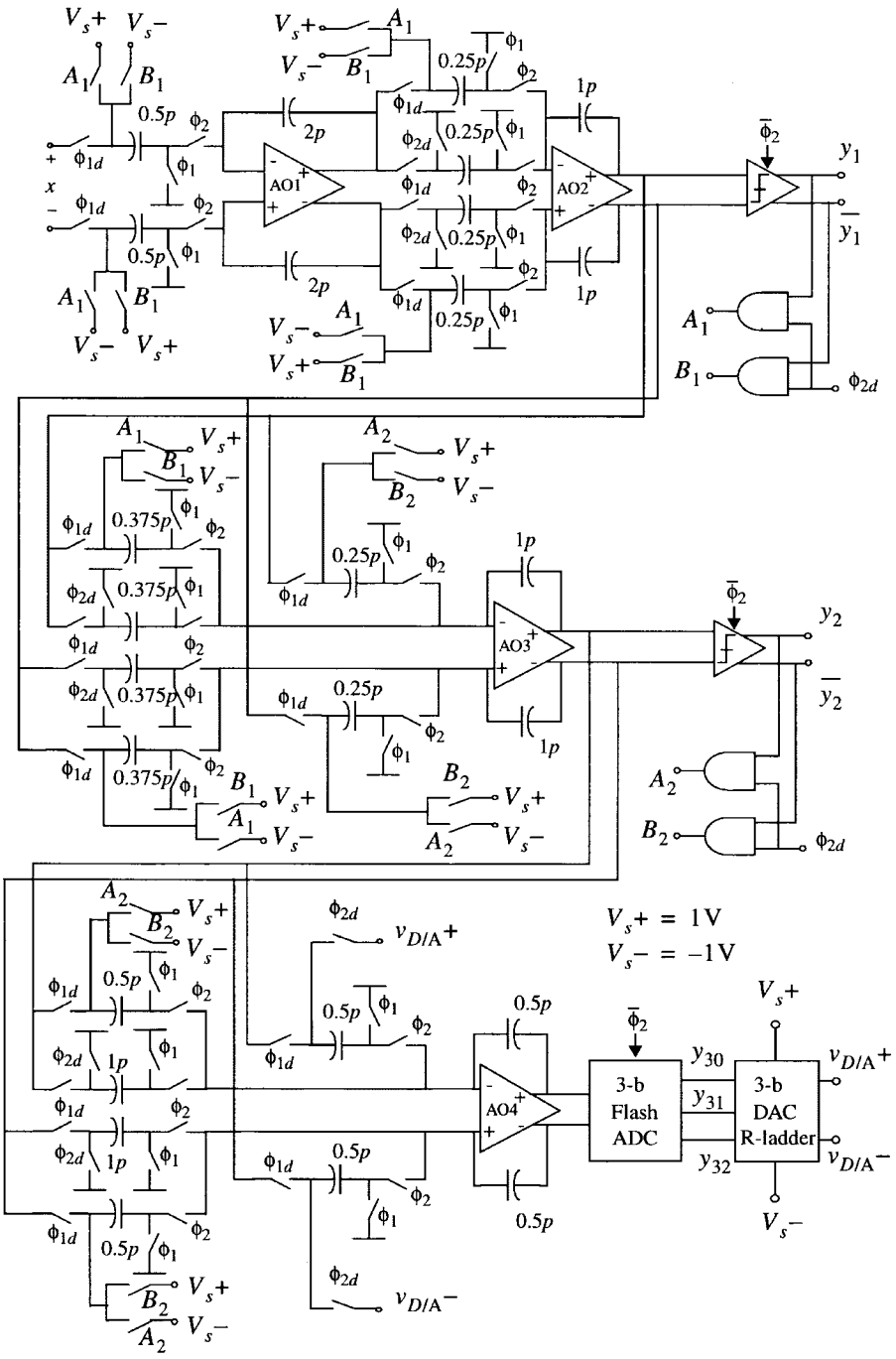


Fig. 7. Switched-capacitor implementation of the analog part of the 2-1-$1_{\rm mb}$ $\Sigma\Delta$ modulator.

input with $\overline{\phi}_2$) to avoid any possible interference due to the transient response of the integrator outputs in the beginning of phase ϕ_1. This timing guarantees a single delay per clock cycle. To attenuate the signal-dependent clock feedthrough, a set of slightly delayed versions of the two phases, ϕ_{1d} and ϕ_{2d}, is provided [22].

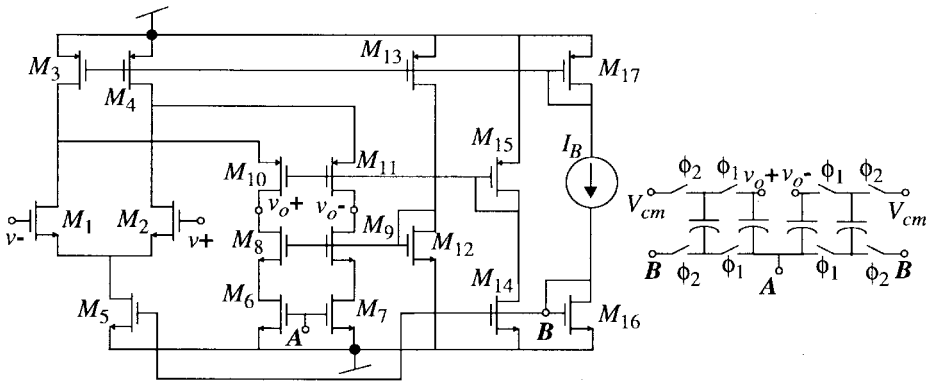
C. Building Block Design

1) Op-Amp: Fig. 8(a) shows the op-amp schematic. It consists of a fully differential folded-cascode operational transconductance amplifier (OTA) (transistors M_1–M_{11}) and a biasing stage (transistors M_{12}–M_{17}). The common-mode feedback net is based on the SC circuit of Fig. 8(b). Such a dynamic common-mode feedback circuit yields smaller power consumption than its static counterparts for high-frequency operation.

Table IV shows an estimation of the equivalent load for each op-amp. It has been calculated as

$$C_{\rm eq} = C_i + C_p + C_l[1 + (C_i + C_p)/C_o] \tag{5}$$

where C_i and C_o are the sampling and feedback capacitors, respectively, and C_p and C_l are the parasitics at the amplifier input and output, respectively. The latter are significant because in the intended technology, the capacitors are formed



(a) (b)

Fig. 8. Fully differential folded-cascode OTA: (a) amplifier core and (b) common-mode feedback SC circuit; all capacitors equal 0.2 pF.

TABLE IV
ESTIMATION OF THE EQUIVALENT LOAD OF EACH AMPLIFIER

Amplifier	phase ϕ_1	phase ϕ_2	Units
1	6.1	3.95	pF
2	5.8	3.25	pF
3	7.5	4.55	pF
4	3.25	11.575	pF

TABLE V
AMPLIFIER WIDTH/LENGTH (μm) AND BIAS CURRENT

Trans.	AO1 and AO2	AO3 and AO4	Trans.	AO1 and AO2	AO3 and AO4
$M_{1,2}$	492/1.2	598.8/1.2	M_{12}	2.3/1.2	4.5/1.2
$M_{3,4}$	137.7/1.2	165/1.2	M_{13}	13.8/1.2	16.5/1.2
M_5	331.2/1.2	300/1.2	M_{14}	18.2/1.2	26.2/1.2
$M_{6,7}$	182/1.2	165/1.2	M_{15}	3.1/1.2	7.5/1.2
$M_{8,9}$	19.6/1.2	48/1.2	M_{16}	66.1/1.2	30/1.2
$M_{10,11}$	142.8/1.2	300/1.2	M_{17}	26.2/1.2	15.7/1.2
			I_B	149µA	143µA

by poly over N-diffusion. Since the latter layer is directly on the P-type substrate, a large diffusion capacitor is associated to the bottom plate of each capacitor in Fig. 7. To cope with such parasitics, which amount to around 50% of the nominal capacitor values, the power consumption per op-amp has to be increased. Note that in Table IV, $C_{\rm eq}$ is considerably larger for OA4 during phase ϕ_2 because during this phase, the output of this op-amp drives the 3-bit ADC. Note that the total parasitic capacitance of the seven input capacitors contributes to C_l in (5) and hence its contribution to $C_{\rm eq}$ is amplified by $1 + (C_i + C_p)/C_o$, which is around five. This problem can be overcome by inserting buffers at the last-integrator output [7]. However, these buffers, which also should be placed between the resistor string and the comparator stage in order to compensate for the buffer gain error and nonlinearity, require an extra power budget. Also, their usage may reduce the useful output range. Another strategy is using two op-amps with different driving capabilities: one for the first two integrators, capable of driving capacitors between 4 and 6 pF; and another with larger driving capability (up to 12 pF) for the third and fourth integrators. We adopted this last strategy because it reduces the power budget and improves the performance. Table V shows the transistor sizes for these two op-amps obtained with the sizing tool in [19]. The simulation results of their corresponding extracted layouts are shown in Table VI. Note that the supply current of the larger op-amp is approximately twice that of the smaller. Although the latter has a phase margin of only 53° under worst case loading conditions, behavioral simulations using a two-pole model for the op-amp with the tool presented in [19] show that this is enough for the intended modulator specifications.

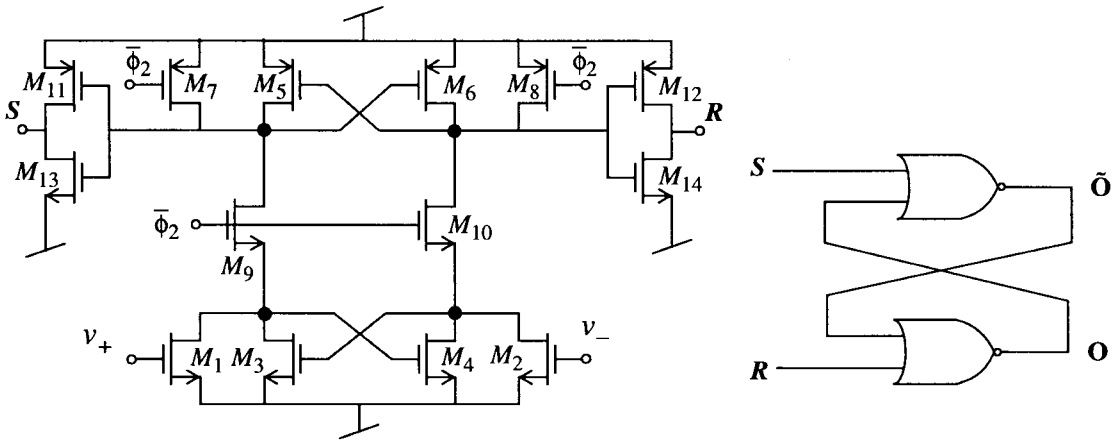
TABLE VI
SIMULATION RESULTS FOR THE AMPLIFIERS

Specs.	AO1 and AO2	AO3 and AO4	Units
Open-loop DC gain	75.7	75.4	dB
Trasconductance	4.87	7.4	mA/V
GB	151(4pF)	93 (12pF)	MHz
Phase margin	53 (4pF)	70.8 (12pF)	°
Input white noise	3.1	2.4	nV/√Hz
Input flicker noise (DC-1.1MHz)	11	-	μV_{rms}
Differential output swing	5.6	5.3	V
Maximum output current	0.7	1.35	mA
Supply current	1.82	3.4	mA

Simulated input flicker noise of the first integrator yields 11-μV rms (−99 dB) after integration in the signal band (from dc up to 1.1 MHz)—a value well below the limit imposed by the modulator resolution. Consequently, no low-frequency noise-compensation mechanism is needed.

2) Single-Bit Comparator: Note from Table III that the comparator hysteresis requirement is not very demanding. On the other hand, the resolution time should be a quarter of the sampling period (7 ns). A simple regenerative latch without amplification front-end can hence be used to minimize power consumption. Fig. 9 shows its schematics [23], whose sizing has been realized using the tool in [19] to fulfill the specifications with minimum possible power consumption. Transistor sizes and simulation results are given in Tables VII and VIII, respectively.

3) Multibit ADC and DAC: The low sensitivity of the 2-1-$1_{\rm mb}$ architecture to the imperfections of the DAC circuitry,



(a) (b)

Fig. 9. Comparator: (a) regenerative latch and (b) NOR flip-flop.

TABLE VII
REGENERATIVE LATCH SIZES IN μm

Trans.	W/L	Trans.	W/L
$M_{1,2}$	3/4	$M_{7,8}$	2.2/0.7
$M_{3,4}$	3/4	$M_{9,10}$	2.2/0.7
$M_{5,6}$	8/3	$M_{11\text{-}14}$	2.2/0.7

TABLE VIII
SIMULATION RESULTS FOR THE COMPARATOR

	Simulated	Units
Hysteresis	< 10	mV
TPLH	6	ns
TPHL	6.5	ns
Average power	0.42	mW

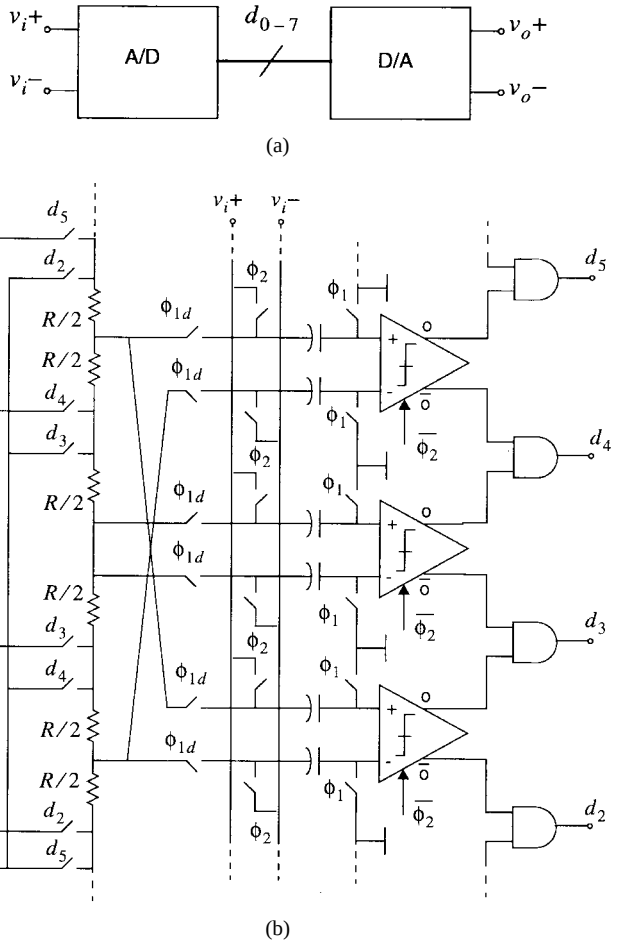


Fig. 10. (a) Block diagram of the A/D/A converters and (b) partial view of their SC implementations.

and even more to those of the ADC, allows use of very simple topologies for both blocks with consequent power savings. With respect to the 3-bit ADC, a flash architecture is feasible because data have to be coded into a small number of bits at the clock rate (35.2 MHz). Fig. 10 shows three of the seven comparison stages of the converter. The classical architecture of these stages has been slightly modified [7] to enable the comparison of differential signal v_i and reference v_r voltages (generated through a resistor string), using two capacitors for computing the difference $(v_{i+} - v_{i-}) - (v_{r+} - v_{r-})$. The value of the sampling capacitors is 0.5 pF. At the end of phase ϕ_2, the comparator is activated for evaluating the sign of the difference. All the comparators are identical to that used in the first- and second-stage single-bit quantizer. In practice, without a preamplification stage, such a comparator may provide a resolution not much better than 50 mV, which is enough not to degrade the performance taking into account that the value of the LSB is 571 mV. However, if the LSB decreases, as would happen if the gain of the ADC had to be increased, the hysteresis inherent in the latched comparators might become a problem. In that case, more complex topologies with preamplification stages should be used, with a considerable increase in power consumption. That is the reason why it is interesting to keep the ADC gain equal to unity. After the comparator array, eight AND gates generate a 1-of-8 code, which is translated to binary by a ROM memory (not shown) whose outputs are buffered out of the chip.

To implement the DAC, the 1-of-8 code is used to select through analog switches the voltages generated in the same resistor string used to generate the reference voltages for the ADC, which also contributes to reduce the power consump-

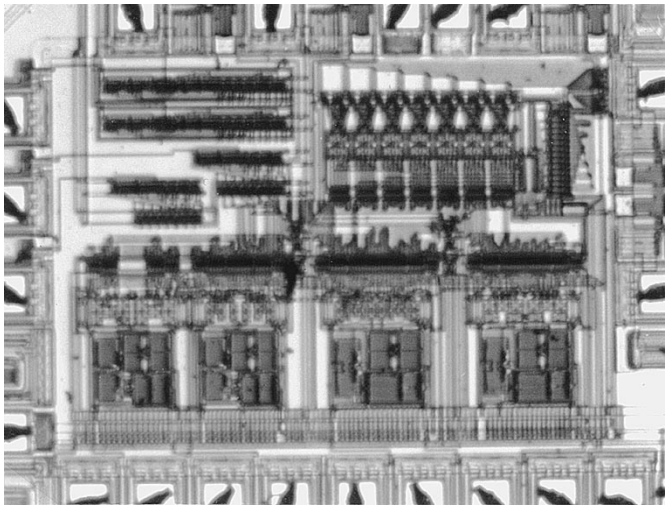


Fig. 11. Microphotograph of the 2-1-$1_{\rm mb}$ in 0.7-μm CMOS technology (area $= 1.3$ mm^2).

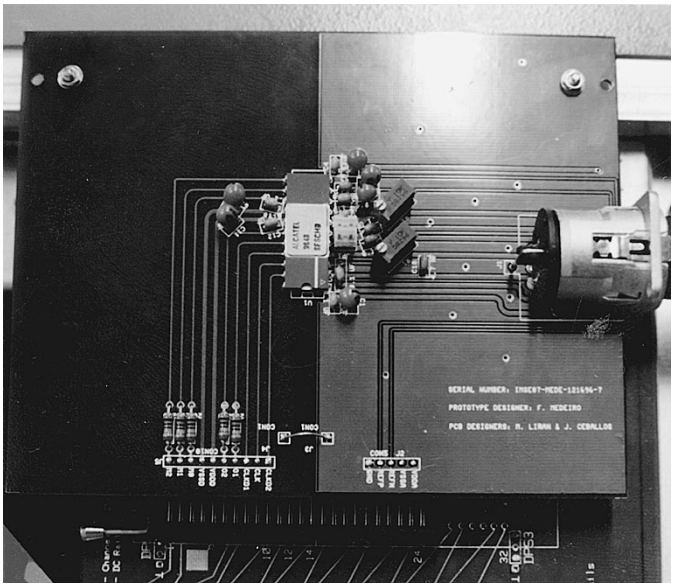


Fig. 12. Two-layer printed circuit board used for testing.

tion. The resistors in the ladder are $R = 307.5\,\Omega$; this value is low enough to ensure that the settling error of the voltages in the ADC input capacitors (during phase ϕ_1) and the fourth integrator input capacitors (during phase ϕ_2) are not excessive. All switches are complementary with aspect ratio 4.4/0.7 μm for both NMOS and PMOS transistors.

The INL was measured for several samples of the ADC and DAC integrated separately, working at 50 MS/s. In both cases, the INL is smaller than 1.4% FS (0.1 $\text{LSB}_{\text{3-bit}}$), which according to the requirement 2.8% FS (0.2 $\text{LSB}_{\text{3-bit}}$) is enough not to degrade the performance of the overall modulator.

IV. Experimental Results

Fig. 11 shows a microphotograph of the complete modulator, including the clock phase generator, fabricated in a 0.7-μm CMOS technology. The prototype occupies 1.3 mm^2 without the pads and dissipates 55 mW operating at 5-V supply. The two-layer test board shown in Fig. 12 was used to characterize the modulator. It includes separate analog and digital ground planes, decoupling capacitors at the biasing and reference traces, a first-order anti-aliasing filter for the input with 2-MHz, -3-dB frequency, and impedance coupling termination at the digital traces in order to reduce the switching noise. The performance of the modulator was evaluated using a high-quality programmable source to generate the input signal and a digital data-acquisition unit to generate the clock signal and to acquire the bitstreams of the first, second, and third stages of the cascade. The same unit controlled the supply and reference voltages. After the acquisition, performed automatically by controlling the test setup through proprietary C routines, data were transferred to a workstation to perform the digital postprocessing using MATLAB. The digital filtering was performed with a fifth-order Sinc filter, implemented by software.

Fig. 13 shows the unfiltered modulator output spectrum obtained by processing 65 536 consecutive output samples at a 35.2-MHz clock rate. The shaded line is the cumulative noise power. The modulator input consisted of a sinusoid of

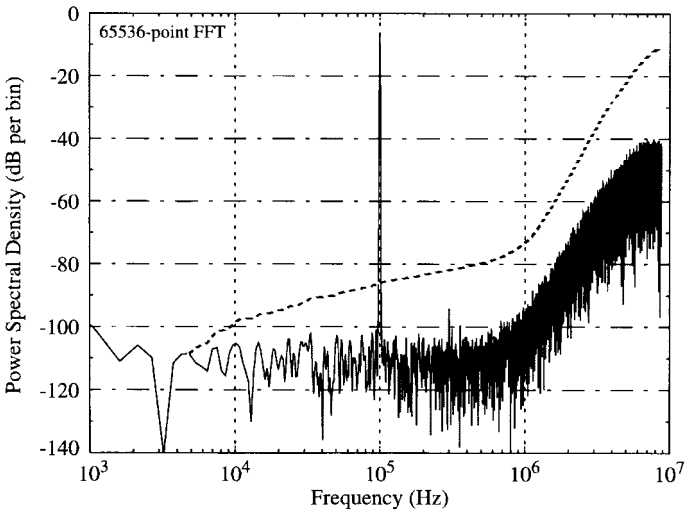


Fig. 13. Measured output spectrum at 35.2-MHz clock rate for a 100-kHz, 2-$V_{\text{p-p}}$ input signal.

amplitude 1 V and frequency of 100 kHz. Note that the noise is nearly white (no noise shaping is observed) up to 700 kHz. We found that this value strongly depended on clock frequency and on the supply voltage of the digital output buffers—the noisiest digital blocks. Thanks to the supply being provided separately for the digital and analog part of the chip, we were able to significantly improve the modulator performance at the nominal sampling frequency by scaling down the supply voltage of the digital output buffers up to 3 V. However, this supply reduction is also applied to the internal logic, so that it directly affects to the voltage applied to the switches, thus limiting their linearity. This might be the cause of the presence of a third-order harmonic distortion. Nevertheless, note that the measured distortion in Fig. 13 agrees with that predicted in Table III.

Fig. 14 shows the SNDR in the base band (from dc to 1.1 MHz) as a function of the input level (fractional input with

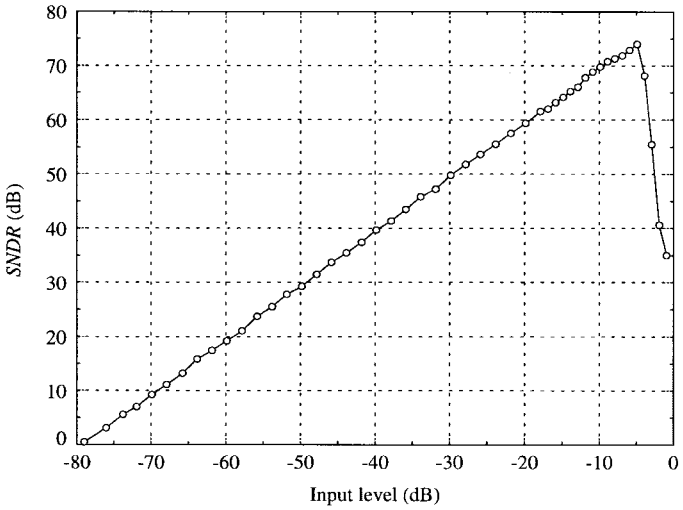
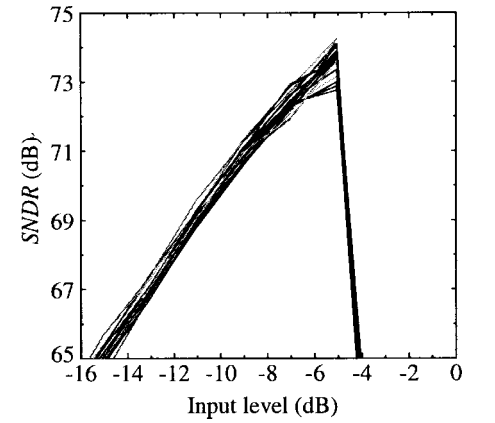
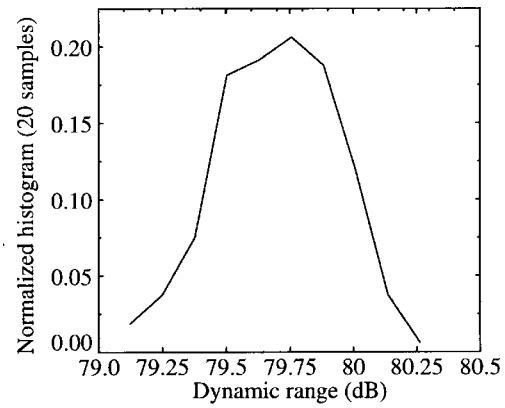


Fig. 14. Measured in-band SNDR as a function of the input level.



(b)



(a)

Fig. 15. (a) Measured SNDR curves for 20 modulator samples and (b) DR histogram.

respect to the reference voltage [7], so that an input level of 0 dB represents a sine wave whose peak-to-peak amplitude is equal to the modulator full scale = 4-V differential). Data were measured at a 35.2-MHz clock rate with a sinusoidal input at 100 kHz and level varying from −79 to 0 dB. The maximum value of the SNDR is 74 dB, obtained for a −4.9-dB input level. The DR is 79.5 dB. Actually, these figures

TABLE IX
SUMMARIZED PERFORMANCE OF THE 2-1-1_{mb} MODULATOR

Sampling frequency	35.2	MHz
Digital output rate ($M = 16$)	2.2	MS/s
DR	79.5	dB
Effective resolution	12.9	bit
SNDR peak	74	dB
Reference voltages	±2	V
Power consumption (5-V supply)	55	mW
Active area	1.3	mm^2

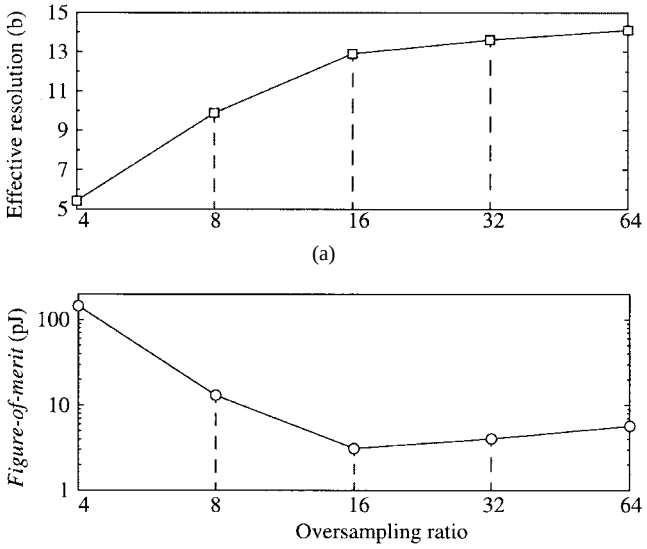


Fig. 16. (a) Measured effective resolution and (b) value of the FOM as a function of the oversampling ratio, for a constant sampling frequency equal to 35.2 MHz.

are reduced 3 dB after brick-wall filtering, due to the noise attenuation of the Sinc filter at frequencies close to the end of the signal band.

Fig. 15(a) shows the large-input region of the SNDR plot for 20 samples of the modulator prototype. The dispersion of the curves due to the effect of integrator weight mismatch can be seen. As shown in Fig. 15(b), the DR distribution seems to be Gaussian with 79.7 dB mean and 0.25 dB standard deviation.

The performance of the modulator is summarized in Table IX. Such a performance yields a value of 3.3 pJ for the figure of merit (FOM) defined in [24]

$$\text{FOM} = \frac{\text{power(W)}}{2^b \cdot \text{DOR(S/s)}} \tag{6}$$

with DOR being the digital output rate, which places this modulator between those with the lowest value of said figure reported until now [25]. The FOM as well as the effective resolution have been evaluated for several values of the oversampling ratio, for a constant sampling frequency equal to 35.2 MHz. The results are shown in Fig. 16. Note that, as shown in Fig. 16(a), for $M = 16$, the effective resolution is just in the border between the quantization-noise limited region, characterized by a slope of 4.5 bit/octave in the resolution-oversampling ratio plane; and the white-noise

TABLE X
SUMMARY OF PUBLISHED HIGH-FREQUENCY CMOS $\Sigma\Delta$ MODULATORS AND THEIR FOM's

	DR (b)	*DOR* (kS/s)	Modulator Power (mW)	Process / Supply	Architecture	*FOM* (pJ)
Modulator here	12.9	2200	55	0.7μm CMOS / 5V	Cascade 2-1-1, 3b	3.3
[26] (1993)	15.7	320	65	1.2μm CMOS / 5V	Cascade 2-1	3.9
[8] (1997)	14.8	2000	230	1μm CMOS / 5V	Cascade 2-1-1	4.0
[7] (1991)	12	2100	41	1μm CMOS / 5V	Cascade 2-1, 3b	4.8
[9] (1997)	14.5	2500	435	0.6μm CMOS / 5-3V	2nd-order, 5b / 12-b pipeline cascade	7.5
[5] (1994)	14.7	200	40	1.2μm CMOS /5V	Cascade 2-2-2 (tri-level)	7.7
[4] (1996)	13.7	500	58	1.2μm CMOS / 5V	4th-Order, 4b	9.0
[1] (1995)	12	1540	250*	0.7μm CMOS / 5V	Cascade 2-1-1	39.6

*. Estimated

limited region, where the slope becomes only 0.5 bit/octave. Also, Fig. 16(b) shows that, as a consequence of the intensive use of optimization at the architectural as well as the cell level, the minimum value of the FOM is obtained for the nominal value of the oversampling ratio $M = 16$. Thus, although it is possible to obtain either more resolution (for a larger value of M) or a larger signal bandwidth (for a lower value of M), the value of the FOM increases as well.

For comparison purposes, the value of the FOM, together with the information needed to calculate it, is given in Table X for some representative medium/high-frequency IC modulators. It is worth mentioning that with the exception of the modulator in [4], which uses a fourth-order, single-loop, 4-bit architecture, all these modulators use some form of cascade architecture, with either single-bit or multibit quantization. In particular, that in [9] uses a cascade of a 5-bit-quantization, second-order loop, and a 12-bit pipeline ADC. This strategy has allowed obtainment of the largest DOR but with the price of large power dissipation, which leads to a higher value of the FOM.

V. CONCLUSIONS

Because they provide high DR with low oversampling ratio, high-order multibit quantization architectures are natural candidates to implement very high-speed $\Sigma\Delta$ modulation-based ADC's. The main drawback of such architectures—tendency to instability and large dependence on the multibit DAC linearity—can be solved using a cascade (multistage) modulator with multibit quantization only in the last stage. Based on that idea, a three-stage, 2-1-1 cascade $\Sigma\Delta$ modulator including multibit quantization in the third stage and single-bit quantization in the first two stages is suggested because it shows lower sensitivity to the DAC error than those previously reported. Behavioral simulations show that, even in the presence of circuit imperfections (most limiting are integrator leakage and weight mismatching), 3-bit quantization is feasible.

The proposed architecture has been used to implement an ADC for an ADSL copper-wire telecom system requiring more than 12 bits at 2.2 MS/s. The low sensitivity of the modulator to the circuit imperfections, especially to those of the last-stage ADC and DAC, allows us to use very simple circuitry, thus decreasing power dissipation. Experimental results, 13-bit DR at 2.2 MS/s, dissipating 55 mW, demonstrate the viability of using advanced $\Sigma\Delta$ modulation-based ADC's for telecommunications.

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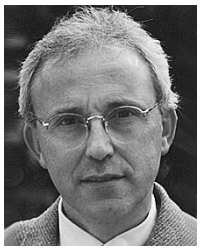

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