A New Nonlinear Time-Domain Op-Amp Macromodel Using Threshold Functions and Digitally Controlled Network Elements

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Abstract—**In this paper we present a new general-purpose nonlinear macromodel for the time-domain simulation of integrated circuit operational amplifiers (op amps), either bipolar or MOS. We can mention three main differences between this macromodel and those previously reported in the literature for the time domain. First, all the op-amp nonlinearities are simulated using threshold elements and digital components, thus making the macromodel well suited for a mixed electrical/logical simulator. Second, the new macromodel exhibits a superior performance in those cases where the op amp is driven by a very large signal. Finally, the macromodel is advantageous in terms of CPU time. Several examples are included illustrating all of these advantages. The main application of this macromodel is for the accurate simulation of the analog part of a combined analog/digital integrated circuit.**

I. INTRODUCTION

As digital/analog integrated systems are becoming more and more popular, the demand for simplified but still accurate models which handle analog subsystems is continuously growing. Analog chip designers ask for models that allow them to combine as much accuracy as possible with a maximum simulation speedup.

Resorting to macromodels instead of device-level models is a widely used strategy that allows the designer to reduce the high computation time required when simulating complex systems. This is particularly true in many analog applications where the basic component is the operational amplifier (op amp). Op amps are usually composed of 15–30 transistors and, in circuits incorporating tens (or even hundreds) of them, considerable savings in time can be obtained using a macromodel. A secondary advantage of macromodels is that determining the parameters of every op-amp circuit component (transistor, capacitor, etc.) is not needed. Since macromodels only reflect the input–output behavior of the op amp, the macromodel parameters can be calculated from measurements made at the op-amp terminals. Finally, it is worthwhile to mention that macromodels allow us to derive meaningful design equations in many practical cases where device-level models are senseless due to their inherent high complexity.

Several op-amp macromodels have been reported in the past [1]–[18], [21], [22]; but only some are intended for nonlinear transient simulation [1]–[7], [18], [21], [22], the others being exclusively valid or intentionally oriented for the frequency domain [8]–[17]. However, two points must be put in the foreground with respect to these time-domain macromodels. First, they have been developed at a circuit level, this fact rendering them specially suited for electrical simulators (like SPICE2 [23]) but not adequate for timing or switch-level programs. Second, some of them exhibit specific problems in those cases where very large amplitude driving signals are involved [19]. In particular, these limitations have considerable influence in nonlinear applications, such as oscillators, A/D converters, etc. In modern-day integrated systems, where digital and analog circuits coexist on the same chip, both drawbacks become more and more important. On the one hand, a switch-level simulator would be able to handle this kind of complex system in a more efficient way; on the other hand, those systems have to be accurately analyzed although they are very nonlinear in nature.

This paper addresses both points. Section II gives a critical view of op-amp macromodels in the time domain. Based on those criticisms, Section III develops the basis for a new macromodel suited for timing simulators. Finally, Section IV presents results showing the relative performance for the new macromodel as compared with the ones previously reported in the literature.

II. A CRITICAL GLIMPSE AT OP-AMP MACROMODELS

Actual op amps differ significantly from their ideal behavior in many aspects. Let us focus on the most important of these nonidealities, namely, the frequency-dependent voltage gain, the finite input and output resistances, the offset voltage, the slew-rate limitation, and the

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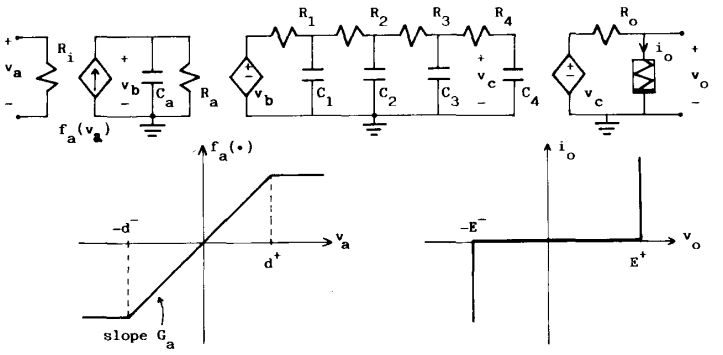

Fig. 1. Conceptual op-amp macromodel using nonlinear-controlled sources [1].

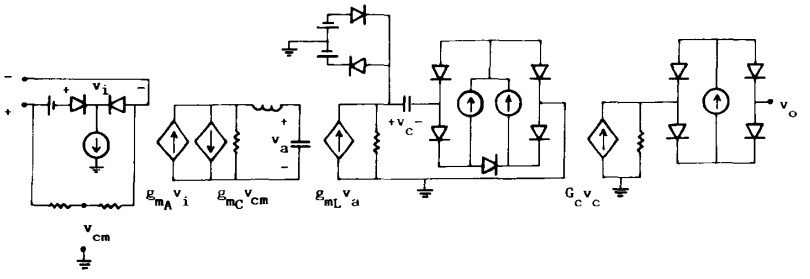

Fig. 2. Circuit diagram of the op-amp macromodel by Weil and McNamee [7].

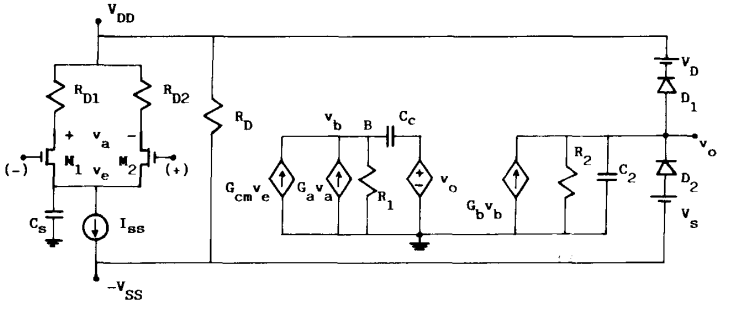

Fig. 3. Circuit diagram of the MOS op-amp macromodel by Turchetti and Massetti [5].

output voltage-saturation mechanism.[1] Essentially, all of the previously reported macromodels [1]–[7], [18], [21], [22] are based on a dominant storage element (a linear capacitor) and use some linear-controlled sources for modeling the frequency-dependent gain. However, they differ significantly in the devices used to represent both the slew rate and the voltage saturation. Since the way they represent such nonlinearities has a big influence on our ability for using each macromodel in a given simulator, it is worth discussing the different implementation alternatives. Namely, we will consider the following:

[1]In MOS amplifiers, the settling time is a very important parameter. However, it can be calculated from the slew rate and the frequency-dependent gain [5].

Class I — macromodels based on nonlinear-controlled sources [1], [2], a typical example of which is shown in Fig. 1;

Class II — macromodels using semiconductor diodes [6], [7], the most representative being the one shown in Fig. 2 [7]; and

Class III — macromodels resorting to two- and three-terminal semiconductor devices [3]–[5], as the one shown in Fig. 3 [5].

Macromodels from Class I cannot be incorporated into general-purpose simulation programs because nonlinear-controlled sources are not available in those simulators. On the contrary, such macromodels are the most adequate for design purposes, since closed expressions can be de-

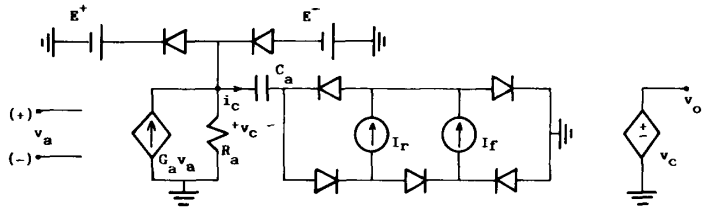

Fig. 4. Simplified Weil–McNamee macromodel for modeling the frequency-dependent gain, the slew rate, and the output-voltage saturation.

rived more easily for circuits where the op amp is represented by controlled sources than for those where macromodels of the other classes (using semiconductor devices) are used.

A typical macromodel from Class II is the one proposed in [7], which is shown in Fig. 2; a simplified version, which only covers the aspects we are interested in, is represented in Fig. 4. Qualitative as well as quantitative simulation results can be read from [19], and we must assert that, in our experience, it fits well with the examples we have tried. However, two drawbacks are worth consideration in this case. First, this macromodel uses semiconductor diodes for simulating the static and dynamic nonlinearities of an op amp; since semiconductor devices other than MOS transistors are not available in many timing simulators, the range of usefulness of this macromodel is restricted to electrical simulators, which are not well-suited for combined digital/analog systems. Of course, diodes can be substituted by diode-connected MOS transistors, but if this is the case, we will handle again a high number of transistors. The second problem is concerned with the diodes themselves because of the exponential nature of the diode function. Thus, a trade-off must be established between accuracy and speed for any situation.

In principle, macromodels pertaining to Class III can be exclusively used at the electrical level (in SPICE2 [23], for instance) because bipolar devices are not available at a higher abstraction level. However, in some cases [5] we can resort to either electrical- or switch-level (DIANA [24], SPLICE [25], etc.) simulators, since a model for the MOS transistor is usually included in these two simulation levels. Anyhow, in the latter case: 1) the overall simulation accuracy is very much dependent on the MOS model itself, this model being much more precise at the electrical level than at the switch level; 2) the number of three-terminal devices means a relatively high calculation overhead as well as the need of determining many parameters; and 3) since diodes have to be simulated by MOS transistors, a difficult compromise between accuracy and speed must be established *a priori*.

In fact, each macromodel class is different from the others in its particular way of charging a linear capacitor and modeling the nonlinear dynamics of the op amp. Thus, the general working principle of both Classes II and III can be roughly understood from the study of the conceptual model included in Class I. Therefore, although

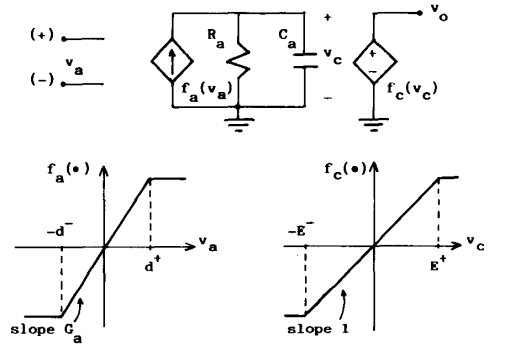

Fig. 5. Simplified conceptual op-amp macromodel for modeling the frequency-dependent gain, the slew rate, and the output-voltage saturation.

there is an intimate connection among the three classes, in the next section we will pay attention to the first one because we will derive a new interesting class from it.

III. A New Macromodel for the Time Domain

A. Objectives

Evolving from considerations made in the preceding section, we faced the problem of developing a new time-domain macromodel following three guidelines:

1) the macromodel has to be built from the component set available in a timing or switch-level simulator, i.e., two-terminal linear elements, linearly controlled sources, switches, digital gates, etc.;
2) the new model must be able to handle both the low- and the high-frequency range of the op-amp behavior, including its nonlinearities. That means potential for accurate nonlinear transient analysis; and
3) the macromodel must retain a basic analytical form, thus allowing formulation of meaningful design equations for any practical circuit composed of op amps.

These three objectives can be reached when a Class I macromodel is modified in two ways: first, eliminating some drawbacks of that model due to an incomplete representation of its dynamics, and second, implementing the model nonlinearities by using a combination of linear-controlled sources, switches, and digital gates.

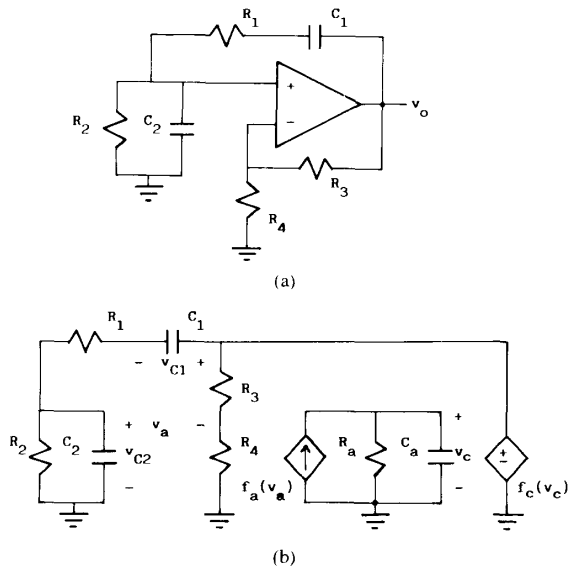

Fig. 6. Wien–Bridge oscillator: (a) circuit diagram; and (b) conceptual macromodel.

B. Inaccuracies in Class I Macromodels

A macromodel of Class I is shown in Fig. 1 [1]. This model is simplified for our purposes in Fig. 5, where the circuit elements used to represent the input and output resistances as well as the higher frequency poles of the op amp have been dropped for simplicity, since they are not important in this discussion and can be added very easily. Let us consider the Wien–Bridge oscillator shown in Fig. 6(a). Fig. 6(b) depicts an equivalent circuit when the macromodel in Fig. 5 is employed for substituting the op amp. A routine analysis gives the state equations for the network:

$$\frac{dv_{c_1}}{dt} = -\frac{1}{R_1C_1}\left[v_{c_1} + v_{c_2} - f_c(v_c)\right] \tag{1}$$

$$\frac{dv_{c_2}}{dt} = -\frac{1}{R_1C_2}\left[v_{c_1} + \frac{R_1+R_2}{R_2}v_{c_2} - f_c(v_c)\right] \tag{2}$$

$$\frac{dv_c}{dt} = \frac{1}{C_a}f_a\left[v_{c_2} - \frac{f_c(v_c)}{K}\right] - \frac{v_c}{R_aC_a} \tag{3}$$

where

$$K = 1 + \frac{R_3}{R_4} \tag{4}$$

$$f_a(x) = \frac{G_a}{2}\left[|x + d^-| - |x - d^+| + d^+ - d^-\right] \tag{5}$$

$$f_c(x) = \tfrac{1}{2}\left[|x + E^-| - |x - E^+| + E^+ - E^-\right]. \tag{6}$$

We have proceeded to design and build up several oscillators, by changing K and the RC product. These circuits were based on the use of μA741 op amps, whose parameters were measured in the laboratory. When the above general equations are simulated using a fourth-order Runge–Kutta integration algorithm, the result is Table I, which gives a comparison between predicted and empirical data for the actual oscillators that were under study. In all the cases, the value of the amplitude corresponds to the signal v_{c_2} measured at the positive input lead of the op amp. The op-amp output voltage saturation levels were $\simeq \pm 15$ V. For low oscillation frequencies ($\leqslant$12.2 kHz in our case), the output of the op amp is saturated and an important disparity between simulation and experience is exhibited. On average, an error higher than 20 percent could be expected in both the frequency and the amplitude of the oscillations. For high frequencies ($\geqslant$12.2 kHz), the accuracy in the calculation of the frequency increases a lot (average error of 0.7 percent) while the improvement in the accuracy of the amplitude is not significant.

TABLE I
EXPERIMENTAL RESULTS AND SIMULATION RESULTS USING THE MODEL IN [1] FOR THE WIEN–BRIDGE OSCILLATOR AND FOR DIFFERENT OSCILLATION FREQUENCIES

Design values		Experimental results		Simulation results		Errors, %	
K	$1/RC, s^{-1}$	freq.,hz	ampl.,v	freq.,hz	ampl.,v	freq.	ampl.
3.1	354.3	55.9	5.3	43.7	6.26	21.8	18.1
3.1	1786	280.4	5.32	214.1	6.4	23.6	20.7
3.05	11915	1878	5.16	1487	6.24	20.8	20.9
3.5	11915	1776	5.65	1141	6.98	35.7	23.5
3.5	71269	9576	5.5	6583	6.28	31.2	14.2
3.5	106942	12206	5.19	9626	5.62	21.1	8.2
3.05	106942	14900	4.41	15155	4.48	1.7	1.6
3.08	370370	46961	1.18	47006	1.41	0.09	19.5
3.5	986039	86286	0.67	85793	0.78	0.57	16.4

A qualitative interpretation of these disparities can be derived from Fig. 7, where some interesting waveforms are plotted for both an experimental circuit (Fig. 7(a)) and its simulated counterpart (Fig. 7(b)). These signals correspond to the Wien–Bridge oscillator in Fig. 6(a) with the design parameters trimmed to be $K = 3.5$ and $(1/RC) = 11915\ s^{-1}$. For the sake of clarity we have divided the time axis in Fig. 7 into several intervals, which are associated with different mechanisms during the network operation. Thus, inside (a, b) the circuit and its model are operating in the positive output saturation region. After the time instance $t = b$ there is an important disparity between the two entities, since the actual circuit goes out of saturation while the model still remains in saturation until the time instance $t = b'$. A similar situation happens in the negative saturation region. Looking at Fig. 6(b), we postulate that the delays appearing in the simulation could be due to the accumulation of a supplementary charge in the capacitor C_a during the time interval in which the output of the op amp is saturated, accumulation which does not correspond to a physical mechanism. In other words, the disparities are due to the absence in the macromodel of a circuit element that can stop the process of delivering charge to C_a when the output saturation is reached.

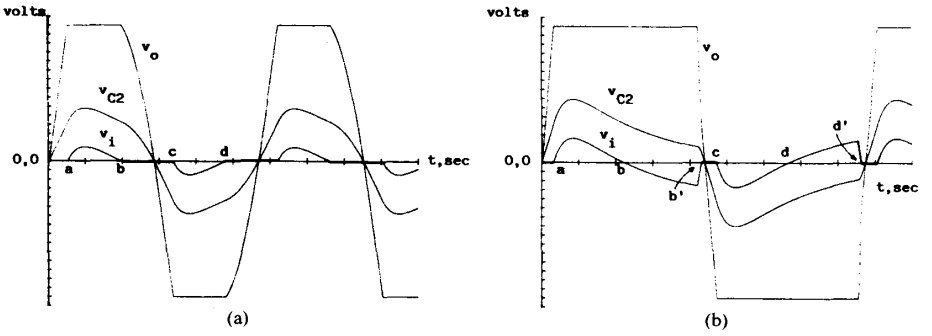

Fig. 7. (a) Experimental waveforms measured from the circuit in Fig. 6(a) for $K = 3.5$ and $(1/RC) = 11\,915\ s^{-1}$; and (b) corresponding simulated waveforms obtained from the model in Fig. 6(b).

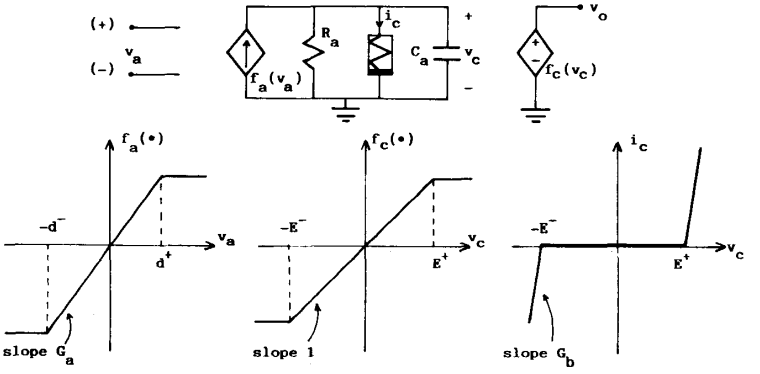

Fig. 8. Modified conceptual op-amp macromodel.

C. Basic Digitally Controlled Macromodel

Turning back to the conceptual model in Fig. 5, we will consider first the introduction of a network mechanism for limiting the charge of capacitor C_a. It can be done by connecting a nonlinear resistor across C_a, this resistor having the current–voltage characteristic shown in Fig. 8. However, the model in Fig. 8 is not adequate for our purposes because: a) it relies on nonlinear-controlled sources, not available in timing simulators, and b) it is prone to numerical latch-up [19].

In order to circumvent both drawbacks we propose to use the threshold elements introduced by Arnout and de Man for modeling digital MOS circuits [20]. These kinds of components are available in several timing simulators [24], [25]. For the sake of completeness we will reproduce herein the definition of such elements.

Definition 1:

$$T_{F1}(v_i, E) = \begin{cases} 1, & v_i > E \\ 0, & \text{elsewhere} \end{cases} \tag{7a}$$

$$T_{F2}(v_i, E) = \begin{cases} 0, & v_i > E \\ 1, & \text{elsewhere} \end{cases} = \overline{T_{F1}(v_i, E)}. \tag{7b}$$

Fig. 9 shows the new macromodel. Note that we use a linearly controlled source for modeling the low-frequency gain, the different op-amp nonlinearities being modeled by digitally controlled analog switches. Let us explain in more detail the simulation of these nonlinearities.

The nonlinear voltage-controlled current source, $i = f_a(v_a)$, is implemented in Fig. 9 by a linear voltage-controlled current source, two constant current sources, and the three switches labeled S_2, S_3, and S_4, which are controlled by the digital variables Z_2, Z_3, and Z_4, respectively. These digital variables are generated by the circuit in Fig. 9(b), which employs two threshold elements. When the op-amp differential input is higher than d^+, switch S_3 is closed and switches S_2 and S_4 are open. Then, the current charging C_a is I_r.[2] When the op-amp input is lower than $-d^-$, the charging current is I_f. Finally, if the input voltage is comprised in the interval $(-d^-, d^+)$, the charging current depends linearly on v_a. It should be noted that asymmetries in the slewing behavior are modeled by this circuit by means of the two constant sources (I_r and I_f) and two switches (S_3 and S_4). This allows a slew

[2]Here we assume that the current flowing through the resistor R_a is neglected. As a matter of fact, the highest value of this current is given by E^+/R_a, while the value of I_r is given by $I_r = SR^+ C_a$, where SR^+ is the value of the positive-going slew rate. As $SR^+ \gg E^+/(R_a C_a)$ for every properly designed op amp, we can neglect the current flowing through R_a.

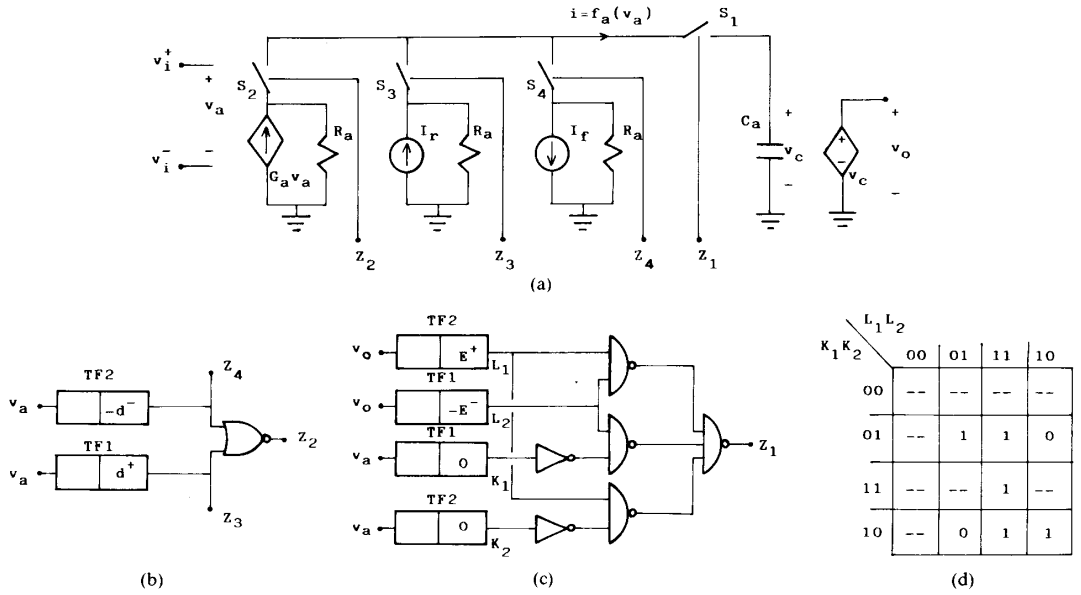

Fig. 9. Basic digitally controlled op-amp macromodel: (a) circuit diagram using analog switches; (b) electrical to logical converter for obtaining the variables $Z_2 - Z_4$; (c) electrical to logical converter for obtaining Z_1; and (d) truth table for the digital part of the circuit in Fig. 9(c).

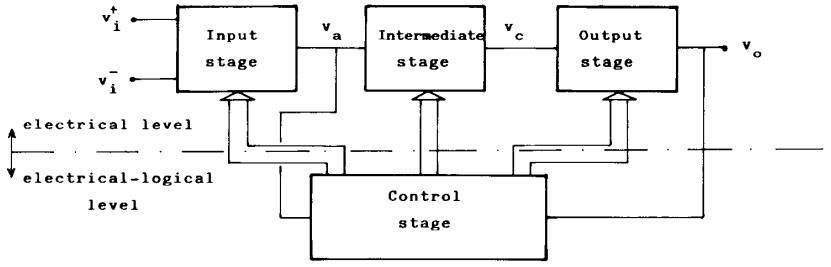

Fig. 10. Conceptual block diagram showing the architecture of the macromodel proposed in this paper.

enhancement in one direction and a slew degradation in the other, as is observed in practice [26].

The other nonlinearities are implemented by the switch S_1, the corresponding control circuit being the one shown in Fig. 9(c). Since S_1 is connected in series to the capacitor, no charge is flowing into C_a in the case when v_0 is at one of the output saturation levels. Thus, both the output-voltage saturation mechanism and the charge limitation mechanism are simultaneously implemented by S_1. For a better understanding of how the controlling circuit of this switch works, we must refer to Fig. 9(d), where its truth table is represented. From this last figure, we see that the logic variable depends on both the op-amp differential input voltage and the op-amp output voltage. The dependence on v_0 is obtained through the upper threshold elements, while the dependence on v_a is obtained via the lower ones.

The different element values for the basic macromodel can be calculated from the data sheets using the following equations:

$$G_a R_a = A_0 \qquad \frac{G_a}{C_a} = A_0 \omega_1 \tag{8}$$

$$\frac{I_r}{C_a} = SR^+ \qquad \frac{I_f}{C_a} = SR^- \tag{9}$$

$$d^+ = \frac{I_r}{G_a} = \frac{SR^+}{A_0 \omega_1} \qquad d^- = \frac{I_f}{G_a} = \frac{SR^-}{A_0 \omega_1} \tag{10}$$

where A_0 is the dc gain of the op amp, ω_1 is the low-frequency pole, and SR^+ (alternatively SR^-) is the positive-going (negative-going) slew rate.

D. Extending the Capabilities of the Macromodel

Note from Fig. 9 that there are four different stages in the new macromodel. A block diagram illustrating the way these stages are interconnected is shown in Fig. 10, where

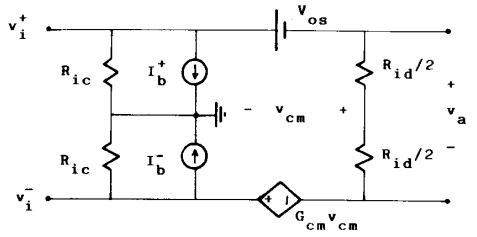

Fig. 11. Circuit diagram for the input stage of the enhanced macromodel.

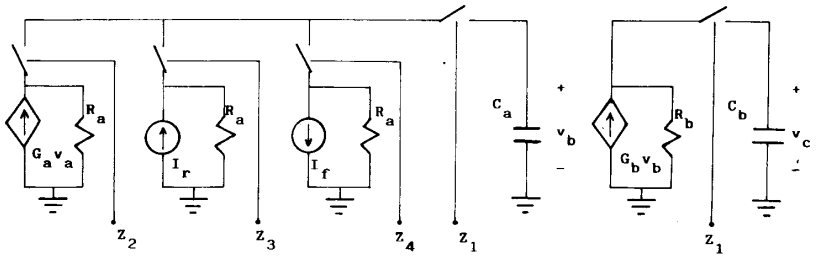

Fig. 12. Circuit diagram showing the intermediate stage to be used in case a high-frequency pole is included in the small-signal frequency response of the macromodel.

we distinguish two different levels: a) an electrical level comprising the input, intermediate, and output stages, and b) an electrical–logical level comprising the control stage. The different stages in either the electrical or the electrical–logical level are connected by voltage-controlled sources. In the next paragraphs we will show how to modify the different stages in order that all the relevant characteristics of the op-amp performance—with the exception of noise and thermal effects—can be modeled in a way compatible with timing simulators.

1. Modifications of the Input Stage: Taking into account considerations reported elsewhere [7], [15]–[18], we propose the input stage shown in Fig. 11. It simulates the finite input bias current, the offset voltage, the common-mode gain, the differential-mode input resistance, and the common-mode input resistances. By elementary analysis of the circuit in Fig. 11 and assuming $G_{cm} \ll 2$, we find

$$v_a \simeq (v_i^+ - v_i^-) + \frac{v_i^+ + v_i^-}{2} G_{cm} - V_{os}\left(1 + \frac{G_{cm}}{2}\right) \quad (11)$$

and thus it follows that

$$G_{cm} = \frac{1}{\text{CMRR}}$$

$$V_{os}\left(1 + \frac{G_{cm}}{2}\right) \simeq V_{os} = \text{offset voltage} \quad (12)$$

where both the common-mode rejection ratio (CMRR) and the offset voltage can be read from the op-amp data sheets. With regard to the other elements appearing in Fig. 11, their values can be directly obtained from the corresponding parameters in the data sheets.

2. Modifications of the Intermediate Stage: The small-signal frequency response of the basic macromodel in Fig. 9 is given by

$$A(s) = \frac{V_o(s)}{V_a(s)} = \frac{V_c(s)}{V_a(s)} = \frac{G_a R_a}{1 + sR_a C_a} = \frac{A_0}{1 + \dfrac{s}{\omega_1}} \quad (13)$$

which accounts for a phase shift of 90° at the unity-gain frequency, i.e., at a frequency such that $|A(j\omega_{0_{dB}})| = 1|$. The excess phase shift appearing in practical op amps can be modeled by including one or more high-frequency poles in the macromodel frequency response. Fig. 12 shows the intermediate stage for a case in which a two-pole behavior is exhibited—additional high-frequency poles can be included by adding more stages as the one on the right side of Fig. 12. The small-signal frequency response of a macromodel including the intermediate stage of Fig. 12 is given by

$$A(s) = \frac{G_a G_b R_a R_b}{(1 + sR_a C_a)(1 + sR_b C_b)} = \frac{A_0}{\left[1 + \dfrac{s}{\omega_1}\right]\left[1 + \dfrac{s}{\omega_2}\right]}. \quad (14)$$

If we choose $G_b R_b = 1$, then (8)–(10) are still applicable. The values of the elements R_b, G_b, and C_b can be calculated using

$$R_b = \frac{1}{\omega_2 C_b}$$

$$G_b = \frac{1}{R_b} \quad (15)$$

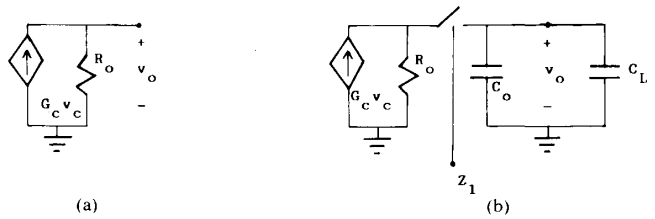

Fig. 13. Alternative circuit diagrams for the output stage of the enhanced macromodel: (a) circuit for modeling the finite output resistance; and (b) circuit for modeling both the finite output resistance and the high-frequency pole.

where the value of ω_2 can be either read from the data sheets or calculated using the unity-gain frequency $\omega_{0_{dB}}$ and the phase margin Φ_m. As a matter of fact, assuming $\omega_2 \gg \omega_1$, we get

$$\omega_2^{-1} = \frac{1}{\omega_{0_{dB}}} tg\left[\frac{\pi}{2} - \Phi_m\right]. \tag{16}$$

3. Modifications of the Output Stage: In Fig. 13 we show two alternatives for modeling op-amp output stages. In both cases, we assume that the dc gain of the output stage is unity, i.e., we choose $G_c R_0 = 1$, which ensures that (8)–(10) remain valid. Note that the circuit in Fig. 13(b) introduces a high-frequency pole in the small-signal op-amp frequency response. Thus, it can be used as an alternative way to include the second pole influence, instead of using the intermediate stage in Fig. 12. This alternative scheme is specially suited for those cases where only capacitive loads are significant, as happens in MOS op amps used in switched-capacitor circuits. The design equations are the following:

$$R_0 = R_{\text{out}}$$

$$G_c = \frac{1}{R_0} \tag{17a}$$

$$C_0 + C_L = \frac{1}{\omega_2 R_0} \tag{17b}$$

where (17a) is valid for both circuits in Fig. 13 and (17b) is only valid for the one in Fig. 13(b). In the latter case, C_L is the load capacitor and ω_2 can be either directly read from the data sheets or calculated using (16).

4. Modifications of the Control Stage: The modifications of the control stage to be considered herein account for a more detailed modeling of the op-amp dynamic behavior when the output voltage is at any of the saturation states (either positive or negative), and it is driven out of this state. This has not yet been studied in detail, but in some cases it becomes important enough to justify its modeling. For instance, in [19] we have shown that frequency errors can appear when designing op-amp-based oscillators if these dynamics are not taken into account. Also, we have found that the effect of this is a time delay when leaving the saturation region. That delay is not symmetric; instead, it is in general different for the positive-going output and for the negative-going one. The way we have chosen for incorporating this effect is a delay associated with the logic variables labeled as K_1 and K_2 in Fig. 9. It can easily be included in the model for the logic elements used in DIANA.

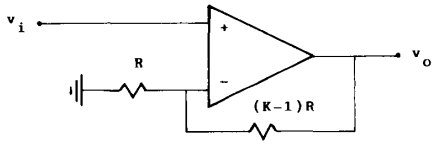

Fig. 14. Circuit diagram for a positive gain amplifier realized using an op amp.

IV. Macromodel Performance

The validation of a new macromodel has to be done at different levels. First of all, we need to investigate the qualitative and the quantitative performance of the model referred to the electrical characteristics of actual op amps. A second point is the comparison between the macromodel and device-level models, the keys being here the accuracy as well as the simulation speedup. Finally, the performance and properties of the new macromodel have to be compared with those from other macromodels previously proposed in the literature. Concerning these aspects, we have carried out many experiments. In particular we will include herein several examples that we consider significant for validating our macromodel.

A. Positive Gain Amplifiers

The circuit of Fig. 14, for a value of $K = 3.5$, has been built using off-the-shelf components (μA741 for the op amp). The agreement between the circuit and the model performances was found to be excellent; specifically, Fig. 15 shows a case for which other op-amp macromodels are less accurate than ours, namely, for a 10-V square wave of 10 kHz. Fig. 15(a) corresponds to the experimentally observed output waveform, Fig. 15(b) depicts the response for one of those macromodels—in this case, it was obtained using the model by Weil and McNamee [7] in SPICE2, and Fig. 15(c) plots the output as obtained by our model when implemented in DIANA. As can be seen from this figure, a delay due to the output saturation dynamics

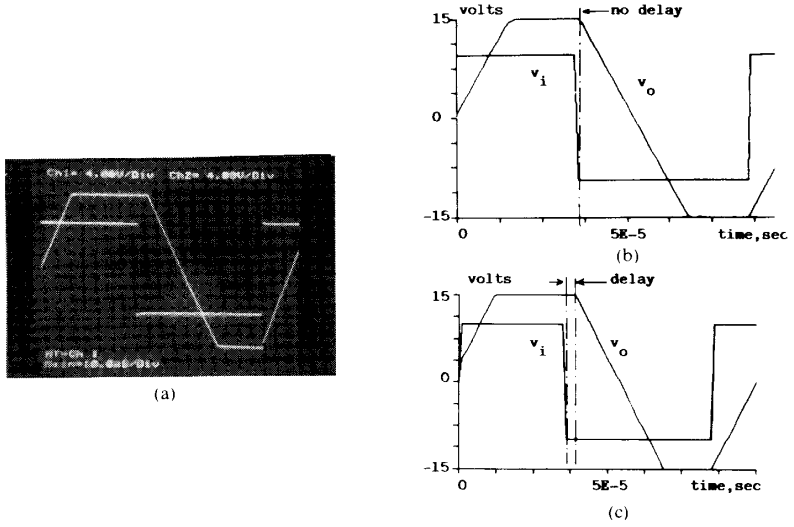

Fig. 15. Experimental and simulation results for the positive-gain amplifier: (a) measured waveforms showing a delay in the output response corresponding to the falling edge of the input; (b) simulation results obtained using SPICE2 and the model by Weil–McNamee [7]; and (c) simulation results obtained using DIANA and the new model.

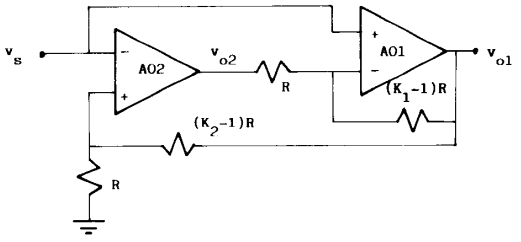

Fig. 16. Circuit diagram for a phase-compensated positive-gain amplifier [27].

is shown by the actual circuit as well as by our macromodel. Weil–McNamee's model fails in exhibiting that effect.

Consider now the composite amplifier in Fig. 16 [27]. We have selected $K_1 = K_2 = 3$ and built the circuit by using a μA747. Fig. 17(a) shows the experimental waveforms observed when a sinusoidal input of 6 V and a frequency of 10 kHz is applied. Fig. 17(b) depicts the corresponding waveforms obtained when using our model in DIANA.

B. Wien–Bridge Oscillator

Using a μA741, we have compared an experimental circuit for the Wien–Bridge oscillator with its model following our approach. A detailed consideration of many circuit value combinations can be found in [19]. Table II shows a comparison made by using the macromodels in [1] and [7], the new macromodel, and the empirical results for several designs. The errors in predicting both the amplitude and the frequency of every oscillator prove the superior performance of our approach. Fig. 18 shows the waveforms for a particular design condition, namely for $(1/RC) = 71\,269\ s^{-1}$ and $K = 3.5$. Fig. 18(a) corresponds to the experimental result. Fig. 18(b)–(c) has been obtained using special-purpose programs [19] and shows the simulation results when using either our model (Fig. 18(b)) or the model in [1] (Fig. 18(c)). Finally Fig. 18(d)–(e) shows the results obtained when using our model in DIANA (Fig. 18(d)) and when using the model in [7] in SPICE2 (Fig. 18(e)).

C. A MOS Unity-Gain Buffer

The experimental comparisons we have detailed above exclusively deal with bipolar op amps. The new model is also suitable for MOS amplifiers. To illustrate this we have selected one of the four NMOS op amps given in [5], namely, the so-called design *D*. This is a case where the settling behavior corresponds to a two-pole transient characteristic. The amplifier was connected in a unity-gain configuration and driven by a positive voltage step of 1 V.

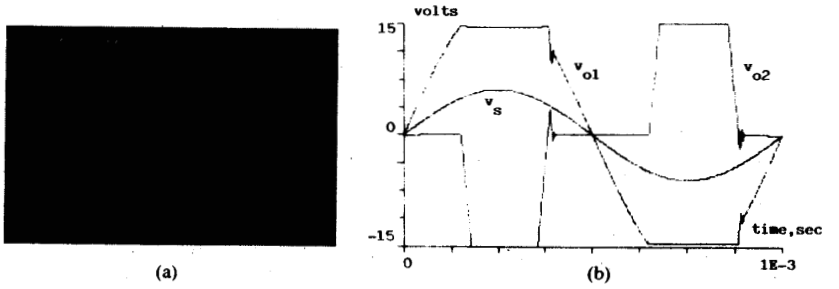

Fig. 17. Experimental and simulation results for the circuit in Fig. 16 ($K_1 = K_2 = 3$) when driven by a sinusoidal voltage of 6-V amplitude and 10-kHz frequency: (a) measured waveforms; and (b) corresponding simulated waveforms obtained using our model in DIANA.

TABLE II
EXPERIMENTAL AND SIMULATION RESULTS FOR DIFFERENT OSCILLATOR FREQUENCIES AND DIFFERENT OP-AMP MACROMODELS

Experimental results		Errors for the model in [1], %		Errors for the model in [7], %		Errors for the new model, %	
freq.,hz	ampl.,v	freq.,hz	ampl.,v	freq.,hz	ampl.,v	freq.	ampl.
55.9	5.3	21.8	18.1	0.71	6.9	0.3	0.56
280.4	5.3	23.6	20.7	0.11	6.9	0.35	1.5
1878	5.16	20.8	20.9	0.68	3.1	0.03	1.9
1776	5.65	35.7	23.5	0.01	22.5	0.63	1.2
9576	5.5	31.2	14.2	1.3	20.3	0.88	1.3
12206	5.19	21.1	8.2	2.8	15.4	0.89	1.1
14900	4.41	1.7	1.6	2.7	10.4	1.7	1.6
46961	1.18	0.09	19.5	1.4	22.1	0.09	19.5
86286	0.67	0.57	16.4	3.5	3.28	0.57	16.4

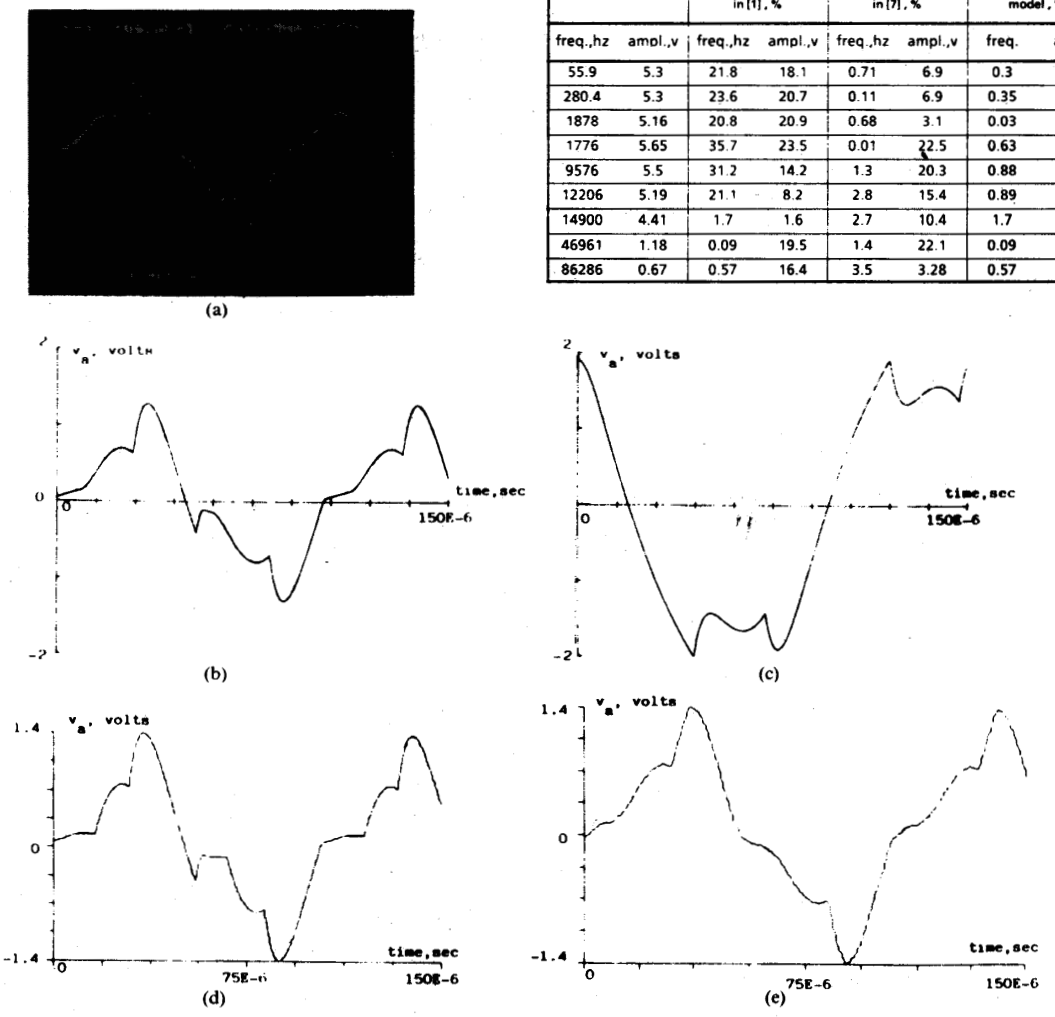

Fig. 18. Experimental and simulation results for the Wein–Bridge oscillator with $(1/RC) = 71\ 269\ s^{-1}$ and $K = 3.5$: (a) measured waveform for the differential input of the op amp; (b) simulation result using our model in a special-purpose program; (c) simulation result using the Chua–Lin model [1] in a special-purpose program; (d) simulation result using our model in DIANA; and (e) simulation result using the Weil–McNamee model [7] in SPICE2.

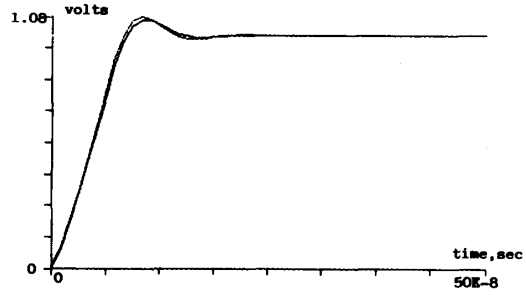

Fig. 19. Simulation results for a NMOS op amp connected in a unity-gain configuration and driven by a positive voltage step. The results obtained using the new model in DIANA have been superimposed on those using the model from [5] in SPICE2.

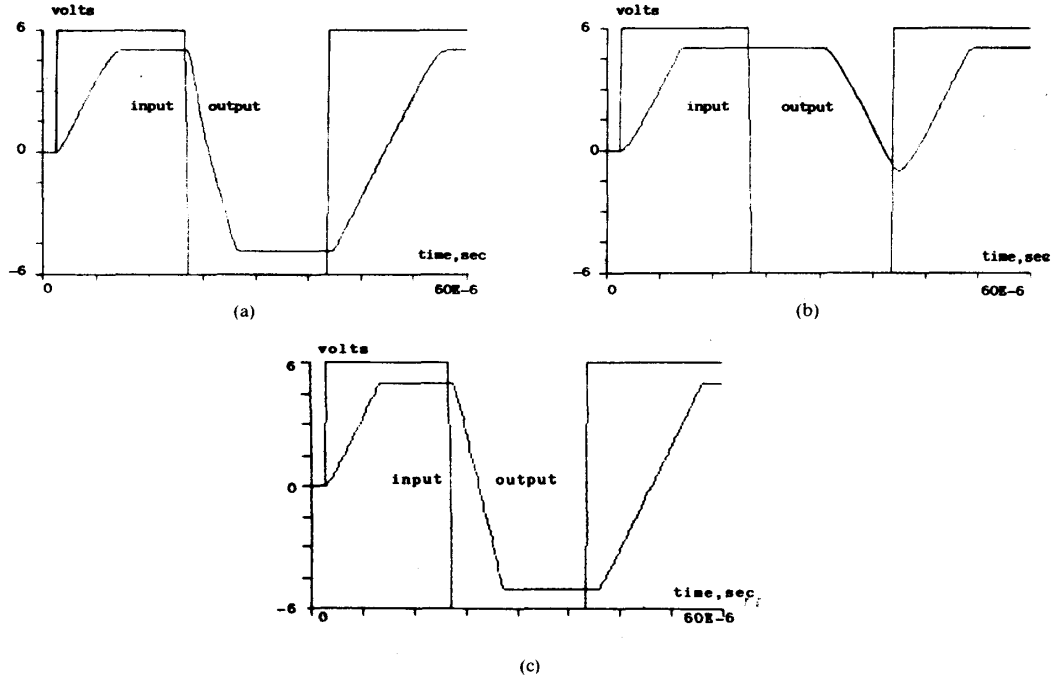

Fig. 20. Simulation results for a CMOS op amp connected in a unity-gain configuration and driven by a square wave of 6-V amplitude: (a) input and output waveforms for the device-level model; (b) corresponding waveforms for the model from [5]; and (c) corresponding waveforms for the new model.

Since in [5] the actual output was compared with the macromodel reported there, we have compared in Fig. 19 the output given by our macromodel with the output obtained from the macromodel in [5, fig. 3].

As can be seen from Fig. 19, the performance of the new model when simulating MOS amplifiers is similar to that of the model in [5], this latter model being specially suited for MOS op amps. A new experiment will show that, under very large input signals, the new model performs in a more accurate way than the model in [5]. We have considered a two-stage CMOS amplifier [28], and have designed it to exhibit the following specifications:

$$\begin{aligned} A_0 &= 92\,400, \\ w_1 &= 2\pi \times 38.9\ \mathrm{s}^{-1} \\ w_2 &= 2\pi \times 2.4 \times 10^6\ \mathrm{s}^{-1} \\ E^+ &= E^- = 5\ \mathrm{V} \\ R_{\mathrm{out}} &= 4.53 \times 10^5\ \Omega \\ SR^+ &= 6.8\ \mathrm{V}/\mu\mathrm{s} \\ SR^- &= 14.8\ \mathrm{V}/\mu\mathrm{s}. \end{aligned} \tag{18}$$

We connected the op amp in a unity-gain configuration and drove it using a square wave of 6-V amplitude and zero offset. Fig. 20(a) shows the output waveform obtained using the device-level model in SPICE2. Fig. 20(b) shows the result obtained when the op amp is simulated by the model in [5]. Finally, Fig. 20(c) shows the corresponding result obtained when using our model in DIANA.

D. A Comparison in Terms of CPU Time

It is difficult to carry out an exact comparison of our macromodel versus other macromodels in terms of CPU time. One of the reasons for this is that a unique standard simulation program cannot be used to evaluate all of them. In fact, as we have asserted in the introduction, our macromodel is intended to be used in a hybrid simulator, part of its benefits being the higher speed of such simulators as compared with electrical-level simulators. However, it is interesting to make some additional considerations.

Summarizing our observations of many simulation runs of SPICE2 using bipolar and MOS device-level models of the macromodels in [3], [5], and [7], we can conclude that among them, the macromodel by Weil–McNamee is the fastest one. Taking this into account, we have used a special-purpose program written by us to compare this latter macromodel and our model in a unified framework [19]. Thus, we have found a CPU time ratio between our model and that of Weil–McNamee which ranges favorably to ours from 4 to 6 times. It should be noticed that a comparison between SPICE2 and DIANA has no meaning at all concerning the macromodels themselves, since there are factors affecting the CPU time that are inherent to each program. Anyway, we have made this comparison and found that, for the same degree of precision, our macromodel in DIANA runs from 2 to 4 times faster than the ones from [3], [5], and [7] when running in SPICE2, those macromodels being on average four times faster than the device-level models (SPICE2). The first factor tends to be even higher when the op amp is driven into operation regions where a combination of several nonlinearities applies. Also, the second factor depends on both the number of transistors and its type (either bipolar or MOS). Further improvements in CPU time can be obtained under some circumstances if we substitute each switch S_1 and S_2 in Fig. 9(a) and the corresponding control logic by two single-threshold controlled switches connected in series—S_{11}, S_{12} and S_{21}, S_{22}, respectively. The voltage controlling the switches S_{11} and S_{12} should be v_a, the corresponding thresholds being $-d^-$ and d^+, respectively. On the other hand, switches S_{21} and S_{22} should be controlled by the voltage at the input of switch S_1 in Fig. 9(a), the thresholds being $-E^-$ and E^+, respectively. For example, CPU time can be reduced by a factor of 2.5 when using this strategy in the circuit of Fig. 16.

Concerning computer time, a major advantage of our macromodel is that it allows us to include a precise simulation of the analog part of an analog/digital chip in a simulation run where the digital part is simulated at the timing level (or even at the logical level). We foresee an important overall speedup for such large circuits.

V. Conclusions

A new macromodel has been presented, incorporating the following interesting features:

1) its precision is equal to or higher than that of other macromodels previously proposed;
2) it is suited for switch-level simulations, allowing both a precise waveform prediction and a low computation time;
3) it gives faster response time as compared with other known macromodels; and
4) it resorts for the first time to digital components for simulating analog building blocks, thus broadening the perspective of macromodeling of analog circuits.

The model still is described by a set of nonlinear equations that describes the op-amp behavior, thus allowing the designer to handle them for synthesis purposes. Furthermore, its efficiency relies on the implementation of every nonlinearity by a combination of linear control sources and standard digital components.

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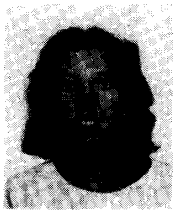

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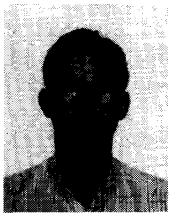

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