# VERY HIGH FREQUENCY CMOS OTA-C QUADRATURE OSCILLATORS

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## ABSTRACT

**An approach to the design of high-frequency monolithic voltage-controlled oscillators using operational transconductance amplifiers and capacitors is given. Results from two 3$\mu$m CMOS prototypes are presented. Both frequency and amplitude of the oscillations can be tuned by means of control voltages. Programmable oscillator frequencies up to 56.1Mhz are obtained, the amplitudes being adjustable between 1 v peak-to-peak and 100mv peak-to-peak. Total Harmonic Distortions from 2.8% down to 0.2% have been experimentally measured in the laboratory.**

## I. INTRODUCTION

The design of voltage controlled sinusoidal oscillators is a classical problem with applications in communication systems, instrumentation, measurement, etc. It has been proposed [1,2] to use circuits constructed by Operational Transconductance Amplifiers and Capacitors (OTA-C) as a way to overcome the performance limitations of conventional RC-active Voltage Controlled Oscillators (VCO). This proposal is based on two basic facts. On the one hand, the undoubted potential of the OTA for high frequency applications [3-6,8]. On the other hand, the possibility of exploiting the programmability of the transconductance gain $g_m$ of the OTA [7] to readily implement the VCO operation. As a matter of fact, the validity of these hypotheses has already been demonstrated for discrete bipolar implementations of OTA-C oscillators up to 1Mhz [1,2]. However, not much work has been reported yet on monolithic implementations where much higher frequencies can be expected [8].

In this paper we demonstrate that it is possible using standard 3$\mu m$ CMOS technology, to implement monolithic OTA-C VCOs working within the megahertz range. In particular, a 3$\mu m$ CMOS prototype is reported oscillating at a maximum frequency of 56Mhz. We show that this result can be achieved due to the combination of 1) a simple design technique based on OTAs, and 2) a fundamental modeling of the OTA taking into account parasitic effects.

## II. THEORY OF QUADRATURE OSCILLATORS

The OTA-C architecture proposed in the next section is based on the quadrature oscillator mode of operation. The ideal quadrature oscillator consists of a positive and a negative integrator in a feedback loop as shown in Fig. 1 [2]. This results in a characteristic equation with a pair of roots lying on the imaginary axis of the complex frequency plane.

$$s^2 + \omega_{o1}\omega_{o2} = 0 \tag{1}$$

In a practical quadrature oscillator, due to the influence of parasitics, the poles are displaced from their nominal position ($s_p = \pm j\sqrt{\omega_{o1}\omega_{o2}}$) to either the right or the left side of the frequency plane. For this reason, the oscillator must be designed to have its poles initially located inside the right half complex frequency plane in order to assure self starting operation. This is usually accomplished by making one of the integrators have a pole in the right half of the complex frequency plane. Also, some nonlinear feedback mechanism has to be included so that as the amplitude increases the poles move towards the left half frequency plane. Thus, a stable limit cycle would be reached with a stable amplitude and frequency while the poles are located exactly on the imaginary axis. The nature of the feedback mechanism can be of several types [2]. In this paper we discuss one of them, namely the nonlinear amplitude limiting mechanism.

Fig. 2 shows two possible block diagrams of a practical quadrature oscillator with linear and nonlinear feedback [2]. Assuming the nonlinearities $f(\cdot)$ and $g(\cdot)$ in Figs. 2(a) and 2(b), respectively, are even functions, the block diagram of Fig. 2(a) yields to a stable quasi-sinusoidal limit cycle if $\frac{df(x)}{dx}$ is decreasing for $x > 0$ [10]. The same result is obtained for the case of Fig. 2(b) if $\frac{dg(x)}{dx}$ is increasing for $x > 0$. The time domain differential equations associated respectively with these block diagrams are:

$$\frac{d^2x}{dt^2} + \frac{dx}{dt}\left[b_2\omega_{o_2} - b_1\omega_{o_2}\frac{df(x)}{dx}\right] + \omega_{o_1}\omega_{o_2}x = 0 \tag{2a}$$

$$\frac{d^2x}{dt^2} - \frac{dx}{dt}\left[b_2\omega_{o_2} - b_1\omega_{0_2}\frac{dg(x)}{dx}\right] + \omega_{o_1}\omega_{o_2}x = 0 \tag{2b}$$

For Fig. 2(a), if the distortion of the oscillator is low enough so that the high order harmonics produced by $f(\cdot)$ are filtered out before they appear at the input of the nonlinear element, we can approximate $V(t)$ (see Fig. 2) by the first term of its Fourier series expansion. Hence, if $x(t) = A\cos(\omega t)$ and $f(\cdot)$ is even then $V(t) = AN_1(A)\cos t(\omega t)$, where

$$N_1(A) = \frac{1}{AT}\int_0^T f(x(t))\cos(\omega t)dt, \quad T = \frac{2\pi}{\omega} \tag{3}$$

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This means that the nonlinear function $f(\cdot)$ can be approximated by a linear function with slope $N_a(A)$ that depends on the amplitude of its input. The same applies to $g(\cdot)$ in Fig. 2(b). This is called the *describing function approach* [2]. Therefore,

$$\frac{df(x)}{dx} \simeq N_1(A), \qquad \frac{dg(x)}{dx} \simeq N_1(A) \tag{4}$$

and the Laplace transform of (2) yields

$$s^2 + s(\omega_{o2}b_2 - \omega_{o2}b_n N_1(A)) + \omega_{o1}\omega_{o2} = 0 \tag{5a}$$
$$s^2 - s(\omega_{o2}b_2 - \omega_{o2}b_n N_2(A)) + \omega_{o1}\omega_{o2} = 0 \tag{5b}$$

Once the limit cycle is reached the amplitude and frequency of the oscillators will be given by

$$A_o = N_i^{-1}(b_2/b_1) \text{ and } \Omega_o^2 = \omega_{o1}\omega_{o2}, \qquad i = 1,2 \tag{6}$$

Note that the oscillator will be self starting if $b_2 - b_1 N_1(0) < 0$ for Fig. 2(a) and $b_2 - b_1 N_2(0) > 0$ for Fig. 2(b). The quadrature oscillator implementation we are going to introduce in the next section corresponds to the block diagram of Fig. 2(b).

## III. OTA–C VCO ARCHITECTURE

If an OTA is loaded by a capacitor, the output and input voltages of the OTA are simply related by an integration operation. This basic principle can be used to obtain a quadrature OTA–C oscillator from Fig. 2(b). The resulting circuit is shown in Fig. 3 where $R_N$ is a nonlinear resistor used to implement the limiting mechanism and whose characteristics are shown in Fig. 4(a). Two different approaches for the implementation of this nonlinear resistor in our experimental prototypes were taken. The simplest one, shown in Fig. 4(b), uses two diode–connected MOS transistors to implement each of the branches in Fig. 4(a). The second approach, depicted in Fig. 4(c) uses, for each branch, a comparator and an MOS transistor. Consider, for instance, the lower half of the circuit. If the input voltage is less than $E$, the NMOS transistor is off, but if the input voltage is greater than $E$, the output of the comparator is high and the NMOS transistor is able to sink a great amount of current. We have implemented the right half branch of the curve in Fig. 4(a). The upper half of the circuit in Fig. 4(c) implements the other half branch of the curve in Fig. 4(a). Analysis assuming that no current is entering $R_N$ gives the following characteristic equation for Fig. 3.

$$s^2 - \frac{s}{C_2}[g_{m3} - g_{m4}] + \Omega_0^2 = 0 \tag{7}$$

where we have defined $\Omega_0^2 \doteq (g_{m1}g_{m2})/(C_1C_2)$. We see that by adjusting $g_{m3}$ and $g_{m4}$ the poles can be positioned close to the imaginary axis but in the right–half complex plane, so that the circuit is unstable and self–starting. Proper operation of the oscillator is guaranteed because of the nonlinear feedback introduced by the nonlinear resistor, whose effect is to pull the poles back towards the imaginary axis until they finally reach this axis for some value, $A_o$, of the amplitude. Thus a stable quasi–sinusoidal oscillation of frequency $\Omega_o$ and amplitude $A_o$ is obtained.

## IV. OTA PARASITIC EFFECTS

Previous analyses have assumed an ideal model for the OTAs. Some experimental deviations can be expected as a consequence of using such an ideal model. Unfortunately, for high–frequency operation, the resulting errors are very large to be tolerated. For accurate high–frequency design, OTA parasitics cannot be ignored in analyzing Fig. 3. In principle, only two parasitics have to be considered to obtain a valid design technique up to, at least, 56Mhz, as it is demonstrated in the experimental results. These are the input and output impedances and the phase shift of the OTAs [2,9], which are both included in the macromodel of Fig. 5.

Let us calculate again the characteristic equation of Fig. 3 considering the impedances (associated to $C_1$, $C_0$, $G_0$) and phase–shifts ($\omega_z$) of the OTAs. After some approximations, we get

$$s^2 - s\left[\frac{1}{C}(g_{m3} - g_{m4}) + 2\frac{\Omega_0^2}{\omega_z} - \frac{4G_0}{C}\right] + \Omega_0^2 = 0 \tag{8}$$

where we have assumed that the OTA parasitic capacitors have been included in $C_1$ and $C_2$ and have taken for simplicity $C_1 = C_2 = C$. As it can be seen, for high–frequency operation the effect of the phase shift is the dominant parasitic effect. Because of this phase–shift, the poles, which are nominally located very close to the imaginary axis, move further into the right–half plane. As a consequence, the amplitude control mechanism is forced to work harder than in the ideal case to pull the poles back towards the imaginary axis, causing the distortion level to increase and the oscillation frequency to decrease.

A way to avoid this performance degradation and hence to yield high–frequencies from Fig. 3 is to use a predistortion technique based on the analysis of the parasitics influence. We have used this method. The experimental results we have obtained confirm the validity of our approach.

## V. EXPERIMENTAL RESULTS

Several monolithic prototypes of Fig. 3 were fabricated using a $3\mu m$ CMOS double–metal technology (through and thanks to MOSIS). Different implementations were used for the OTA as well as for the nonlinear resistor. Here we are including results from two of these prototypes, respectively proto#1 and proto#2.

### Proto#1

The OTA used in proto#1 was similar to the linearized one presented by Nedungadi and Geiger [3] but with an increased transconductance by a factor of four. For the nonlinear resistor we used the two alternative implementations of Figs. 4(b) and 4(c), the complete CMOS realization of this latter resistor being the one shown in Fig. 6. Frequencies up to 10.34Mhz were obtained, the Total Harmonic Distortion (THD) ranging between 0.20% to 1.87% for a corresponding peak–to–peak amplitude voltages between 100mv to 1v. Fig. 7(a) shows, for 1v peak–to–peak, the experimental results of $(g_{m1}g_{m2})^{\frac{1}{2}}$ vs frequency. Fig. 7(b) shows the measured THD vs amplitude of a 10Mhz sinusoidal signal, for the two different implementations of $R_N$. In Fig. 8 a photomicrograph of the chip is given.

**Proto#2**

This prototype was intended for a larger oscillation frequency than the previous one. Thus, in order to minimize additional phase–shift of typical linearized OTAs, we selected a simple OTA architecture. Besides, since large frequency means large values of $g_m$ this OTA was made to operate at high current. This means making the input transistors and the tail current of the differential pair as large as possible, while maintaining also a large linear range [7]. The OTA used with the geometry factors of each transistor is shown in Fig. 9. The nonlinear resistor in this prototype was implemented using Fig. 4(b). The frequency of proto#2 can be tuned between 12Mhz and 56.1Mhz. Table 1 shows the dependence of the frequency on the biasing (see $V_{bias}$ in Fig. 9, the OTA $g_{m3}$ was not included in this prototype). The experimental result for a waveform at 56.1Mhz and 400mv of amplitude is shown in Fig. 10.

## VI. CONCLUSIONS

The design of monolithic CMOS OTA–C quadrature oscillators has been addressed. A simple practical OTA macromodel has been used to analyze the influence of OTA parasitics. Design techniques based on this analysis have been applied to obtain high–frequency oscillations (up to 56.1Mhz) using a conventional $3\mu m$ CMOS process. Since the oscillators are voltage–controlled, the design of practical AGC and/or automatic tuning schemes is possible. Furthermore, higher frequencies are expected as better CMOS processes are used.

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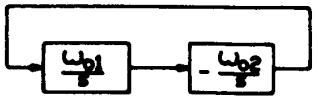

Fig. 1. Two–integrator Loop Quadrature Oscillator

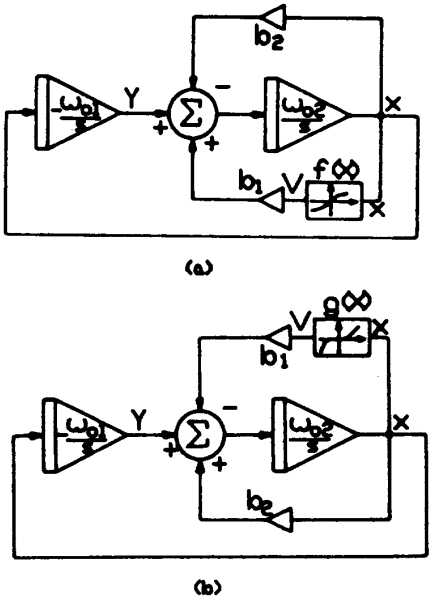


Fig. 2. Possible Block Diagrams of a Practical Quadrature Oscillator

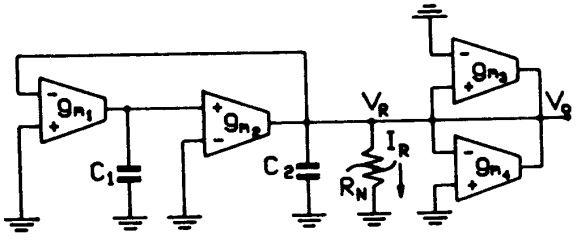


Fig. 3. OTA–C Quadrature Oscillator Structure

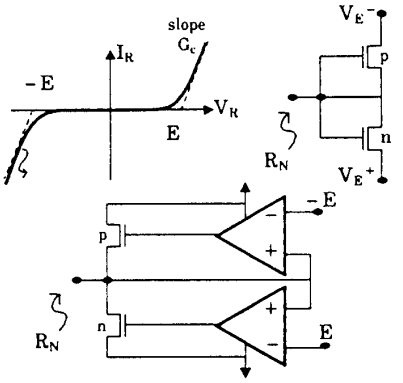


Fig. 4. (a) Nonlinear Resistor Characteristics, (b–c) Alternative $R_N$ Implementations

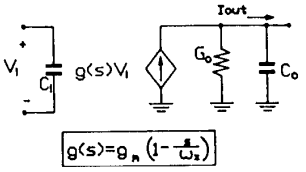


Fig. 5. OTA Macromodel

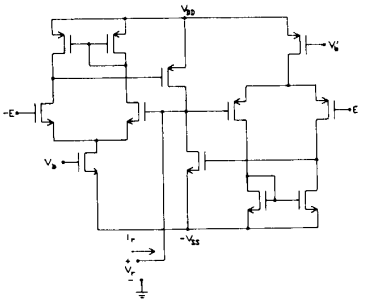

Fig. 6. CMOS Implementations of Fig. 2(c)

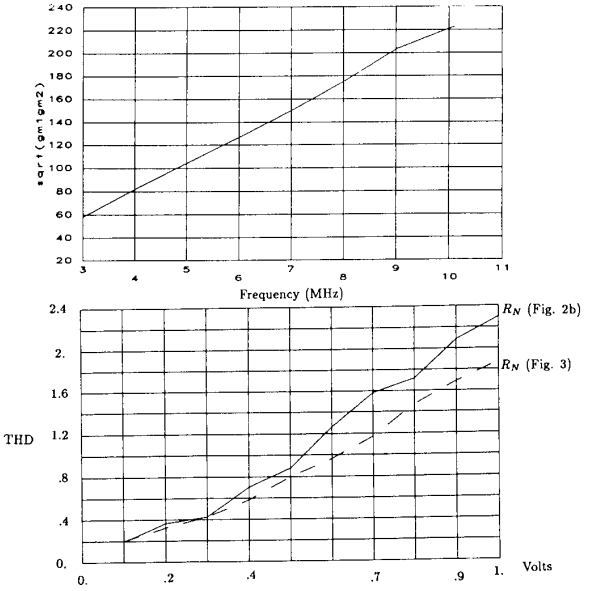


Fig. 7. (a) Measured $(g_{m1}g_{m2})^{\frac{1}{2}}$ vs $f$ for Proto #1, (b) THD vs Amplitude for Two Different Implementations of the Nonlinear Resistor

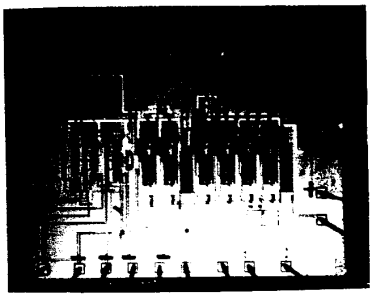

Fig. 8. Photomicrograph of Proto #1.

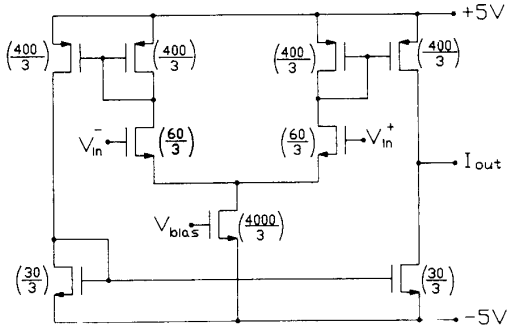


Fig. 9. OTA Architecture for Proto #2

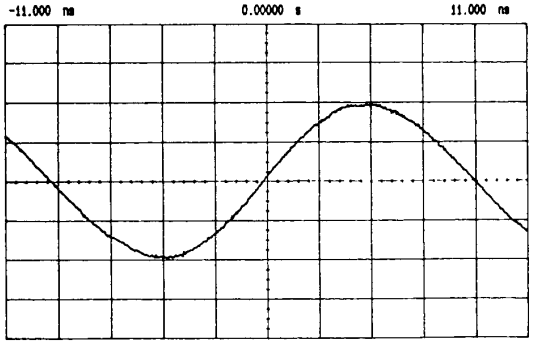


Fig. 10. Waveform at 56.1 MHz, 200 mv Peak-to-Peak

| OTA1-2 volts | OTA4 volts | freq. Mhz |
|---|---|---|
| -2.90 | -3.39 | 56.1 |
| -3.19 | -3.35 | 55.5 |
| -3.40 | -3.35 | 50.5 |
| -3.51 | -3.37 | 46.1 |
| -3.61 | -3.41 | 40.9 |
| -3.68 | -3.51 | 38.2 |
| -3.80 | -3.66 | 31.3 |
| -3.88 | -3.80 | 24.3 |
| -3.96 | -3.84 | 12.4 |
| -3.98 | -3.86 | 12.0 |

Table 1. Oscillation Frequency and Corresponding OTA Bias