CMOS Analog Neural Network Systems Based On Oscillatory Neurons

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Abstract

This paper addresses the design of two neural network systems based on the use of pulsing neurons. Each neuron is built as a simple voltage controlled oscillator (VCO) whose control voltage makes the circuit to oscillate or not. The interconnecting synapses between neurons are made with programmable transconductance amplifiers. The weight of each synapse is represented by the transconductance gain of the amplifiers, and is externally adjustable for each synapse. Using this technique a 5-neurons Hopfield network and a 6-neurons BAM network were built and tested, using standard 2μm double-metal, double-polysilicon CMOS (MOSIS) chips.

I. Introduction

During the last years intensive research has been performed in the area of neural network systems and their applications. Also some efforts have been invested exploring hardware implementations of these neural network systems, mainly because a good specialized hardware would exploit much more efficiently and faster the potential of neural network based systems. Most of the efforts in hardware are oriented towards the construction of special purpose digital computers for applications with neural networks (see for example [1]-[4]), and fewer people are researching on analog implementations for neural networks [5]-[12]. However, very few people are looking for hardware implementations based on pulsing models of the neurons [13]-[17]. The reason might be that at this moment it is not sufficiently clear what the advantages of neural systems based on pulsing neurons might be, even though the living brains use such neurons.

On one hand, one obvious reason that justifies the use of pulses is that, since such systems operate on the basis of averaging principles, they are inherently more tolerant to imperfections and nonidealities in the components.

On the other hand, one of the biggest problems in hardware neural network implementations is the efficient storage of the vast amount of synaptic weight values of neural network systems. Although we don't address such a problem in this paper, may be we can justify the use of pulsing neural network systems as candidates to produce very efficient weight storage networks.

In digital implementations of neural network systems the storage problem is solved using conventional RAMs or DRAMs. In analog implementations of non-pulsing neuron models, the storage problem is not easy.

Some short term storage techniques of analog values on capacitors have been proposed [18]-[19], or long term storage techniques on floating gates MOS devices [19]-[21]. For analog signals, the floating gate approach requires the use of some extra circuitry in order to generate some pulsing signals which produce the tunneling effect and the change stored information. However, if a neural network hardware were used based on oscillatory neurons the pulses necessary to program the floating gate devices would be already available in the signal paths of the network, therefore simplifying greatly the programming circuitry of the floating gate devices.

In this paper we will present first a VCO to be used as the neuron. Then we will show an interconnection technique for these neurons based on transconductance programmable synaptic devices. After this we will give experimental results of 2μm double-metal, double-poly CMOS (MOSIS) prototypes of a 5-neurons Hopfield network and a 6-neurons BAM network.

II. The Oscillatory Neuron Circuit

In a biological living neuron the electric impulses transmitted between neurons are generated as a consequence of the electrochemical dynamics of the neurons cell membrane. This cell membrane is doped all over with chemically and electrically gated biochemical channels which allow the flow of certain electrolytes from the inside to the outside, and vice versa, of the membrane. These flows are actual electrical currents, which depend on electrical impulses received from other neurons. In 1952 Hodgkin and Huxley [22] gave an equivalent electrical circuit for the behavior of the nervous cell membrane (see Fig.1), where the transconductances G_{Na} and G_K where governed by first order nonlinear differential equations. In the early 60's FitzHugh and Nagumo [23],[24] proposed a simplification of Hodgkin-Huxley's model with the same basic qualitative behavior. This model is shown in Fig.2. In [25] the authors showed that the FitzHugh-Nagumo neuron description can be extrapolated to a hysteresis based description [9],[26], as shown in Fig.3

$$H(x) - f(x) = C\dot{x} \tag{1}$$

where the functions $H(x)$and $f(x)$ are depicted in Fig.4.

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Depending on the saturation value of $f(x)$ the circuit can be made to oscillate (if $f(x)=f_2(x)$ in Fig.4) or not (if $f(x)=f_1(x)$ in Fig.4). A CMOS circuit that would perform this operation is shown in Fig.5 [27]. The experimentally measured input-output behavior of this circuit is shown in Fig.6.

III. Interconnection Strategy for Oscillatory Neurons

Most of the neural network systems can be described by the following set of continuous-time first order differential equations[1],

$$\dot{x}_i = -\frac{1}{\alpha}x_i + I_i + \sum_{j=i}^{N} w_{ji} f(x_j) \qquad i = 1, \ldots N \qquad (2)$$

where x_i is the activity of each neuron, I_i its external input, $f(x_i)$ its output, and w_{ji} the weight of the synaptic interconnection from neuron j to neuron i. Usually the function $y_i=f(x_i)$ is a sigmoidal continuous time one. If the element that implements $f(\cdot)$ is substituted by our oscillatory neuron, as is shown in Fig.7, the dynamics of the system will be more complicated now, but the qualitative behavior remains the same. The outputs of the neurons will fire a sequence of pulses if the neuron is on, or will produce no pulses if it is off. These pulses, correspondingly weighted by the synapses, will be summed and integrated at the input capacitors of the neurons, and a voltage level will be developed at each capacitor. Depending on whether or not this voltage is beyond the threshold value, the corresponding neuron will be on or off.

In the following section we have used the neurons of Section II together with the synaptic interconnections of Section III to build a 5-neurons Hopfield network and a 6-neurons BAM network.

IV. Experimental Results

Fig.8 shows the circuit schematic of the transconductance multiplier used as a synapse in our networks. V_{bias} is adjusted to the same value for all the synapses in the network, and the weight is adjusted independently for each synapse between the 'Y' and 'GND_{bottom}' terminals. The input to the synapse is connected between the 'X' and 'GND_{top}' terminals, and I_{out} provides the output current. Fig.9 shows the DC transfer curves of this synaptic circuit for different weight voltages.

The interconnection topology for implementing a Hopfield network is already shown in Fig.8. The pattern '10101' was stored into the network. Fig.10 shows the stable output pattern obtained for all possible inputs. As can be seen, the output always settles to either pattern '10101' or its complementary '01010' depending on the hamming distance between the input and the stored pattern. Fig.11 shows the convergence to pattern '10101' for one of the inputs.

For a BAM network, the interconnection topology is shown in Fig.12. We implemented a 6-neurons BAM (3 neurons per layer) and stored the pattern given in Fig.13. Fig.14 shows the convergence to the stored pattern for all neurons inputs and outputs.

1. Grossberg provides a method [28] to map a discrete-time description of a neural system into a continuous-time one, and vice versa.

V. Conclusions

This paper addresses the issue of neural network hardware implementations based on oscillatory neurons. The approach is justified by highlighting the possible advantages of the use of this approach when using floating gates devices to store analog weight values. The oscillatory neuron model is obtained after successive simplifications of biological neuron models, and is used afterwards to build a complete programmable Hopfield and BAM network. Prototypes were fabricated and tested using a standard 2μm, double metal, double-poly CMOS process (MOSIS).

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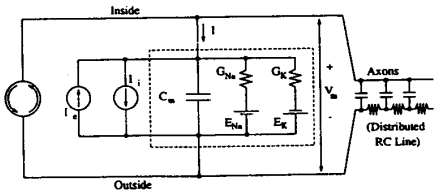

Fig. 1. Biological Neuron Electrical Circuit Model

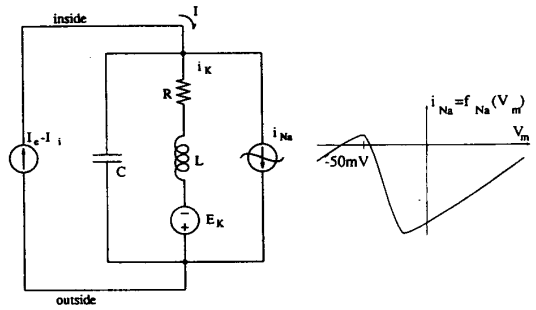

Fig. 2. Equivalent Circiut for FitzHugh-Nagumo Neuron Model

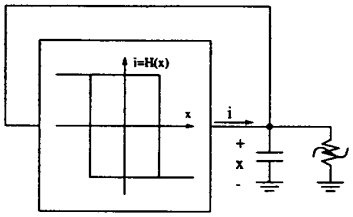

Fig. 3. Block Diagram of Hysteresis Based Neuron Model

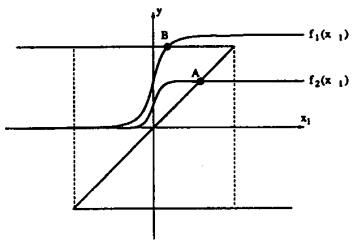

Fig. 4. Nonlinear Functions of Hysteretic Neuron Model

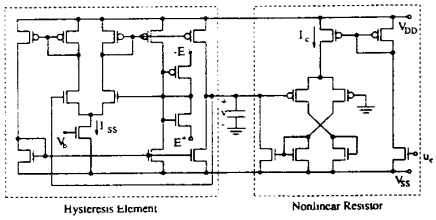

Fig. 5. CMOS Circuit for Hysteretic Neuron Cell

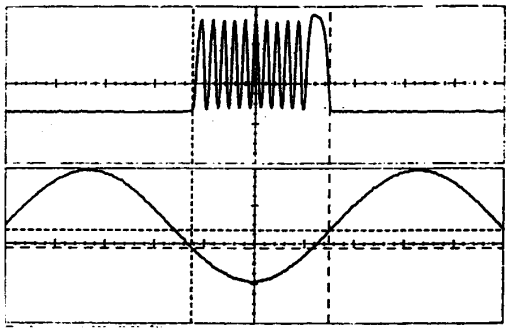

Fig. 6. Input Output Behavior of Oscillatory Neuron

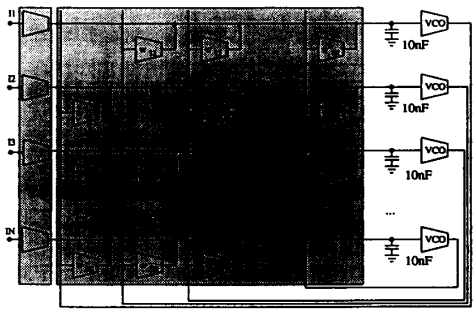

Fig. 7. Interconnection Topology for Oscillatory Hopfield Network

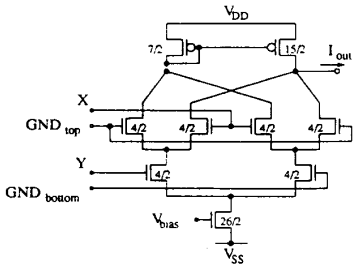

Fig. 8. Synaptic Multiplier Circuit

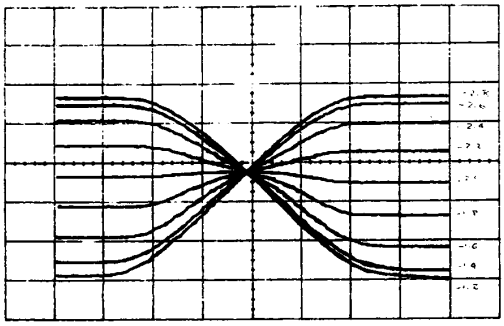

Fig. 9. Measured DC Transfer Curves of Multiplier Synaptic Cell

Input		Stable Pattern	
(0)	00000	01010	(10)
(1)	00001	10101	(21)
(2)	00010	01010	(10)
(3)	00011	01010	(10)
(4)	00100	10101	(21)
(5)	00101	10101	(21)
(6)	00110	01010	(10)
(7)	00111	10101	(21)
(8)	01000	01010	(10)
(9)	01001	01010	(10)
(10)	01010	01010	(10)
(11)	01011	10101	(21)
(12)	01100	01010	(10)
(13)	01101	01010	(10)
(14)	01110	01010	(10)
(15)	01111	10101	(21)
(16)	10000	10101	(21)
(17)	10001	10101	(21)
(18)	10010	01010	(10)
(19)	10011	10101	(21)
(20)	10100	10101	(21)
(21)	10101	10101	(21)
(22)	10110	01010	(10)
(23)	10111	10101	(21)
(24)	11000	01010	(10)
(25)	11001	10101	(21)
(26)	11010	01010	(10)
(27)	11011	01010	(10)
(28)	11100	01010	(10)
(29)	11101	10101	(21)
(30)	11110	01010	(10)
(31)	11111	10101	(21)

Fig. 10. Measured Stable States for Oscillatory Hopfield Network Loaded with Pattern '10101'

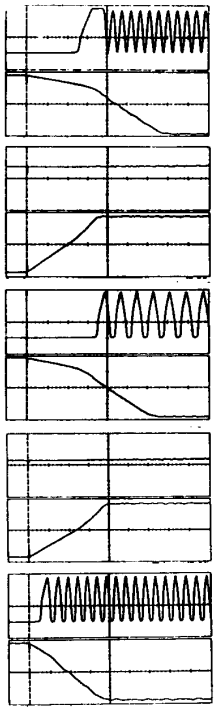

Fig. 11. Convergence to Pattern '10101' for Oscillatory Hopfield Network; Inputs and Outputs of all 5 Neurons Are Shown

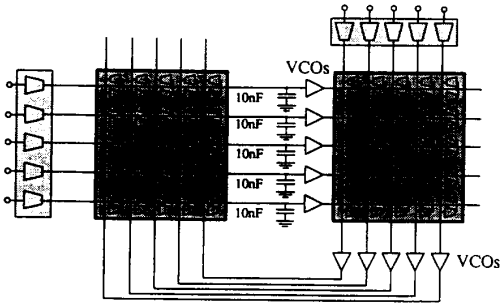

Fig. 12. Interconnection Topology for Oscillatory BAM

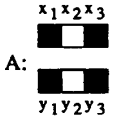

Fig. 13. Pattern Stored in Oscillatory BAM

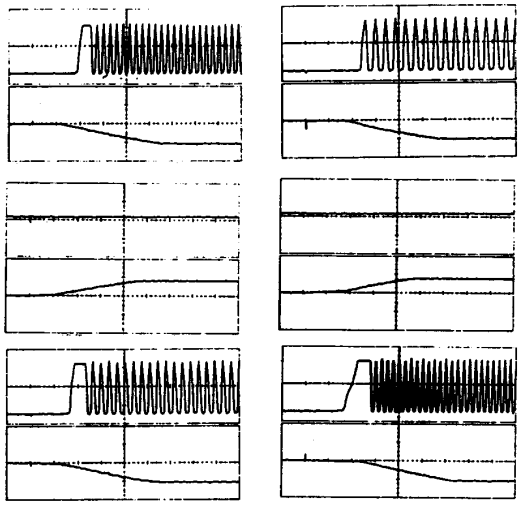

Fig. 14. Convergence to Stored Pattern for Oscillatory BAM; Inputs and Outputs of all 6 Neurons Are Shown