A PIECEWISE-LINEAR FUNCTION APPROXIMATION USING CURRENT MODE CIRCUITS

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Abstract. A methodology to design current-mode circuits for piecewise-linear function approximation is presented. The technique is based on the utilization of current mirrors as basic building blocks. The resulting circuits are very compact, modular, programmable and can operate at very high frequencies. Experimental results are presented that verify the proposed theoretical technique.

I. INTRODUCTION

Nonlinear circuits are required for many applications, i.e. to linearize the nonlinear transfer characteristic of many types of sensors, in neural networks, in companding A/D and D/A converters, etc. Nonlinear transfer characteristics can be approximated piecewise-linearly using electronic circuits. These have been traditionally implemented with operational amplifiers, diodes and resistors connected in closed loop (feedback) configurations [1]. In these circuits, variables are represented by voltage signals. They have fixed transfer characteristics and poor high frequency performance. Recently a new methodology to synthesize nonlinear circuits was reported [2]. This technique is based on the utilization of Operational Transconductance Amplifiers (OTAs) as basic elements to implement nonlinear functional blocks which include, among others, multipliers and circuits for piecewise-linear (PWL) function approximation. These circuits use the OTA in open loop configurations and operate in "transconductance mode", that is, some of the variables are represented by voltage signals and some by current signals. They have fully programmable characteristics (breakpoints and slopes of all segments are voltage programmable) and they have very good high frequency performance. One drawback of these circuits is that they are relatively silicon area intensive, since a linear OTA is required for each segment of the piecewise linear characteristic. Linear OTAs have relatively complex structures.

In this paper a methodology for piecewise-linear (PWL) approximation using current mode circuits with very simple topologies is presented. Current mode because all variables in these circuits are represented by current signals. In this technique current mirrors are used as basic building blocks. In section II the current mode PWL approximation technique is introduced. Section III discusses improvements to the basic technique. Section IV shows experimental results and conclusions are given in section V.

II. DESCRIPTION OF PWL APPROXIMATION TECHNIQUE

Fig. 1 shows the four basic building blocks used to implement current mode PWL approximation circuits. These blocks are denoted TP(I1,I2), TN(I1,I2), BP(I1,I2) and BN(I1,I2). The transfer characteristic for each block (defined in terms of output current I_{out} vs. input current I_{in}) is also shown in Fig. 1. These basic building blocks are current mirrors. They approximate ideal current rectifiers, DC currents I1 and I2 on the input and output sides of each circuit building block are used to shift the rectifying characteristic to any arbitrary position. Broken lines show the transfer characteristics for the case where I1 and I2 are zero. In this case, the breakpoint of the transfer characteristic is at the origin. From a large signal point of view a current mirror behaves as an ideal current rectifier. This is a basic advantage over OTA based circuits where a linearized OTA and a diode are required to implement an ideal rectifier. The polarity of the transistors determines the quadrant where rectification takes place. The slope of the transfer characteristic corresponds to the gain of the mirror, which is determined by ratios of transistor geometries. Current mirrors have negative gain, positive current gains (slopes) are obtained by cascading two current mirrors as shown in Fig. 1. Topologies using bipolar transistors are identical and for this reason are not shown.

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For PWL approximation, a number of building blocks equal to the number of segments of the PWL transfer characteristic is used. The individual output currents of all blocks are added in a common (low impedance) load. The input currents of each block are all replicas of the input signal current I_{in}. These replicas are easily generated using current mirrors with multiple outputs or, if the input signal is available as a voltage signal, by using a multiple output OTA. The transfer characteristic results from simply adding the transfer characteristics of each of the individual building blocks.

As example to illustrate the proposed technique, Fig. 2 shows block diagrams and actual CMOS implementations of a) an absolute value circuit, b) a "dead zone" circuit, c) a limiter circuit and d) a circuit with a three segment characteristic, one of them having negative slope

Some advantages of the proposed technique are: 1) circuits are open loop configurations, so that, they are unconditionally stable, 2) there are only low impedance nodes in the signal path, and for this reason the circuits have very good high frequency performance, 3) the simplicity and modularity of the circuits, makes them very appropriate for a CAD-VLSI implementation, 4) the small number of transistors required for each block, 5) the inherent programmability of the breakpoints of each segment, 6) the possibility to operate with low supply voltages (+-2.5 V) due to the simplicity of the circuits.

III. IMPROVEMENTS TO BASIC TECHNIQUE

Circuits with programmable slopes can also be implemented using linear programmable current mirrors with either bipolar transistors or MOS transistors operating in weak inversion [6]. These circuits have voltage (or current) programmable gain and a linear rectifying characteristic. Other programmable MOS current mirrors previously reported [7], are not linear and for this reason can not be used as building blocks for the proposed approach. Offset and nonlinearities due to channel length modulation (or Early voltage) effects can be reduced by using cascode and/or regulated cascode current mirrors [8].

Class AB configurations can be used to avoid node saturation and improve high frequency performance [3]-[5]. The delay required to discharge parasitic capacitances of saturated nodes is the main factor that limits high frequency operation of these circuits [2]. In the class AB current mirror of Fig. 3 no nodal saturation takes places since there is always a path for the input current to flow. This circuit can be used as a generalized class AB circuit building block. It can generate (unrectified) replicas of the input current signal (output a), and simultaneously positive and negative rectifying outputs (outputs b and c respectively). Class AB mirrors also minimize quiescent power consumption since the amplitude of the signal currents is not limited by the bias currents. The outputs of this circuit can be replicated as many times as necessary (for example to produce replicas of the input current as required in Fig. 2) and geometry scaled to any desired gain value.

IV. EXPERIMENTAL RESULTS

Fig. 4 shows the experimental DC transfer characteristics of the absolute value and the "dead zone" circuits of Fig. 2a and 2b. The circuits were implemented using CA3096 bipolar transistor arrays. Fig. 4a shows the input and output waveforms of the absolute value circuit of Fig. 2a . Fig. 4b shows the input and output waveforms, Fig. 4c the transfer characteristic of the dead zone circuit of Fig. 2b (not shown but also experimentally verified was the expected change of the width of the dead zone with changes in the bias currents I_x). For testing purposes, a 2 V_{p-p}, 10 kHz sinusoidal input voltage signal was transformed into a current signal using a two-output OTA (implemented also using CA3096 transistor arrays and according to the scheme of [6]) with 1 mA/V transconductance gain. A 1.2 kΩ load was used to sense the output current of the PWL circuit. Supply voltages of +-2.5V were used. High frequency effects started to become noticeable above 100 kHz, SPICE simulations indicate the potential of CMOS versions of these circuits on-chip to operate at 20 MHz using class AB mirrors and in 2 μm CMOS technology.

V. CONCLUSIONS

An efficient technique to implement current mode piecewise linear circuits was presented. The circuits are very compact, modular, and have very good high frequency performance. The technique is appropriate to implement adaptive non linear analog VLSI circuits. Experimental results have verified the proposed technique.

REFERENCES

[1] Ed. D. Sheingold,"Nonlinear Circuits Handbook", Ch.6, Analog Devices Inc., Norwood, MA, 1974.

[2] E. Sánchez-Sinencio, J. Ramírez-Angulo and B. Linares Barranco, "OTA-Based Nonlinear Function Approximation", *IEEE Journal of Solid State Circuits*, vol. 24, No. 6, pp. 1576-1586, December 1989.

[3] J. Ramírez-Angulo, "A Precision Broadband Voltage Rectifier in CMOS technology", *IEEE International Symposium on Circuits and Systems*, New Orleans, Lousiana, May 1-3 1990, pp. 1724-1727

[4] Z. Wang, "Wideband Class AB (Push-Pull) Current Amplifiers in CMOS Technology", *Electronic Letters*, vol. 26, No. 8, April 1990, pp. 543-545

[5] Ed. C. Tomazou, F. Lidgley and D. G. Haigh, "Analog IC Design: The Current Mode Approach", IEE 1990.

[6] J. Ramírez-Angulo and I. Grau, " Highly linear OTA with Wide g_m Adjustment Range Highly Linear OTA with Linear Programmable Current Mirrors", *IEEE International Symposium on Circuits and Systems*, San Diego, CA, May 10-12, 1992.

[7] E. A. Klumpernik and E. Seevinck, "MOS Current Gain Cells With Electronically Variable Gain and Constant Bandwidth", *IEEE J. Solid State Circuits*, vol. 24, No. 5, pp. 1465-1467, October 1989.

[8] E. Säckinger and W Guggenbühl, "A High Swing, High impedance MOS Cascode Circuit", *IEEE J. of Solid State Circuits*, vol. 25, No. 1 pp. 289-298, February 1990.

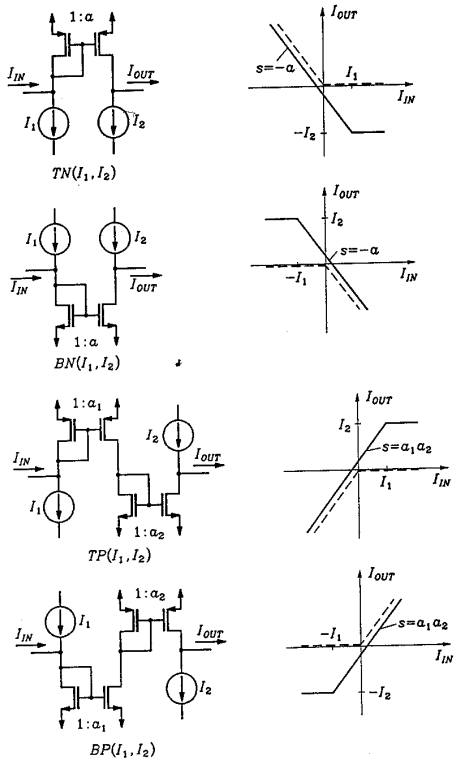

Fig. 1 Basic building blocks for current-mode piecewise-linear approximation

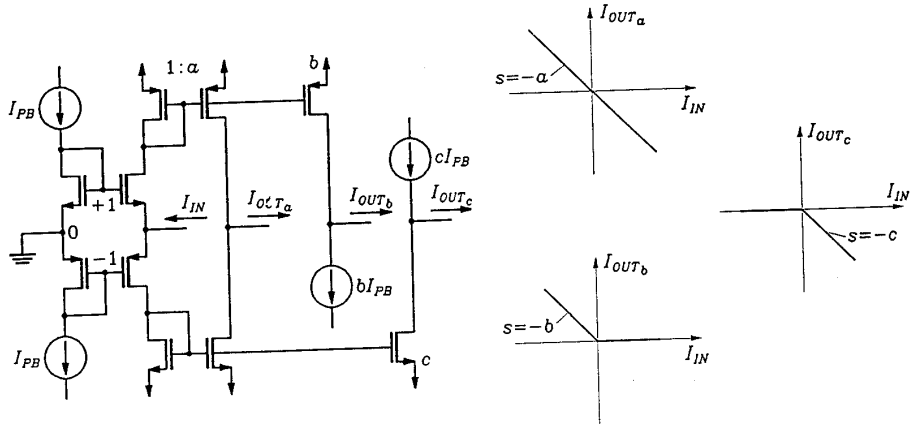

Fig. 3 Class AB current amplifier with: nonrectifying, positive rectifying, and negative rectifying outputs

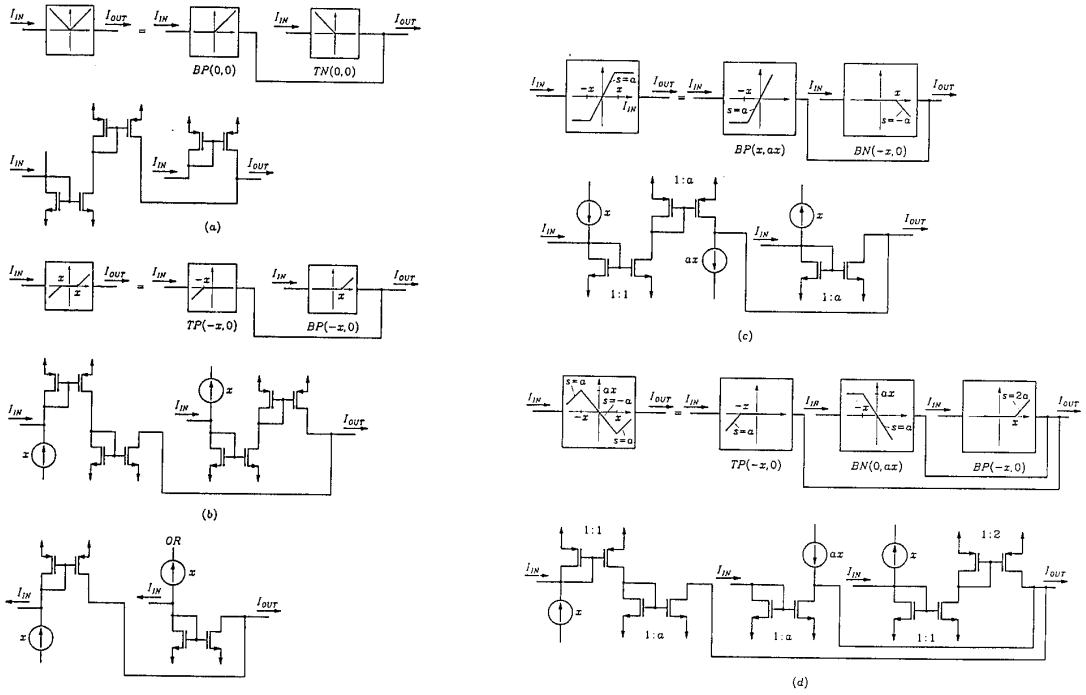

Fig. 2 Generation of nonlinear characteristics using proposed technique (a) Absolute value function (b) "Dead zone" circuit, (c) Limiter, (d) Negative slope circuit

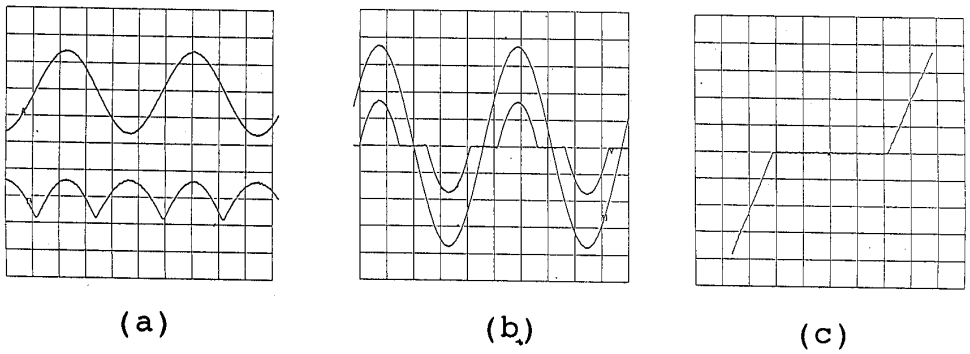

Fig. 4 Experimental results: (a) input and output waveforms of absolute value circuit (b) input and output waveforms of "dead zone" circuit (c) transfer characteristic of "dead zone" circuit