A Tool for Automated Design of Sigma-Delta Modulators using Statistical Optimization

F. Medeiro, B. Pérez-Verdú, A. Rodríguez-Vázquez and J.L. Huertas

Dept. de Diseño de Circuitos Analógicos. Centro Nacional de Microelectrónica.

Edificio CICA. Avda. Reina Mercedes s/n. 41012-Sevilla (Spain).

***Abstract*-A tool is presented which starting from high-level specifications of SC ΣΔ modulators (resolution, bandwidth and oversampling ratio) calculates first optimum specifications for the building blocks (opamps, comparator, etc.), and, then, optimum sizes for their schematics. At both design levels (high-level synthesis and cell dimensioning), optimization is performed via using statistical techniques and innovative heuristics, which allow global design (independent on the initial conditions) and increased computer efficiency as compared to conventional statistical optimization techniques. The tool has been conceived to be flexible at the high-level part (via the use of an architecture independent, behavioral modeling approach) and completely open at the cell-design part. Performance of the tool is demonstrated via the automatic design of a 16bits-dynamic range, 8Khz second-order SC ΣΔ modulator in 1.2μm CMOS technology, for which measurements on a fabricated prototype are reported.**

INTRODUCTION

The continuous evolution of integrated circuit technology during the last decade has paved the way for the monolithic implementation of complete systems, including massive signal processing and control *digital* circuitry together with the *analog* interface circuitry, on a common silicon substrate. In this way, application specific integrated circuits (ASICs) with full custom operability can be designed for areas of strong economic interest like communications, data recovery, and the like [1]. It has motivated a continuous increase of the percentage of mixed ICs in the ASIC marketplace, a percentage which is foreseen to double during this decade, to approximately 45% for the late 90's.

The trend towards mixed A/D microelectronic design has been reinforced due to the availability of innovative circuit design techniques providing *high resolution* in standard digital technologies and with no trimming requirements. In particular, *oversampling converters*, and more specifically ΣΔ *modulation* structures, provide a very convenient vehicle for the implementation of data converters with resolution levels up to 20bits for instrumentation application [2], and 16bits [3], and more [4], for audio applications. Also, a major trend can be identified today towards the extended application of oversampling methods to higher signal frequencies by using proper system level architectures [5].

Manual ΣΔ modulator design, and in general manual analog circuit design, can hardly meet the cost and time-to-market constraints for successful A/D ASIC production. Hence, analog design automation becomes a must to make A/D ASIC design economically feasible. Most of the previously reported analog design tools have focused on cell design (mainly operational amplifiers) [6] and are, typically, closed systems, where automation is only available to a reduced set of topologies. In [7] the authors have proposed a new methodology to design analog cells, which is intrinsically open and requires only minimal designer interaction, thus making the design of arbitrary analog cell schematics available to nonexpert analog designers. In this communication, this methodology is extended to include the automated design of ΣΔ modulators, from the high-level converter specifications to the sizes of the analog cells. Some major features of the proposed tool are:

a) Flexible *high-level synthesis* (calculation of the cell specifications from the modulator system-level specifications), achieved through the use of *behavioral* representations for the different noise and nonidealities which limit ΣΔ modulator resolution. Equations supporting these behavioral representations has been obtained via exhaustive noise analysis of general switched-capacitor circuits, and, more specifically, of SC ΣΔ modulators.
b) Use of a *simulation based*, intrinsically open approach for the sizing of the *analog cells*. This allow nonexpert designers to size complex cell architectures, as requested for demanding ΣΔ modulator specifications.
c) *Optimum global* design, achieved by the use of *statistical optimization* techniques and *innovative heuristics* (variable scale for random displacements in the parameter space, nonmonotonic temperature, DC operating point precalculation for cell sizing, etc.) to reduce the influence of initial parameter estimates and to improve computational efficiency. These innovative heuristics allow to reduce the total iteration count for optimization by, at least, one order magnitude as compared to conventional simulated annealing algorithms.
d) Possibility for fast *exploration* of the design parameter space for modulator architectures, as a way to provide insight on involved specification trade-offs and calculation of the architecture theoretical limits owing to the requirements imposed on the analog cell specifications.

SIGMA-DELTA MODULATORS DESIGN FLOW

A ΣΔ modulation-based analog-to-digital converter comprises two major blocks: the analog *modulator* and the digital *decimation* filter. This communication focuses on the analog modulator. Fig.1 presents a conceptual diagram of the operation flow for the design of ΣΔ modulators. First, a convenient architecture must be selected according to the requested high-level converter specifications (signal baseband, resolution and oversampling ratio). By the way of example, Fig.2 shows a second-order SC ΣΔ modulator [8]. Then, these high-level specifications must be mapped into corresponding terminal

0-7803-1254-6/93$03.00 © 1993 IEEE

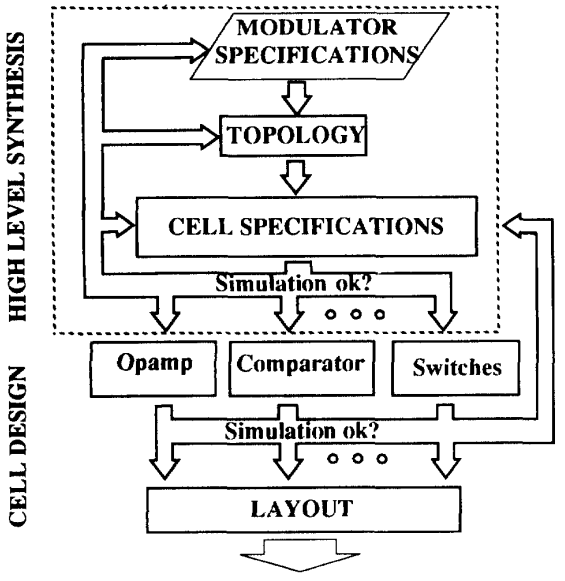

Fig. 1:ΣΔ Modulator Design Flow

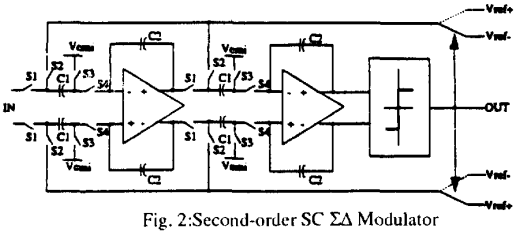

Fig. 2:Second-order SC ΣΔ Modulator

specifications for the analog cells used in the modulator circuit architecture: opamps, comparators, switches, etc. (see Fig.2 for illustration). Next, convenient cell topologies must be selected and sized to meet the required terminal specifications. Finally, a layout of the modulator must be generated according to the calculated sizes. With the exception of the layout phase (whose importance to achieve proper converter operation cannot be underestimated) the remaining steps in Fig.1 involve advanced electrical modeling and nonlinear circuit analysis techniques, as well as solving highly nonlinear problems found in large dimension design parameter spaces. Consequently, manual ΣΔ modulator design is available only to expert analog designers and requires long design cycles, even for these experts. These observations are especially pertinent if large, and typically overdetermined parameter spaces must be explored for optimum achievement of the design objectives associated with demanding designs.

TOOL ARCHITECTURE OUTLINE

Fig.3 is a block diagram for the part of the tool dedicated to high-level synthesis, where an inner *equation based* optimization loop supervised by a outer simulation based monitoring loop are implemented. Behavioral models for the simulation loop are automatically generated by the tool. Simulators considered are TOSCA [9], a special purpose SC ΣΔ simulator developed at Pavia University, and HSPICE [10]. Table I gives an overview of the different noise contribution considered [11].

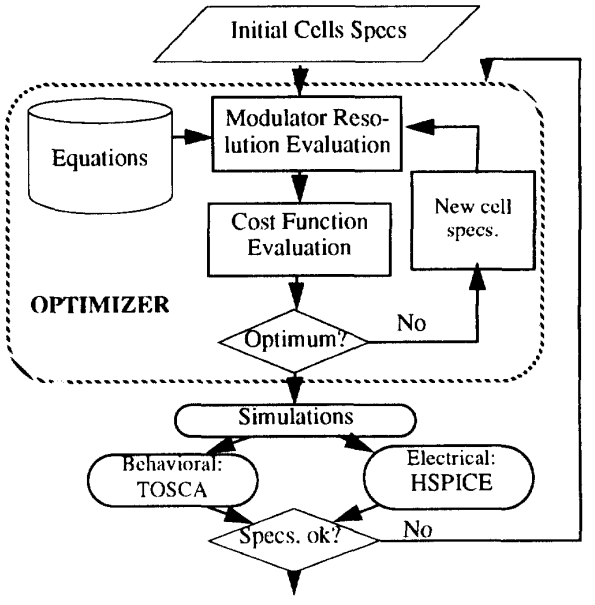

Fig. 3: Proposed Tool Block Diagram

Fig.4 is a block diagram for the part of the tool dedicated to cell design, which is *simulation based*.

The formulation of the cost function for the optimization process is similar for the high-level synthesis part and the cell design part. Assume, for illustration purposes, a general case where the circuit is targeted to achieve a number of *performance specifications* (for instance, $A_o \geq 80$dB, $SR \geq 10$V/μs, etc.) together with some *design objectives* (minimum area or power, maximum bandwidth, etc.). Mathematically this can be formulated as a multi-objective constrained optimization problem,

$$\begin{aligned} &minimize && \Psi_i(\underline{x}) && , 1 \leq i \leq P \\ &subjected\ to && \begin{pmatrix} Y_j(\underline{x}) \geq Y_{jE} \\ Z_k(\underline{x}) \leq Z_{kE} \end{pmatrix} && \begin{matrix} , 1 \leq j \leq Q \\ , 1 \leq k \leq R \end{matrix} \end{aligned} \quad (1)$$

where Ψ_i denotes the value of the *i-th* design objective; Y_j and Z_k denote values of the circuit specifications; and Y_{jE} and Z_{kE} are their targets (for instance, $A_o \geq 80$dB, settling time≤ 0.1μs).

Two different types of specifications are considered: *strong* and *weak*. Strong specifications correspond to critical performance characteristics, without relaxation allowed. For weak specifications, the targets can be relaxed to the extent controlled by the value of associated weight parameters.

No cost function is formulated for those regions where strong specifications are violated. Outside these regions, the cost function is defined in the *minimax* sense, as follows

$$minimize\,(\Phi(\underline{x}) = max\{F_{\Psi_i}(\Psi_i), F_{Y_j}(Y_j), F_{Z_k}(Z_k)\}) \quad (2)$$

where the *partial* cost functions $F_{\Psi i}(\bullet)$ and $F_{Yj}(\bullet)$ are:

$$\begin{aligned} F_{\Psi_i}(\Psi_i) &= -\sum_i w_i \log(\Psi_i) \\ F_{Y_j}(Y_j) &= -K_j(Y_j, Y_{jE}) \log\left(\frac{Y_j}{Y_{jE}}\right) \end{aligned} \quad (3)$$

TABLE I:
NOISE CONTRIBUTIONS AND NONIDEALITIES INCLUDED

OR=oversampling ratio; G_i=integrator gain; C_{SAMP}=sampling cap.; PSD_W=white noise spectral density at the opamp input; T_R=comparator resolution time; L_C= capacitor nonlinearity; A_0=opamp DC gain; **GBW**=opamp gain-bandwidth product; **SR**=opamp slew-rate; **OS**=opamp output swing; R_{ON}=analog switch on resistance

SPECS	Quantization	Incomplete Settling	Thermal	Harmonic Distortion	
OR G_i C_{SAMP}	•	• • •	• •		Integrators
A_0 GBW SR OS PSD_W	•	• • •	• •	• •	Opamps
Hysteresis T_R	•			• •	Comparator
R_{ON}		•	•		Switches
L_C				•	Technology

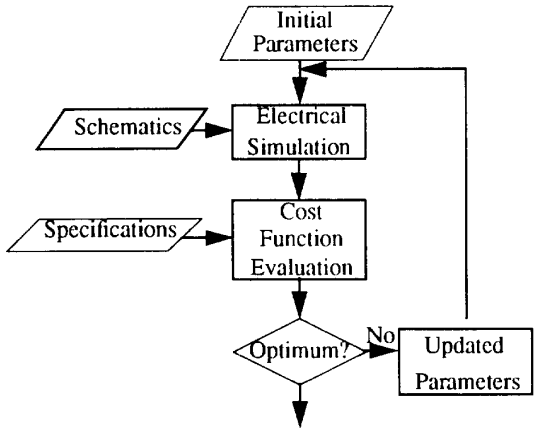

Fig. 4: Simulation based cell design concept

where w_i is a positive real number and for $K_j(\bullet)$ we have,

$$K_j(Y_j, Y_{jE}) = \begin{cases} k_j & , k_j Y_j < k_j Y_{jE} \\ -\infty \operatorname{sgn}(k_j) & , otherwise \end{cases} \quad (4)$$

with k_j positive real. Functions $F_Z(\bullet)$'s are defined as $F_Y(\bullet)$'s but with negative weight values. Weight parameters are used to give priority to the associated design objectives and weak specifications.

Updating of the design parameters among interations is done heuristically, following *statistical optimization* principles. An updating vector, Δx, is *randomly* generated at each iteration. The value of the cost function is calculated at the new parameter space point and compared to the previous one. The new point is accepted in case the cost function has a lower value. It may also be accepted in case the cost function increases, according to a *probabilist function* depending on a *temperature parameter*, T. This probability of acceptance changes during the process, being high at the beginning (for large T) and decreasing as the system *cools* (decreasing T). As mentioned previously, several innovative heuristics have been developed to increase efficiency of this process as well as to make it independent of the initial estimate of the parameter values.

PRACTICAL RESULTS

The ΣΔ modulator of Fig.2 was designed automatically to meet the system level specifications of Table II, in a 1.2μm n-well double poly double metal CMOS technology.

Table II shows the results of the high-level synthesis, obtained after 10^4 iterations in 5s CPU time on a SUN Sparcstation, starting from a randomly selected point in the design parameter space. This table shows optimized specifications for the analog cells, together with some technological requirements and a summary of the different noise figures. Fig.5 showS the analog cell schematics used for the physical design of Fig.2. These schematics were automatically sized, using the cell design part of the tool, for optimum achievement of the specifications in Table II. The sizing process started also from a random point and took about 1 hour CPU time per cell.

Area of the core modulator in the fabricated prototype is about 0.98 mm². Tables III(a) and (b) show measurement results for the opamp and comparator. Slight deviations in GB of the opamp and TP's of the comparator are due to inexact calculation of the load capacitor value, since a protoboard breadboard was used for testing, and buffering to the output nodes was not provided in the circuitThe modulator was tested by performing the FFT of sequences of 65,536 consecutive output samples (acquired via an HP82000 unit) for an input tone of 8Khz (signal source second harmonic level was -90dB below the first) and using different signal amplitudes. A summary of

TABLE II:
OUTPUT OF THE HIGH-LEVEL SYNTHESIS PROCESS

```
*** OPTIMIZED SPECS FOR:        Signal Baseband  = 8.000000e+03 Hz
                                Resolution       = 16.00 bits
                                Ref. Voltage     = 3.00 v
                                Unit Capacitance = 1.00 pF

** MODULATOR **
   Order = 2
   Sampling Frequency (Hz) = 4.096000e+06
   Oversampling Factor = 256

** INTEGRATOR **
   Sampling Capacitor (pF) = 1.00
   Integrator1 Gain = 0.50
   Integrator1 Gain = 0.50
   MOS Switch- ON resistance (Koms) = 1.8
   Maximum Clock Jitter (s.) <= 3.953e-09

** OPAMP **
   DC-Gain (dB) >= 72.7
   GBW (Mhz) = 1.900e+01
   Slew Rate (V/us) >= 20.00
   Total Output Swing (V) >= 7.00
   Input Referenced White Noise Density (nV/sqrt(Hz)) <= 200.5

** COMPARATOR **
   Hysteresis (V) <= 5.000e-02
   Resolution Time (s) <= 3.052e-08

** TECHNOLOGY **
   Cap Non-linearity (p.p.m.) <= 5.000e+00

*** RESOLUTION & NOISE CONTRIBUTIONS

** Total Noise Power (dBrms) = -91.59
   Equivalent to 16.00 bits or 98.12dB DR

** Quantization Noise (dBrms) = -102.68
** Thermal Noise (dBrms)      = -92.13
** Settling Noise (dBrms)     = -129.98
** Harmonic Distortion Noise (dBrms) = -105.51

*** Number of iterations 10000.
*** CPU time 5.00 s.
```

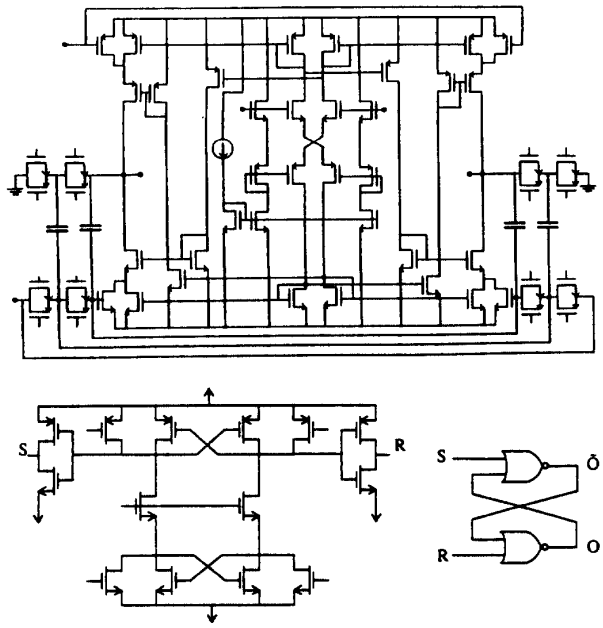

Fig. 5: Opamp and comparator schematics

the measurements performed on the modulator is shown in Table IV, where resolution is calculated according to the definition in [8], the same used for the high-level synthesis tool.

The slight difference regarding the specified 16bits is due to an excessive opamp noise, most probably originated in the measurement setup. Owing to the use of the tool described herein, the design of this modulator was completed in just the time required for the layout, which was very carefully realized by hand in about one week designer work. The high-level synthesis tool is also very useful to explore design spaces of ΣΔ modulator architectures, as it is illustrated by Fig.6, which shows a surface in the design space of a second order ΣΔ modulator.

TABLE III:
SIMULATIONS AND MEASUREMENTS FOR THE CELLS

	Simulated	Measured	Units
A_0	74.9	74.6	dB
GBW	19.7	19.4	Mhz
PM	63.3	65	o
OS	8.0	8.2	V
Input White Noise	44.7	282	nV/√Hz
Power	4.3	4.3	mW

(a)

	Simulated	Measured	Units
Histheresys	40	36.4	mV
TP_{LH}	8	12	ns
TP_{HL}	9	13.9	ns
Offset	-	22.5	mV

(b)

REFERENCES

[1] E. Laes et al.: "Analog-Digital Technologies for Mixed-Signal Processing". *IEEE Micro*, Vol. 12, pp. 34-42, August 1992.

[2] B. P. Del Signore et al.: "A Monolithic 20-b Delta-Sigma A/D Converter". *IEEE J. Solid-State Circuits*, Vol.25, pp. 1311-1317, Dec. 1990.

[3] L. Le Tournelin et al.: "A 5-V CMOS Line Controller with 16-b Audio Converters". *IEEE J. Solid-State Circuits*, Vol. 27, pp. 332-341, March 1992.

[4] P. Ferguson, Jr. et al.: "An 18b 20KHz Dual ΣΔ A/D Converter". *Proc. ISSCC*, pp. 68-69, Feb. 1991.

[5] T. Ritoniemi: "High-Speed 1-Bit ΣΔ–Modulators". *Workshop on Advances in Analog Circuit Design*, pp. 191-203, Delft 1992.

[6] G. Gielen and W. Sansen: "*Symbolic Analysis for Automated Design of Analog Integrated Circuits*". Kluwer 1991.

[7] F. Medeiro et al.: "Simulation Based Automated Analog Design Using Statistical Optimization". *Proc. ESSCIRC'92*, pp. 259-262, Sept. 1992.

[8] B. E. Boser and B. A. Wooley: "The Design of Sigma-Delta Modulation Analog-to-Digital Converters". *IEEE J. Solid-State Circuits*, Vol. 23, pp. 1298-1308, Dec. 1988.

[9] V. F. Dias et al.:"TOSCA: A Simulator for Oversampling Converters whit Behavioral Modeling", User Manual, 1990.

[10] "HSPICE". Meta Sofware Inc. 1988.

[11] F. Medeiro: "*Analysis and Design of ΣΔ Modulators*". PhD dissertation in progress, unpublished.

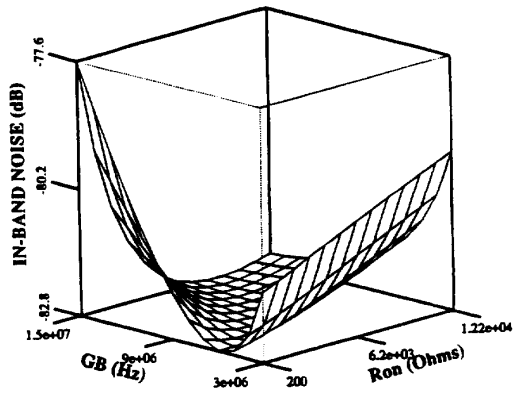

Fig.6: In-band noise vs GB and R_{on} for a second order modulator; OR=256

TABLE IV
MEASUREMENTS FOR THE MODULATOR

Resolution	15.7 Bits
SNR	87 dB
DR	96.3 dB
Supply	5 V
Area	0.98 mm^2