ACE16K: A 128x128 FOCAL PLANE ANALOG PROCESSOR with DIGITAL I/O.

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This paper presents a new generation 128x128 Focal-Plane Analog Programmable Array Processor -FPAPAP-, from a system level perspective, which has been manufactured in a 0.35μm standard digital 1P-5M CMOS technology. The chip has been designed to achieve the high-speed and moderate-accuracy -8b- requirements of most real time -early-vision processing applications. It is easily embedded in conventional digital hosting systems: external data interchange and control are completely digital. The chip contains close to four millions transistors, 90% of them working in analog mode, and exhibits a relatively low power consumption -<4W, i.e. less than 1μW per transistor. Computing vs. power peak values are in the order of 1TeraOPS/W, while maintained VGA processing throughputs of 100Frames/s are possible with about 10-20 basic image processing tasks on each frame.

1 Introduction

The retina, the front-end "device" encountered at *Natural* vision systems is capable to acquire and process the visual information in concurrent manner [1]. Among many other tasks, the early processing realized at the retina serves to extract important features from the raw sensory data and, thus, to reduce the amount of information transmitted to the brain for subsequent processing. In contrast to that, image acquisition and processing are usually separated in conventional *artificial* vision systems. Consequently, these systems become much slower, bulkier and more inefficient that even the simplest natural vision ones.

Biased by Nature's efficiency, during the last few years significant efforts have been made to develop new vision devices capable of overcoming the drawbacks of traditional ones through the incorporation, at the sensory plane, of 2-D *distributed* parallel processors that operate concurrently with signal acquisition [2, 3].

The chip presented in this paper belongs to this general family. However, while most of its relatives are designed for specific functions, the herein reported chip is a *general-purpose* front-end vision device with the following features: 1) a massively parallel 2-D imaging/processing core array consisting of *locally-connected* pixels with embedded optical sensors and digitally-controlled analog processing circuitry; 2) a distributed circuitry for storing locally, pixel by pixel, several 2-D intermediate images; and, 3) stored on-chip programmability.

In addition to the core array, the ACE16K incorporates additional circuitry for control and timing, a fully digital interface, address-event downloading, and on-chip program storage. Hence, the ACE16K is actually a *visual microprocessor* on-chip capable to realize a very large variety of image-related spatio-temporal operations and algorithms through the execution of suitable sequence of instructions – programs [4].

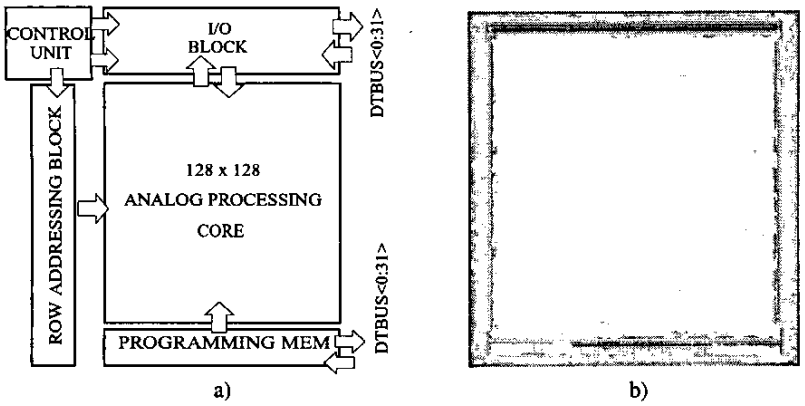

Figure 1. The ACE16K Chip. a) Architecture. b) Microphotography

2 System description

2.1 Architecture

ACE16K can be basically described as an array of 128x128 identical, locally interacting, analog processing units designed for high speed image processing tasks requiring moderate accuracy levels -around 8b-. It contains a set of on-chip peripheral circuitries that, on one hand, allow a completely digital interface with the host, and on the other provide high algorithmic capabilities by means of the use of conventional programming memories.

Despite ACE16K is, essentially, an analog processor, it is digitally controlled. For this purpose, the prototype incorporates DA and AD converters which conform a digital I/O port for images. The chip is conceived to be used in two alternative ways. First, in applications where the images to be processed are directly acquired by the optical input module of the chip [5], and secondly, as a conventional image co-processor working in parallel with a digital hosting system that provides and receives the images in electrical form.

The architecture of the system is sketched in Fig. 1 and contains five functional blocks. 1) The analog processing core, which comprises the inner array of 128 x128 identical cells, a ring of border cells used to establish spatial boundary conditions for image processing, and several buffers driving analog and digital signals to the cell array. 2) A programming block, which contains SRAM digital memories used to store the algorithms to be executed by the chip. Finally, blocks third to fifth are dedicated to -electrical form-images I/O tasks. It contains a global I/O control unit which generates the signals required for I/O image accesses, row and column addressing signals, and the control of the Digital-to-Analog and Analog-to-Digital I/O converters bank.

The chip uses a 32b bidirectional data bus for external communication purposes, and several address buses for the different blocks within the programming memory. The I/O

interface follows very simple hand-shaking protocols. Table 1 summarizes the main characteristics of the prototype.

Table 1. ACE16K characteristics

Technology	STM-0.35 μm 5M-1P
Design Style	Full Custom (Analog Core) and Standard Cells (Digital I/O block)
Package	Ceramic QFP144
# of Cells	16384 (128 x 128 Array)
# of Transistors	3,748,170
# of Transistors per cell	198
Cell Size	75.7 μm x 73.3 μm
Cell Density	180 cells/mm^2
State Signal Swing	[0.6, 1.4]V (Programmable)
Weight Signal Swing	[2.15, 2.95]V (Programmable)
Time-Constant -linear. convol.-	~160ns
Time-Constant -CT Dynamics-	~0.8μs
I/O Master Clock	32 MHz
Power Supply	3.3V +/- 5%
Power Consumption	< 4 Watts
# of Analog Instructions in mem.	32
# of Digital Instructions in mem.	64 x 64 Configurations
Die Size	11885.0 μm x 12230 μm

2.2 Programming block

The programming block, illustrated in Fig. 2, provides the algorithmic capability of ACE16K. It is basically a set of 8 SRAM memory blocks with miscellaneous contents purpose, varying from digital vectors defining the algorithms to be executed -what we call "digital instructions"-, to sets of cell-to-cell interaction weights and reference levels to be applied to the cell array -what we call "analog instructions"-.

The chip has two operating modes, namely the programming and the operation mode. During the programming mode, each of the 8 SRAM blocks can be independently accessed trough the data bus in order to be written -or read, just for testability purposes-. On the other hand, in the operation mode, the contents of different groups of memory

blocks are selected through different address buses, and transmitted in parallel to the cell array.

The programming block can be divided into three sub-groups. Two of them -Operations Memory and Addresses Memory- are used to store digital instructions. Each of these blocks is designed to store 64 words of 32 bits. A digital instruction is defined as a 64b digital vector that controls the configuration of the chip circuitry. It comprises a word from the operations memory -32b- and another one from the addresses memory -32b. The third group -Weight and Analog References memory- is used to store cell-to-cell interaction weights and some references levels. This group consists of six identical SRAM blocks, each of them designed to store 32 words of 32b. Analog coefficients are defined by 8b words -each of these blocks stores 32 sets of 4 analog values. An analog instruction comprises 24 -i.e., 6 x 4- analog values that are transmitted in parallel to the processing core by means of a bank of 24 digital to analog converters.

2.3 Analog core

The analog Processing Core in ACE16K consists of an array of 128x128 locally interacting, identical processing units arranged in a rectangular grid[a].

Fig. 3 shows the block diagram of the cell in ACE16K. Arrows indicate how information flows. It contains 8 fundamental building blocks that communicate to each other by means of the so-called *ACE-BUS*. Data transferences are always carried out in the same way; some block -the data source- drives the ACE-BUS while another one -the data destination-, at the same time acquires this information from the ACE-BUS. Since the processing is done in the analog domain, this bus is, in practice, a single wire. In addition to the basic analog processing kernel -which will be described later-, the cell contains the following functional blocks: 1) An Analog Random Access Memory -LAM- with capacity for 8 gray-scale pixel values with a resolution of 8b. 2) A Local Logic Unit, consisting of a programmable two-input one-output logic operator. 3) A multimode optical sensor [5]. 4) An Address Event Downloading module, which allows the chip to download, sequentially,

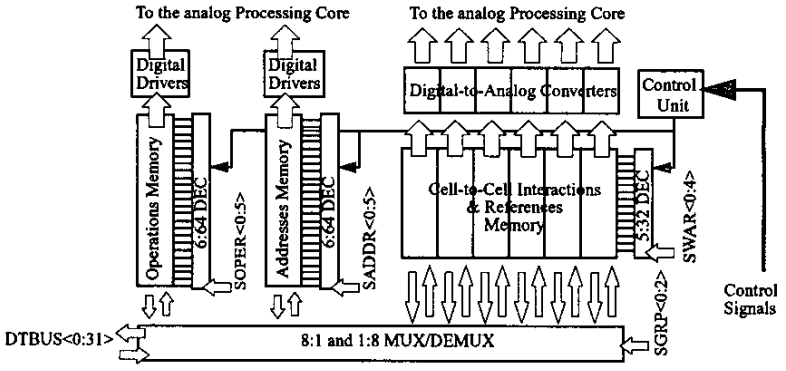

Figure 2. Diagram of the programming block

a. In addition, a ring of surrounding blocks is used to establish the proper spatial boundary conditions and to buffer the analog and digital instructions to the inner array

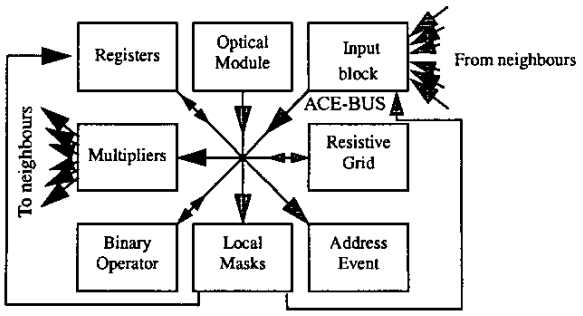

Figure 3. Block Diagram of the PE in ACE16K.

the location of active pixels. And 4) a resistive grid module that allows for continuous-time diffusion in a resistive-grid like manner.

2.3.1 Image Processing Kernel.

A bank of programmable analog multipliers is used to implement the neighborhood operations required in low-level image processing. It connects the cell with its 8 nearest neighbors and with the cell itself. Multipliers are designed using a one transistor technique [10], which, in addition to the intended product term, also generates a signal independent current -offset- that must be cancelled afterwards. Both, pixel and scaling coefficient variables, are codified in voltage form, while multiplier' output is provided as a current. Multipliers, in Fig. 4a) , are driven by three different pixel values, P_A , P_B and P_C in such a way that the current which flows to the processing core is expressed as,

$$I_{in} = \mathbf{A} \bullet \mathbf{P}_\mathbf{A} + b \cdot P_B + c \cdot P_C + z \tag{1}$$

where the $\mathbf{A}$ and $\mathbf{P}_\mathbf{A}$ matrices are defined as,

$$\mathbf{A} = \begin{bmatrix} a_{br} & a_{bc} & a_{bl} \\ a_{cr} & a_{cc} & a_{cl} \\ a_{tr} & a_{tc} & a_{tl} \end{bmatrix} \qquad \mathbf{P}_\mathbf{A} = \begin{bmatrix} P_{A_{tl}} & P_{A_{tc}} & P_{A_{tr}} \\ P_{A_{cl}} & P_{A_{cc}} & P_{A_{cr}} \\ P_{A_{bl}} & P_{A_{bc}} & P_{A_{br}} \end{bmatrix} \tag{2}$$

The currents, generated by those multipliers, are collected by the input block of the cell -in Fig. 4 (b). Due to the low output impedance of the one-transistor multipliers, a virtual ground -with the appropriate voltage value Vw_0 - must be provided -by a class II current conveyor. The non-desired offset contribution generated by the multiplier topology, is substracted from the total input current, by using a high accuracy current memory block based on a s^3I memorization scheme. Afterwards, I_{in} , can be either directly steered to the ACE-BUS or sent to the input of a current comparator, whose output can be also connected to the ACE-BUS. When the cell is operated to produce a grey-scale result, the input current is allowed to flow into any -user selectable- of the capacitors associated to the pixels. Depending on this selection, different processing kernels are obtained. Thus, for instance, to run a Sobel operator, we would define the operator in the $\mathbf{A}$ matrix, the image to be processed would be loaded to the P_A pixel, and we would use $c = z = 0$, and $b = -1$, to obtain,

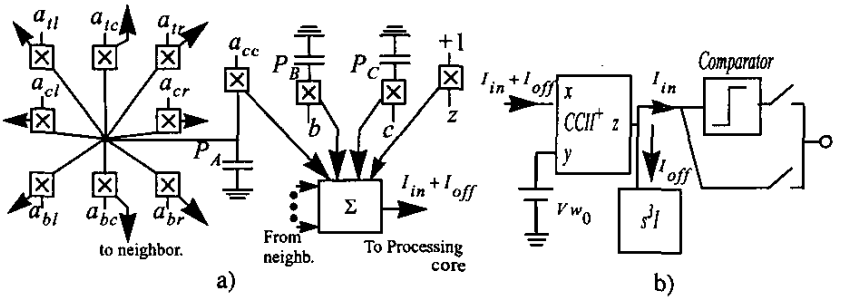

Figure 4. Distribution of Multipliers. a) Bank of Multipliers. b) Current Processing Block

$$C_B \frac{dP_B}{dt} = -P_B + \mathbf{A} \bullet \mathbf{P_A} \tag{3}$$

whose steady state solution is $P_B = \mathbf{A} \bullet \mathbf{P_A}$

If the capacitor which is allowed to be updated is C_A, then cells become dynamically coupled, and we get CNN-like behavior. In addition, by allowing the current to flow into C_A, and by defining $a_{cc} = -1$ and $a_{ij} = 0$, the steady state solution is,

$$P_A = b \cdot P_B + c \cdot P_C + z \tag{4}$$

thus providing grey-scale arithmetic operations.

2.4 I/O interface

As compared to previous analog focal plane processor implementations -[6], [7], [8], [9]-, and leaving aside the increase in the number of cells, the main improvement of ACE16K is the incorporation of a completely digital interface -not only for system control, but for digitized gray-scale images I/O as well -see Fig. 5-.

The chip incorporates 128 -one per column- DA and AD converters. DAs, used for image input, are based on a resistor string and an analog multiplexer while ADs, for image output, follow a successive approximation approach. These converter architectures pro-

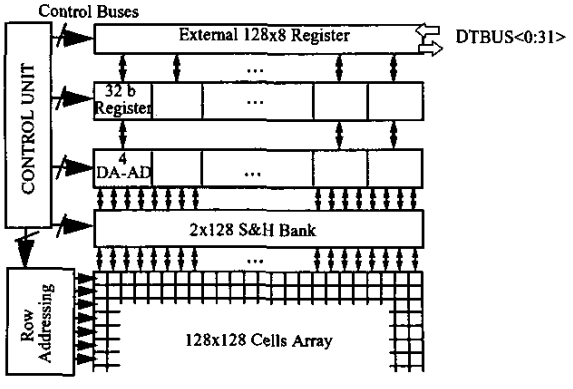

Figure 5. I/O block diagram

vide a very good compromise in terms of area and power dissipation in this particular system. On one hand, the same DACs used for image input can be used as part of the successive approximation ADCs -comparison levels are shifted up 1/2LSB. On the other hand, because the 128 converters work in parallel, a significant part of the digital circuitry needed to control the successive approximation circuitry can be shared in a common peripheral block, resulting in a substantial reduction in area and power dissipation. Finally, A self calibration process is automatically executed at the beginning of every data conversion for I/O-related fixed-pattern noise elimination.
Transferring a row to/from the chip requires $1\,\mu s$. Since the chip uses a two-stages pipelined architecture, the total time for image loading/uploading is $130\mu s$. In order to avoid undesirable digital coupling with the analog processing circuitry, image I/O and processing are normally done sequentially at different times. In most practical cases, an allocation of $140\mu s$ for image processing is more than enough -around 11 basic image processing tasks can be executed within this time-. With this assumption, the time required to load, process, and download a 128x128 image is about $400\mu s$ while VGA frames would be processed at 100 Frames/second

3 Conclusions

A new Focal Plane Analog Programmable Array Processor has been presented. The chip core consists of an array of 128x128 identical, locally interacting analog processing, sensing and storing units. On-chip program memory allows the execution of complex, sequential and/or bifurcation flow image processing algorithms. The systems is specially suited for real-time, concurrent image sensing and processing applications, with maintained complex processing rates in the range of 100 VGA-Frames per second, with a power dissipation below 4W. Its fully digital interface allows an easy interconnection with conventional digital systems

References

1. B. Roska and F. Werblin, "Vertical Interactions across ten parallel, stacked representations in the mammalian retina", *Nature*, No. 410, pp. 583-587, March 2001.
2. C. Koch, H. Li (Eds.), *Vision Chips, Implementing Vision Algorithms with Analog VLSI Circuits*, IEEE Press, 1995.
3. A. Moini, *Vision Chips*. Kluwer Academic Publishers, 2000.
4. T. Roska and A. Rodríguez-Vázquez (Editors), *Towards the Visual Microprocessor.* John Wiley & Sons Ltd., 2000.
5. G. Liñán, A. Rodríguez-Vázquez, S. Espejo, R. Domínguez-Castro and E. Roca, "A Multimode Gray-Scale CMOS Optical Sensor for Visual Computers", *Submitted to this Conference.*
6. G. Liñán, P. Foldesy, S. Espejo, R. Domínguez-Castro and A. Rodríguez-Vázquez. "A $0.5\mu m$ CMOS 10^6 Transistors Analog Programmable Array Processor for Real-Time

Image Processing", *Proc. of the 25th European Solid-State Circuits Conference,* pp. 358-36, Duisburg-Germany, Sept. 1999.

7. R. Domínguez-Castro, S. Espejo, A. Rodríguez-Vázquez, R. Carmona, P. Foldesy, A. Zarándy, P. Szolgay, T. Sziranyi and T. Roska, "A 0.8 μm CMOS Programmable Mixed-Signal Focal-Plane Array Processor with On-Chip Binary Imaging and Instructions Storage", *IEEE Journal of Solid State Circuits*, Vol. 32, No. 7, pp. 1013-1026, July 1997.
8. A. Paasio, A. Dawidziuk, K. Halonen and V. Porra, "Minimum Size 0.5μm CMOS Programmable 48 x 48 CNN Test Chip", *Proc. of the 1997 European Conference on Circuit Theory and Design*, pp. 154-156, Budapest, Hungary, September 1997.
9. P. Kinget and M. Steyaert. "Analog VLSI Integration of Massive Parallel Processing Systems", Ed.Kluwer Academic Publishers, 1996.
10. G. Liñán, *Design of Programmable Vision Chips with Low Power Consumption Levels,* Ph. D. Thesis, University of Seville, to be published in 2002.