A Versatile Sensor Interface for Programmable Vision Systems-on-Chip

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ABSTRACT

This paper describes an optical sensor interface designed for a programmable mixed-signal vision chip. This chip has been designed and manufactured in a standard 0.35µm n-well CMOS technology with one poly layer and five metal layers. It contains a digital shell for control and data interchange, and a central array of 128 x 128 identical cells, each cell corresponding to a pixel. Die size is 11.885 x 12.230mm^2 and cell size is 75.7µm x 73.3µm. Each cell contains 198 transistors dedicated to functions like processing, storage, and sensing. The system is oriented to real-time, single-chip image acquisition and processing. Since each pixel performs the basic functions of sensing, processing and storage, data transferences are fully parallel (image-wide). The programmability of the processing functions enables the realization of complex image processing functions based on the sequential application of simpler operations. This paper provides a general overview of the system architecture and functionality, with special emphasis on the optical interface.

1. INTRODUCTION

Already in 1997, forecasts regarding the next wave of InfoTech Innovation [1] anticipated that high-performance sensors would shape the first decade of the 3rd millenium. Thus, while in the 1980s innovations were focused on creating processor-based computer "intelligences", and in the 1990s on networking those intelligences together with laser-enabled bandwidth, innovations during this decade will most likely be focused on adding *sensing* and *actuating* "organs" to these devices and networks.

In this area we have a lot to learn from nature. The close integration, of interacting sensing, processing and acting substructures featured by natural beings provides an endless source of inspiration for these new generations of sensorial intelligences [2]. Exploiting this source of inspiration may lead to revolutionary changes in the conception and implementation of these systems.

Thus, the extensive usage of digital processing in today's conventional architectures [2] is foreseen to be complemented in the future with an increased usage of *parallel analog* processors capable of operating concurrently and in close interaction with the sensory circuits. The final target is to realize complete sensory/processing (and actuating) systems in a single chip through the smart synergy of sensors, analog processing and digital processing structures.

In this sense, during the last few years significant advances have been made regarding the implementation of *Vision Chips*; i.e. chips which are capable of acquiring images and processing them using circuits embedded in the same silicon substrate in which the image is captured – called *focal-plane processing*.

The design of these chips can be undertaken following two alternative approaches:

- Pick up a specific task and its model and implement it on silicon. This is the usual way, leading to very useful, task-specific smart sensors [3] [4].
- Make *general-purpose* mixed-signal image processing devices [5]. That is, devices which, through *programming*, can be employed to realize a myriad of image processing tasks, similar to the possibility featured by the ubiquitous von Neumann digital processor.

The chip reported covered in this paper, called ACE16k, belongs to this second group. It has a Single-Instruction-Multiple-Data architecture (SIMD) and includes some of the most relevant features of the Cellular Nonlinear/Neural Network Universal Machine (CNNUM) paradigm [6]. Other chips, also belonging to this group, have been reported in

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2. These conventional architectures employ analog blocks only at the front-end sections, while all processing is realized in the digital domain. The overall sequence of operations is: Sensing – A/D Conversion – Digital-Processing – D/A Conversion)

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the last years [7]–[17], etc. Some of them do not have sensory capabilities, they are just conceived as programmable *co-processors*; others are only designed for *black-and-white* image processing; and others are designed for very large density, but feature very small analog *accuracy* in the internal processing.
This paper presents the new multi-mode optical sensor which is used at the sensory part of the chip ACE16k. The presented pixel has the capability of acquiring visual information in very different illumination conditions since it provides both, linear integration and logarithmic compression sensing schemes.

2. ACE16k ARCHITECTURE

ACE16k follows the SIMD-CNNUM paradigm. As shown in Fig. 1, Single Instruction Multiple Data systems consist of an array of identical Processing Elements (PE) which execute the same instructions at the same time. Instructions are executed on data which are *locally* defined, at the PE level, while the instruction sequence is issued by a control unit shared by all the PEs in the array. Most commonly, the communication network among PEs is restricted to the *nearest neighbors*.
In the case of *low-level* [1] image processing, where the same operation sequence is applied to all the processors in the array, the most straightforward mapping between images and chips consists of using one processing element per pixel, thus providing a very compact, and efficient way of defining algorithms.
ACE16K implements most of the relevant functional features of the CNNUM [6] paradigm, namely:

- non-linear dynamic coupling among the elementary processing units, also called *cells*,
- local, distributed memories for storage of intermediate images,
- local, distributed logical processing,
- incorporation of *global*, chip-level structures for storage of *instructions* and control of algorithmic processing flows.

Thus, ACE16k is capable of operating as a flexible, user-programmable algorithmic processor; a kind of *visual microprocessor* [5]. At the hardware level, the instruction set of such a microprocessor includes setting the values for the strenghts of the cell interconnections, called interconnection *templates* which define the actual *low-level* image processing task to be executed; also implies reconfiguring the interconnection topology of the structures incorporated at cell level, thus controlling data flows and basic circuit configuration; and arranging local analog and digital operations between locally-stored images, which allows for the execution of both pixel-wise binary inversion in black and white images, for instance, and image-wise operations - gray-scale combinations of two images by linear arithmetic operations.
The architecture of the system is depicted in Fig. 2(a). Here, various functional substructures are identified:

- A sensory/processing core, which consists of an array of identical 128×128 PEs. These PEs have embedded circuit structures for optical sensing, programmable analog processing (designed for around 7bit accuracy), programmable binary processing, local memory and signal flow reconfiguration.

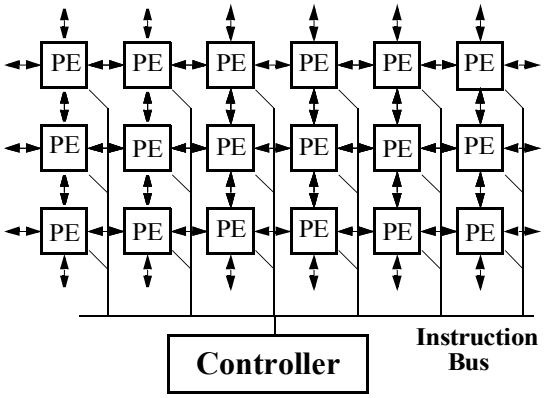


Fig. 1. Typical SIMD Architecture

1. This refers to the processing realized at the early stages of the flow, where the amount of data to process has very large dimensionality, $N \times M$, where N is the number of rows in the array of pixels, and M is the corresponding number of columns. This low-level processing stage is critical for reducing the dimensionality of the data for subsequent processing stages.

- A ring of *border* cells used to establish spatial boundary conditions for image processing, and several buffers driving analog and digital signals to the array.
- A programming block, which contains several SRAM digital memories used to store the algorithms to be executed by the chip.
- A block for I/O image flow control and format conversion[1]. 128 Digital to Analog (DAC) and Analog to Digital (ADC) converters, one per column, which constitute a digital I/O port for images.
- Digital blocks for automatic addressing of rows and columns during image I/O processes.

The chip uses a 32-bit bidirectional data bus for image communication purposes, and several address buses for the different blocks within the programming memory. The I/O interface follows very simple hand-shaking protocols. Table 1 summarizes the main characteristics of the prototype.

ACE16k is conceived to be used in two alternative ways. First, whenever the images to be processed are directly acquired by the optical input module of the chip [5]; and second, as a conventional image co-processor working in parallel with a digital hosting system which provides and receives the images in electrical form.

3. PHYSICAL FOUNDATIONS FOR LIGHT SENSING IN CMOS

Photo-devices are the elements which allow for the combination of sensory and processing planes in a single chip. Several possibilities for the architecture of the photosensor exist, however, all of them rely on the same physical phenomenon, the photoelectric effect. Covalent bonds holding the electrons at their atomic sites in the lattice can be broken by an incident radiation if the energy of the incident photon is greater than the silicon band gap. Since this energy level is about 1.124eV, those photons with wavelengths below $1.1\mu\text{m}$ could be, theoretically, powerful enough to excite carriers from the valence band into the conduction one, thus producing the photo-generation.

Unfortunately, not all the photogenerated carriers are detected. Recombination phenomena make the number of created pairs to decrease very fast. Typical carrier life times in standard CMOS technologies are in the order of $0.1\mu\text{s}$ to $10\mu\text{s}$ and, therefore, efficient mechanisms to collect them before they recombine must be provided. The simplest method to do this consists of using reverse biased diodes. If photo-generation occurs within the depleted quasi-neutral region of the p-n junction, the built-in junction potential will quickly separate electrons and holes. These carriers form a current whose value can be quantified by the following expression [18],

$$I_{ph} = \frac{\eta \cdot q \cdot P_i}{h \cdot \upsilon} \tag{1}$$

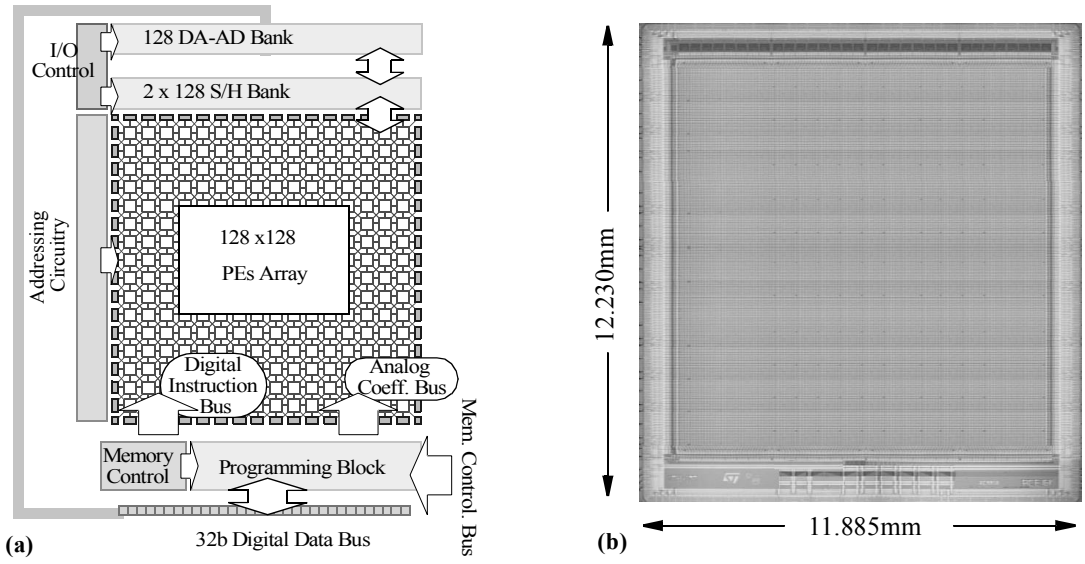


Figure 2. Architecture and microphotograph of ACE16k.

1. From digital to analog and vice versa.

where, η is the quantum efficiency, q is the electron charge, P_i is the density of power of the incident light, and $h \cdot \upsilon$ is the energy of one photon with frequency υ.
The quantum efficiency figure, η, expresses the quotient between the number of generated pairs and the number of incident photons with a certain frequency υ.

$$\eta(\upsilon) = \frac{\text{no. of detected charges}}{\text{no of incident photons}} \tag{2}$$

which is always lower than unity in the visible and infrared portion of the spectrum.
The number of charges photogenerated by an incident light with a power P_0 and a wavelength λ detected during a given time interval ΔT_{int} by using a photosensor of area A and a quantum efficiency $\eta(\lambda)$ is given by [20],

$$\Delta n = A \cdot P_0 \cdot H \cdot \xi(\lambda) \cdot \Delta T_{int} \tag{3}$$

where H is a physical constant defined as $H = (h \cdot c)^{-1}$ and $\xi(\lambda) \equiv \lambda \cdot \eta(\lambda)$ is a function of the wavelength of the incident light.
The total amount of electrical charge detected is simply obtained as,

$$Q_{ph} = q \cdot \Delta n = [A \cdot \xi(\lambda) \cdot \Delta T_{int}] \cdot P_0 \cdot q \cdot H \tag{4}$$

while the equivalent current produced within this interval is,

$$I_{ph} = Q_{ph} \times (\Delta T_{int})^{-1} = [A \cdot \xi(\lambda)] \cdot P_0 \cdot q \cdot H \tag{5}$$

Most usually, the photogenerated current is converted into an equivalent voltage value by using one of the following methods; the integration of the photogenerated current onto a previously initialized capacitor, or the transformation of the

Technology	ST Microelectronics 0.35 µm 5M-1P
Design Style	Full Custom (Analog Core) and Standard Cells (Digital I/O block)
Package	Ceramic QFP144
# of Cells	16384 (128 x 128 Array)
# of Transistors	3,748,170
# of Transistors per cell	198
Cell Size	75.7 µm x 73.3 µm
Cell Density	180 cells/mm^2
Pixel Signal Swing	[0.6, 1.4]V (Programmable)
Weight Signal Swing	[2.15, 2.95]V (Programmable)
Accuracy of Analog Processing Blocks	~1%
Time-Constant -linear. convol.-	~160ns
Time-Constant -CT Dynamics-	~0.8µs
I/O Master Clock	32 MHz
Power Supply	3.3V +/- 10%
Power / Speed / Area Figures	0.33x10^{12}OPS, 0.18 x10^{12}OP/J and 3.8x10^9 OPS/mm^2
# of Analog Instructions in mem.	32
# of Digital Instructions in mem.	64 x 64 Configurations
Die Size	11885.0 µm x 12230 µm

Table 1. ACE16k Characteristics

current into a voltage by driving some kind of resistive load. In any case, attempts to linearly cover the huge range of illuminations existing in real life scenes[1] – 6 to 8 decades – will always fail due to the fundamental limits imposed by noise floor and power supply level.
An interesting possibility to expand the sensor dynamic range – by renouncing to linearity – consists of using a non-linear I-V conversion block with a compressive-like characteristic.
Among all the possible non-linear transfer functions, a very suitable one for visual signal compression is the logarithmic function. Its suitability comes from the evidence [21] that photo-receptors in the human retina exhibit a logarithmic-type response to light stimulus which provides a wide dynamic range of operation.
We will see in the next sections how to exploit the photo-sensitive devices existing in standard CMOS technologies to obtain a multi-mode photosensor.

4. THE MULTIMODE OPTICAL SENSOR

4.1. Sensor Schematic

Fig. 3 shows the architecture of proposed sensor which can be divided into three blocks. The first one, a tri-state readout buffer, is used to control the communications among the sensor and others blocks in the CNNUM cell – basically the LAM module. Sensor readouts are controlled by the global programming signal **ROPT** – which corresponds to one bit in a Switch Configuration Register SCR.
The second part of the sensor is the circuitry devoted to the transduction of the photo-generated charges into either a current or a voltage level. The user has the possibility of selecting the photo-transduction mechanism by means of configuration signals **LOG1**, **LOG2**, **PCH** , which are also stored in the SCR, as will be explained later.
The third block includes the optical sensor itself and two configuration switches $M_{s1,2}$ used to select one out of the three available photosensors. The selection of the sensor is carried out by other SCR programming signals called **DW** and **WS**.

4.2. Integration Modes

In integration modes, the sensor provides an output voltage which linearly depends on the intensity of the incident light. Independently of the actual photosensor selected, the sensing procedure is always the same. First of all, $M_{s5,4}$ are turned off by making **LOG1**=**LOG2**=1. Afterwards, switch M_{s3} precharges the internal node *a* to the user-definable voltage *VPCH*. Finally, switch M_{s3} is turned off and the photogenerated current I_{ph} charges or discharges the pixel capacitor C_{pix}.
Fig. 4 shows the three different configurations for linear integration.
Fig. 4(a) shows the equivalent schematic for the first integration mode. It uses the N-Well/P-Subs photodiode (D_{WS}) as light sensitive device. The P-Diff/N-Well diode is annulled by making signal **WS**=0, while the bipolar transistor is also off by the same signal since it forces $V_{BE} = 0$. Then, it is easy to obtain that,

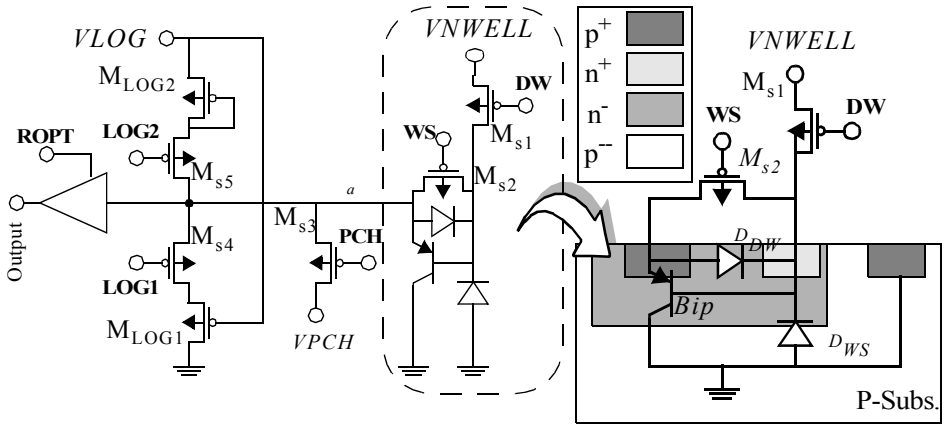


Fig. 3. Representation of the Multimode Pixel. Schematic.

1. In humans, ~200dB separate the glare limit from the scotopic threshold.

$$V_a = VPCH - \frac{I_{Ph}}{C_{pix}} T_{int} = VPCH - \frac{T_{int}}{C_{pix}} \times [A_{WS} \cdot \xi_{WS}(\lambda)] \cdot P_0 \cdot q \cdot H \quad (6)$$

where A_{WS} is the sensing area of the N-Well/P-Subs photodiode, P_0 is the power of the incident light per area unit, and $\xi(\lambda) \equiv \lambda \cdot \eta_{WS}(\lambda)$.

Fig.4(b) shows the sensor schematic when the P-Diff/N-Well photodiode is used. By setting **WS**=1, **DW**=0 and $VNWELL$ to the supply level, we ensure that the N-Well/P-Diff diode remains reverse biased, and that the vertical bipolar transistor is OFF. Only the carriers collected by the P-Diff/N-Well junction will contribute to the photocurrent yielding,

$$V_a = VPCH + \frac{I_{Ph}}{C_{pix}} T_{int} = VPCH + \frac{T_{int}}{C_{pix}} \times [A_{DW} \cdot \xi_{DW}(\lambda)] \cdot P_0 \cdot q \cdot H \quad (7)$$

Finally, Fig. 4(c) shows the schematic of the sensor when **WS**=**DW**=1. In this case, the base of the vertical BJT remains in open circuit. Photogenerated minority carriers in the base-emitter junction produce an emitter-base current which is amplified by the transistor effect. In this case, the output is simply given by

$$V_a = VPCH - \beta \frac{T_{int}}{C_{pix}} [A_{DW} \cdot \xi_{DW}(\lambda)] \cdot P_0 \cdot q \cdot H \quad (8)$$

The use of linear sensing schemes is limited to images where the existing dynamic range is relatively narrow. The next section shows how the proposed multi-mode sensor can be configured to perform different log-compression sensing schemes.

4.3. Logarithmic Compression with Transistor-based Loads

Logarithmic-type sensing has the advantage of producing images in which the difference between pixels only depends on the difference in optic contrast and not on global illumination conditions. Then, sensors exhibit a wider dynamic range DR. However, the price to be paid for that DR increase is a reduction of the contrast in the image – mostly due to the log function.

To better understand the advantages of log compression vision it is necessary to identify the very basic nature of the information that is processed by vision systems. Except in some very special cases, this information is a contrast level. In those situations where transmission effects on the medium can be neglected, the light intensities over the object are the product of the irradiance E and the reflectance ρ of its surface at this point.

The response $O_{Lin}(x, y)$ of a linear sensor focusing to object point (x, y) is always proportional to the irradiance at this point $E(x, y)$ and the reflectance of the surface at this point $\rho(x, y)$, thus,

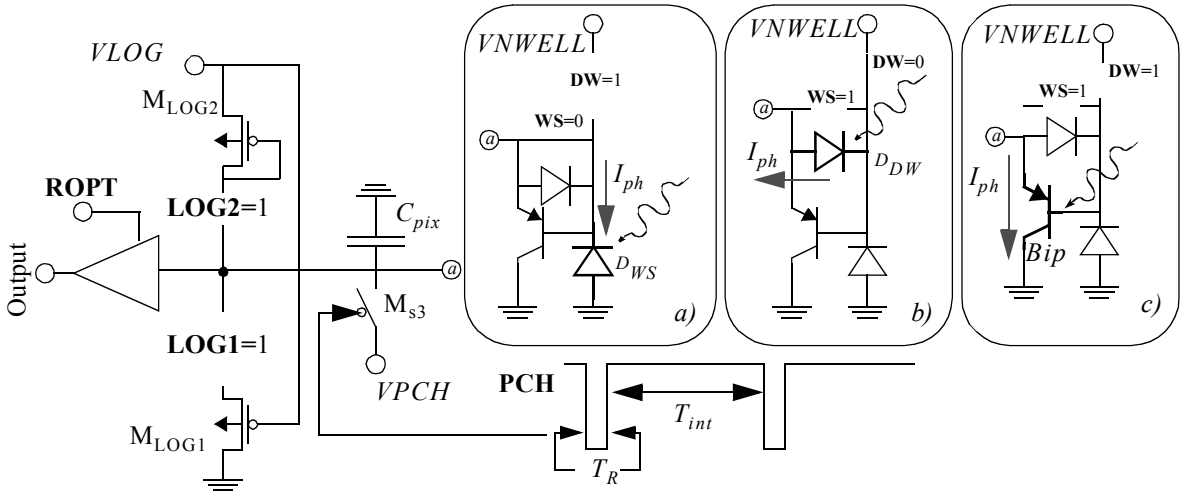


Fig. 4. Available Configurations for Integration Modes.

$$O_{Lin}(x,y) = E(x,y) \cdot \rho(x,y) \tag{9}$$

whereas that of a logarithmic sensor is

$$O_{Log}(x,y) = Log[\rho(x,y) \cdot E(x,y)] \tag{10}$$

Hence, two different regions of a surface with different reflectances $\rho(x_1, y_1)$ and $\rho(x_2, y_2)$, but the same irradiance E would produce a differential output signal given by,

$$\Delta O_{Lin} = E \cdot \Delta\rho \tag{11}$$

in the linear case while for the logarithmic sensor it would be,

$$\Delta O_{Lin} = Log(\rho_1) - Log(\rho_2) \tag{12}$$

As it can be seen, in this latter case, the differential output signal does not depend on the irradiance but on the difference between the reflectances. Obviously, this is not true for the linear sensor, where the differential output signal also depends on the common irradiance level. Hence, the same details – points with the same level of ρ – in an input image might not be distinguishable in linear sensors because of the irradiance level which could even make the sensor to be over-exposed -saturated.

Fig. 5 illustrates the output images provided by linear and logarithmic sensing schemes when capturing a wide dynamic range day-light scene. It is seen how, at the expense of a loss of contrast, the log-type acquired image gives information about areas which couldn't be identified in the linearly acquired one.

Most log-type reported CMOS image sensors exploit the logarithmic relationship existing between the current and the gate to source voltage when MOS transistors operate in the subthreshold regime. This property is used in our sensor as follows.

Fig.6 shows the configurations available for this type of log-sensing in the proposed circuit. Notice that the reset transistor M_{s3} has been removed from the schematic since log-mode acquisitions work in continuous time – the output voltage corresponds to the equilibrium point of driving the non-linear resistive load with the photogenerated current. On the other hand, the selection of the active load must be properly done according to the sensor choice. Assuming that the drain to source current for a saturated PMOS transistor – bulk terminal connected to V_{dd} – within its subthreshold region is approximately given by[1] [22],

(a) **(b)**

Fig. 5. Example of Log-Type Visual Acquisition. a) Normal Linearly Acquired Image. b) Log-Type

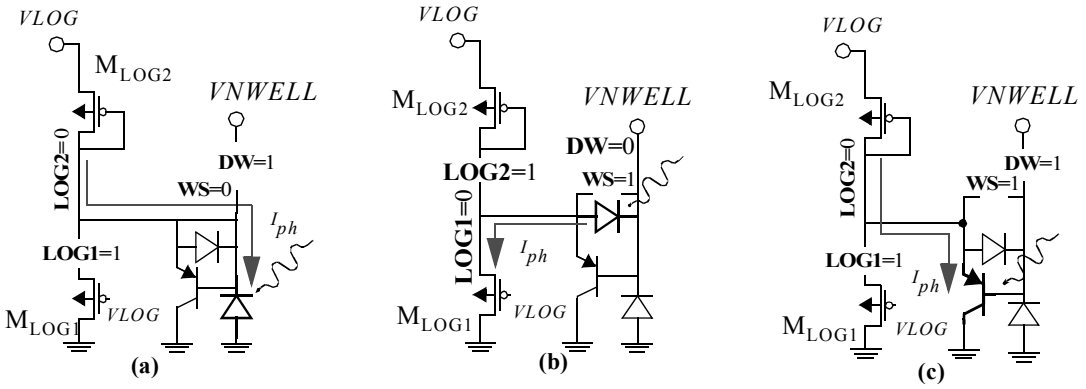
1. The definition of the parameters in this expression can be found in [22].

$$I_{DS} = I_{D0} \cdot e^{\left(\frac{n_p V_S - V_G - V_{T0} - (n_p - 1)V_{dd}}{n_p U_T}\right)} \tag{13}$$

it can be found that the steady state output voltages are given by the set of expressions displayed in Fig.6.
In addition to the loss of contrast produced by the logarithmic function, it is also observed that the expressions for the output voltage contain several technological parameters related to the load transistor. Unfortunately, mismatching phenomena make those parameters to vary from pixel to pixel and, consequently, the Fixed Pattern Noise (FPN) figures in these kind of sensors are worst than those of their linear counterparts.
An interesting alternative which partially solves this problem consists of using correlated-double sampling techniques [23] at the pixel level by exploiting the reconfiguration and algorithmic capabilities of the CNNUM cell. However, it may require adding new modules to the cell and the execution of a certain number of additional operations, thus slowing-down the processing.
In the next section we will present a log sensor which does not use any transistor load and that, consequently, exhibits better FPN figures.

4.4. Logarithmic Compression in the Photo-voltaic Mode

The idea of using the photodiodes in the photo-voltaic mode is relatively recent. Up to our knowledge, it was first introduced and tested by Dr. Ni *et al.* in 1994 [24]. Experimental results demonstrated that this kind of sensors exhibit a very wide dynamic range and good uniformity FPN performances.
The basic concept introduced by this sensing scheme consists of using a photodiode in an open circuit configuration, and to let it to reach its steady state.
In our case it works as follows.
Suppose the circuit in Fig.6(b). If no resistive load is connected to node *a* and the circuit is allowed to achieve its steady state, the charge conservation principle imposes that the current flowing from *VNWELL* to node *a*, that is $I_S + I_{ph}$ [1], must be equal to that flowing through the diode. Assuming a typical exponential expression for the diode current yields,



$$V_a = \begin{cases} n_{p_2} VLOG - V_{T0_{M2}} - \left(n_{p_{M2}} - 1\right) V_{dd} - n_{p_{M2}} U_T Ln\left[\dfrac{A_{WS} \cdot \xi_{WS}(\lambda) \cdot P_0 \cdot q \cdot H}{I_{D0_{M2}}}\right] & \text{Fig. 3(a)} \\ \dfrac{VLOG + V_{T0_{M1}} + \left(n_{p_{M1}} - 1\right) V_{dd} + n_{p_{M1}} U_T Ln\left[\dfrac{A_{DW} \cdot \xi_{DW}(\lambda) \cdot P_0 \cdot q \cdot H}{I_{D0_{M1}}}\right]}{n_{p_{M1}}} & \text{Fig. 3(b)} \\ n_{p_{M2}} VLOG - V_{T0_{M2}} - \left(n_{p_{M2}} - 1\right) V_{dd} - n_{p_{M2}} U_T Ln\left[\beta \dfrac{A_{DW} \cdot \xi_{DW}(\lambda) \cdot P_0 \cdot q \cdot H}{I_{D0_{M2}}}\right] & \text{Fig. 3(c)} \end{cases}$$

Fig. 6. Available Configurations for Standard Log.Compression Modes.

$$V_a = VNWELL + nU_T Ln\left(\frac{I_{ph} + I_S}{I_S}\right) \quad (14)$$

which shows a log-type relationship between the pixel output voltage and the light intensity.
The main advantage of this log-compression scheme is that the obtained expression is simpler, it involves only a few terms, than those on Fig.6, and consequently, its operation is intrinsically more robust against cell-to-cell discrepancies.

4.5. Layout

The multi-mode sensor described in this paper has been included into the cell used by the ACE16K [25] prototype.
Fig.7(a) shows the layout of the sensor in the ACE16K chip. The N-Well in which the sensor is laid-out is $9.8\mu m \times 9.8\mu m$. A silicided protection area has been defined all around the sensing area in order to avoid a loss of sensitivity of the sensor. In addition, all the reconfiguration switches are PMOS type and laid-out in a different NWELL for isolation purposes. Finally, as can be seen in Fig. 7(b), all metal layers contain a hole just in the area under which the sensor is placed in order to allow the light to directly reach the sensing area.

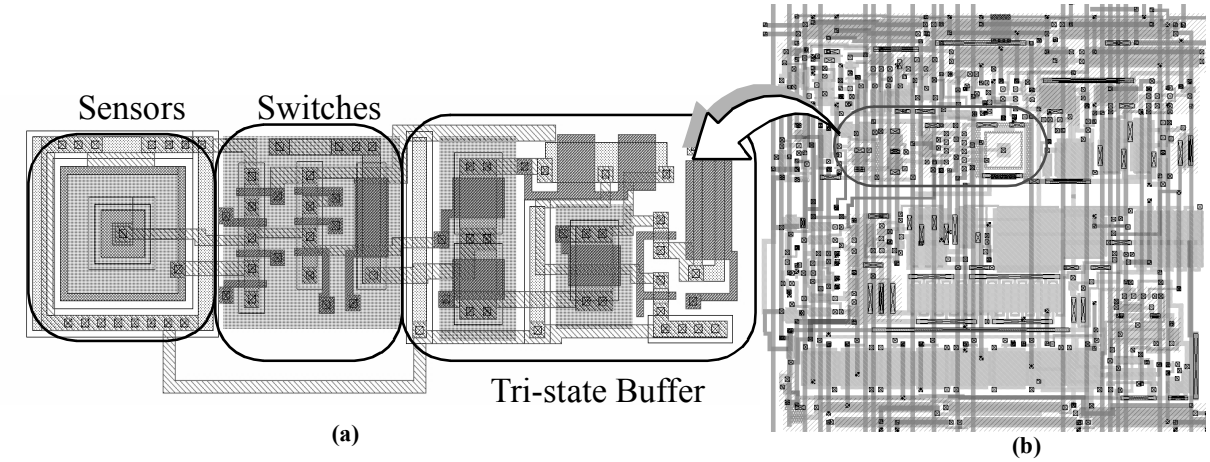


Fig. 7. Layout Views. a) The sensor. b) The Cell in ACE16K.

5. CONCLUSIONS

A new multimode optical sensor architecture for the optical interface of Focal Plane Array Processors chips have been presented. The sensor offers the possibility of selecting the actual light-sensitive device as well as the mechanism for transducing the photogenerated charges. Both linear and log compression acquisition modes are available, making the sensor very suitable to fit into very different illumination conditions.

6. ACKNOWLEDGMENTS

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