CMOS mixed-signal MODEM for data transmission and control of electrical household appliances using the low-voltage power-line

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ABSTRACT

This paper presents a CMOS $0.6\mu m$ mixed-signal MODEM ASIC for data transmission using the low-voltage power line. This circuit includes all the analog blocks needed for input interfacing and modulation/demodulation (PLL-based frequency synthesis, slave filter banks with PLL master VCO for tuning, and decision circuitry) plus the logic circuitry needed for control purposes. The circuit operates correctly within the industrial temperature range, from -45 to $80°C$, under 5% variations of the 3.3V supply voltage.

Keywords: mixed-signal design, communication networks,

1.INTRODUCTION[1]

It is well known that the use of communication circuitry to control and monitorization of multiple home devices provides large benefits to users, not only because it enables a regulation on their cost but also because it allows their control outside home[1], [2], [3]. However, to be of practical interest, the communication systems have to fulfill a set of basic requirementes, that is, they should be able to deal with multiple data transmission channels with sufficient speed to allow a permanent link between the control centers that provide the access to those devices, the user and the devices themselves. Of course, this should be achieved with low cost to guarantee the acceptance of the product.

Unfortunatelly, current systems, based on communication networks, have to deal with very high installation costs due to the need of a parallel network to enable the communication. However, this limitation can be surpassed by using the existing low-voltage power-line to allow the data transmission. Of course, this alternative is not free from some concerns [4]:

- High reliability requires a supervision logic to control the data transmission.
- Low cost implies a high integration of the electronic circuitry.
- Data transmission speed involves the exploration of adequate modulation techniques.

To overcome all these limitations, an ASIC composed by two different basic blocks has been designed as described below:

A part of the ASIC (*High Frequencies Module* from now on) will be used to send and receive signals by two different channels (to ensure the communication in case of transitory degradation of one of the channels). This block will enable the communication with the control center that can be as far as one kilometer beyond the modem. In the approach presented in this paper, the frequencies of these channels have been settled to 375kHz and 450kHz, due to the low level of noise experimentally found arround these values.

A second block (*Low Frequencies Module* from now on), will be used to control the communication inside the building. To cope with this, the basic requirements for this block are to enable the data transmission through small distances (between 50 and 100 meters) with a speed that has to be enough to ensure a real-time control of the devices connected to the system, but not too large, taking into account that the main objective is to provide the largest number of channels as possible, to allow the control of a high number of devices[2]. Having all this into account, a global frequency range (that will contain all the communication channels) from 90kHz to 350kHz will be used to avoid interferences with the HFM, with

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2. The larger the speed, the wider the channel required.

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a minimum speed limit of 100bits/s. Again, to increase the transmission quality, two channels will be simultaneously available; one to control the quality of the communication and a second one to enable the data transmission. Of course, it is mandatory that the ASIC functionality has to be ensured if some, or even all, the channels are active.

The type of modulation used has to be able to maximize the number of channels providing high reliability against the presence of multiple signal in the transmission line, noise, line impedance changes, etc.

2.ASIC OPERATION MODES

Taking into account the position within the communication network, the developed modem has to work with the following requirements, that are illustrated in Fig. 1.

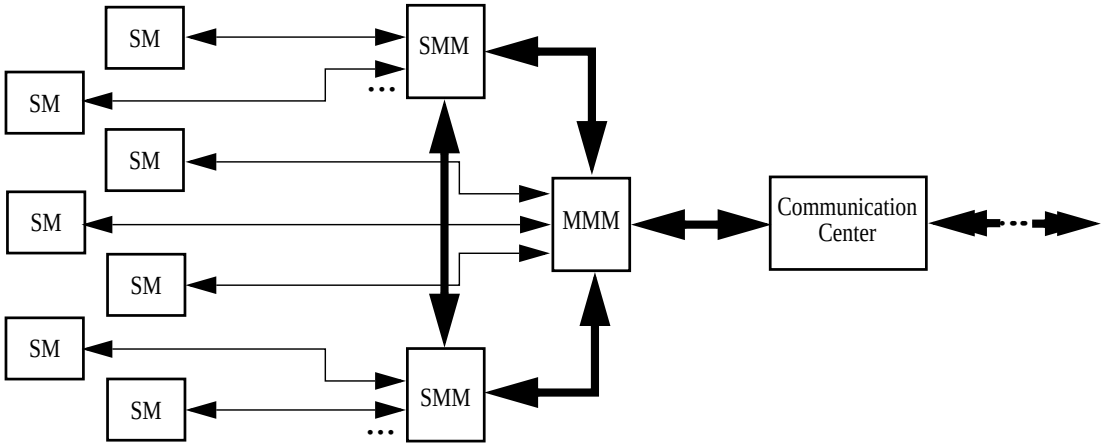

Figure 1. Example of communication hierarchy between modules

•Main Master Modules (MMM) that can communicate with the control center using the HFM and their own High Frequencies Control Module (HFCM). Also, they can communicate with other master and slave modules using the one of the LFM's for each channel. The Low Frequencies Control Module (LFCM) has to be able, at any moment, to assign any of the low frequency channels to be either communication or control channel.

•Simple Master Modules (SMM) that are not allowed to contact the HFM (thus, HFM and HFCM should be disconnected). At low frequencies, their functionality is as any MMM.

•Slave Modules (*SM*) that share information using a single channel with only one MM, assigned during the configuration of the system. Thus, HFM, HFCM and one LFM will be disconnected. They will only respond (but necessarily) upon their master requirement.

The two components of the identification code will be defined by a serial communication interface, that will be stored in an EEPROM. This information will be used during the initialization of the system.

The architecture for the ASIC is shown in Fig. 2.

As shown there, all the modules in Fig. 1, will include these blocks although only partially enabled depending on their requested functionality.

3.DESCRIPTION OF THE ANALOG CIRCUITRY

The already reported HFM, [5], has been shown to demodulate signals down to 283μ*Vrms* under nominal operating conditions, and obtain a worst case sensitivity of 316μ*Vrms* within the whole industrial temperature range, and under 5% variations of the supply voltage. Transmission/Reception (Tx/Rx) is done within temporal windows located around the zero crossing of the 50Hz/60Hz power-line voltage, using two frequency channels located at 375kHz and 450kHz, where clean frequency windows have been encountered in field evaluations. Since [5] gives a detailled information about this module, the rest of the paper will be devoted to the description of the LFM.

Fig. 3 shows a functional scheme of one Transmission-Reception Low Frequencies Module (TRLFM): when it is operating as a demodulator, the signals enter by the input amplifier and are filtered to eliminate the noise and select the de-

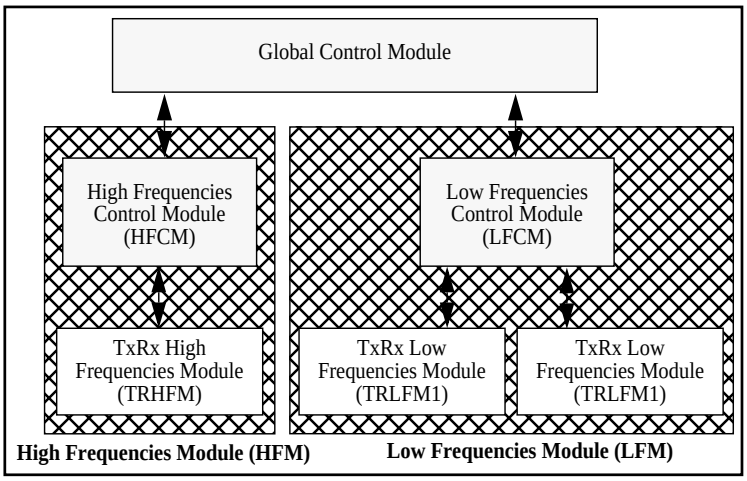

Figure 2. MODEM architecture

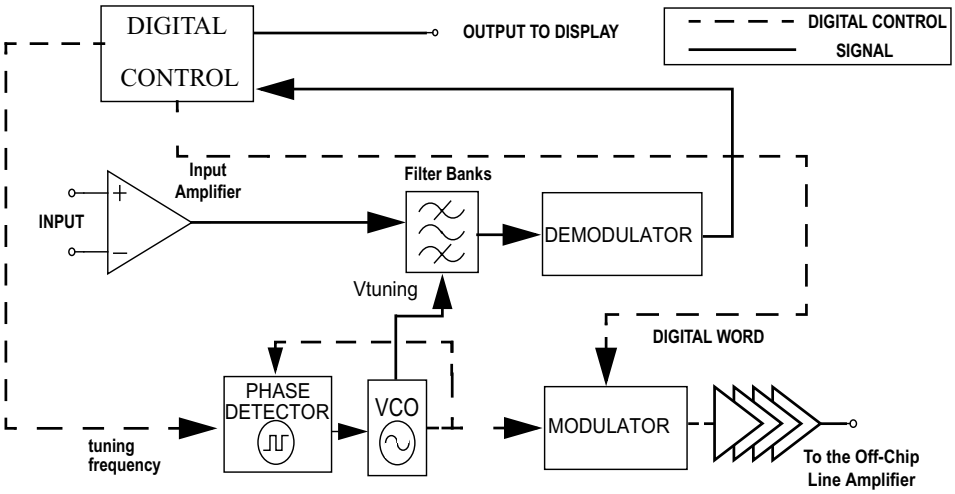

Figure 3. Conceptual TRLF Module operation: transmission/reception sections.

sirable frequency. The tuning channel is selected by a digital control and the required frequency is captured using a phase locked loop (PLL).The filtered signal is demodulated and the result is processed by the digital control, that makes it available for the customer or sends it to the Communication Centre.

In the modulation stage, the digital control is use not only to choose the channel in which the message is going to be transmitted, but also to generate it.

Fig.5 (a) shows the schematic of the bandpass filter used in the TRLFM [6]. This architecture has been chosen because of three reasons: the first one is that this circuit has a very high quality factor, ideally infinite if mismatching is not taken into account; the second one is that the tuning frequency is independent of the quality factor and, finally, this structure has the same parasitic that the voltage controlled oscillator, which has been designed with the same structure[1], so it is expected that both have the same frequency dependence behaviour.

Expression (1) shows the dependence for the tuning frequency when the analysis of the filter in Fig. 5 (a) is done taking into account the output resistance of the OTA's.

1. Where, to achieve the oscillation, the input node must be connected to the reference voltage in Fig.5 (a).

$$f_o = \sqrt{\frac{gm_1 gm_2}{C_1 C_2} + \frac{g_{02}(gm_4 - gm_3 + g_{01} + g_{03} + g_{04})}{C_1 C_2}} \quad (1)$$

In our approach, the tuning is performed in two steps: first, a frequency range containing the desired frequency value is delimited by the selection of C_1 and C_2, then, to select the correct frequency value, the transconductances gm_1 and gm_2 are varied using a tuning voltage, Vtuning, that is generated by the PLL structure shown in Fig.5 (b). If only one pair of capacitors C_1 and C_2 is used to cover all the frequency range, the value of the transconductance must increase by a factor five which is carried out augmenting the Vtuning value. This rise in Vtuning implies a variation in the transconductances linearity which is undesirable. This problem is solved using four pairs of capacitors to cover all the frequency range, the desired frequency value is delimited by the proper selection between one of the four different values of C_1 and C_2, (this commutation of capacitors is achieved by the digital control).

Fig.4 shows the linearity of the OTA transconductance (expressed in percentage) which has been calculated performing a DC sweep to get the transconductance for different tuning parameters and then calculating the relative error respect to the transconductance value in the common mode. With this result it is checked that the error in the transconductance linearity is under 5.5% for a voltage range between1.3V and 2.0V [7].

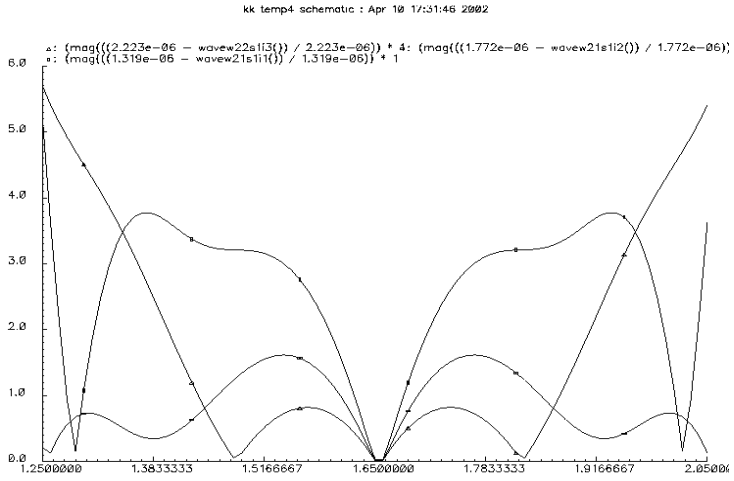

Figure 4. Gm's Linearity error (%).

Another problem is associated with the output resistance, as shown in (1), the second term depends on the transconductances output resistance, which is undesirable too because tuning degradations appears in the filters and in the voltage controlled oscillator because the output resistance depends on the frequency. Thus, to avoid this problem a regulated folded cascode architecture has been elected for the output stage which provides an high and stable, in the tuning frequency range, output resistance.

Fig.5 (d) shows the output stage. The amplifiers settle on the point of operation so the cascode transistors maintain this value and provide a high output resistance for the complete range of variation of the transconductance. Another purpose of the amplifiers is to disconnect the nodes at their outputs and the gates of the cascode transistors, so the parasitic of these nodes is reduced, resulting in an increased output resistance value.

The values of the transconductances are in the vicinity of 1.5μA/V to keep the capacitor values small enough to be integrated. Due to this fact an output resistance larger than 30MΩ is needed in the design of the OTA's. Fig5 shows that an output resistance larger than 80MOhm is achieved within the frequency range of interest, that is, between 90 kHz and 350 kHz. This is enough to ensure that the tuning frequency is correctly modelled keeping only the first term in (1).

Hence, controlling the tuning frequency is possible by varying one, several or even all these variables.

One of the more important circuit of the LFM analog part is the PLL. The objective of the PLL, shown in Fig.5 (b), is to tune the filter and the voltage control oscillator (VCO) by the Vtuning generation. This tuning is performed by comparing the reference frequency, obtained digitally by dividing the master clock frequency, with the frequency generated by

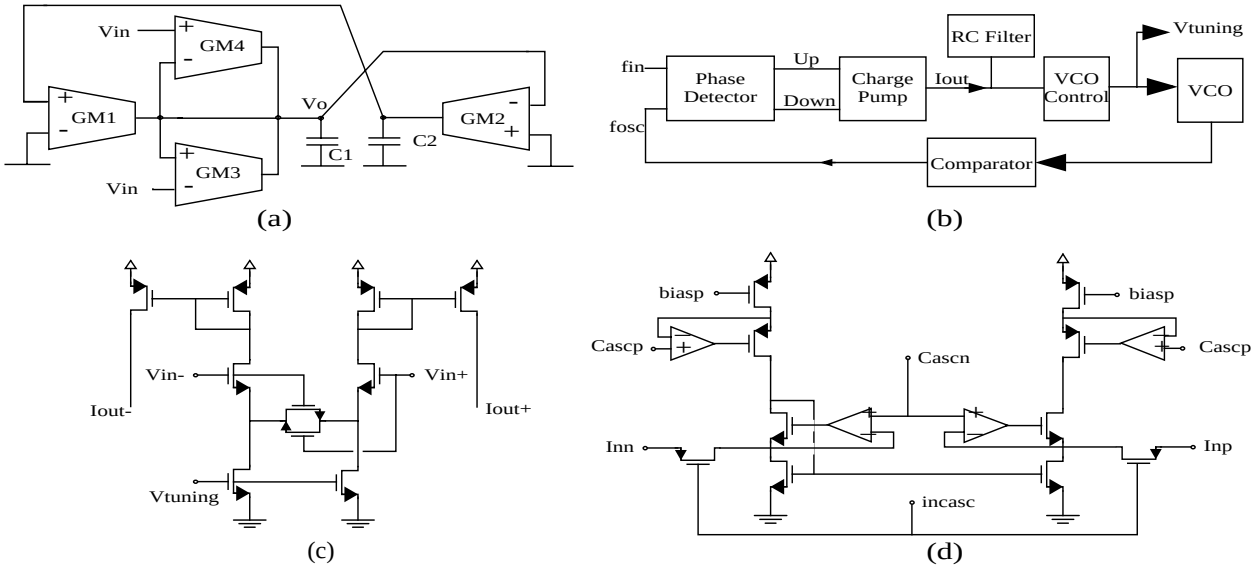

Figure 5. (a) Passband Filter Stage, (b) PLL configuration, (c) Core of Filter OTA's; (d) Output stage of Filter OTA's,

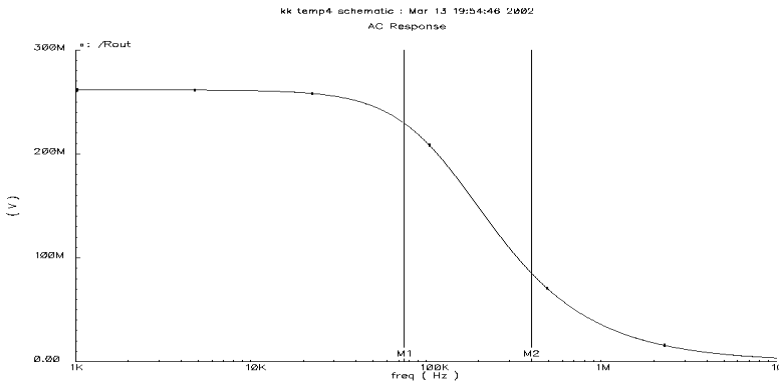

Figure 6. OTA's output resistance.

the VCO. The reference frequency defines the channel selected to transmit information and this frequency is included in the protocol of the message which alerts the Slave Modules to change the transmission channel if the communication is detected to be defective.

The RC filter block, shown in Fig.5 (b), settles the variation of Vtuning; thus, to obtain a good precision in the tuning frequency it is necessary a very large value of the capacitor. This has been the reason to implement it off chip. The value for the passive filter has been selected to assure stability, settling time and loop bandwidth requierements.

As it has been said before, the bandpass filter and the voltage controlled oscillator have the same frequency dependence when the tuning voltage is changed.Fig. 7 shows the tuning frequency of the filter and the spectrum obtained with the VCO for three different values of the tuning voltage. It is shown there how the frequency behaviour in both cases is nearly the same, with a deviation that is always under 2 kHz between each other.

Using the OTA's proposed before, the compesation of the VCO needed for the ASIC has been performed as illustrated in Fig.8 (a). The degradation of the transconductor linearity generates start-up problems. To avoid these problems, an AGC circuit has been considered. Fig.8 (b) shows how the approach has been followed at a system level, then, in Fig.8 (c) it is

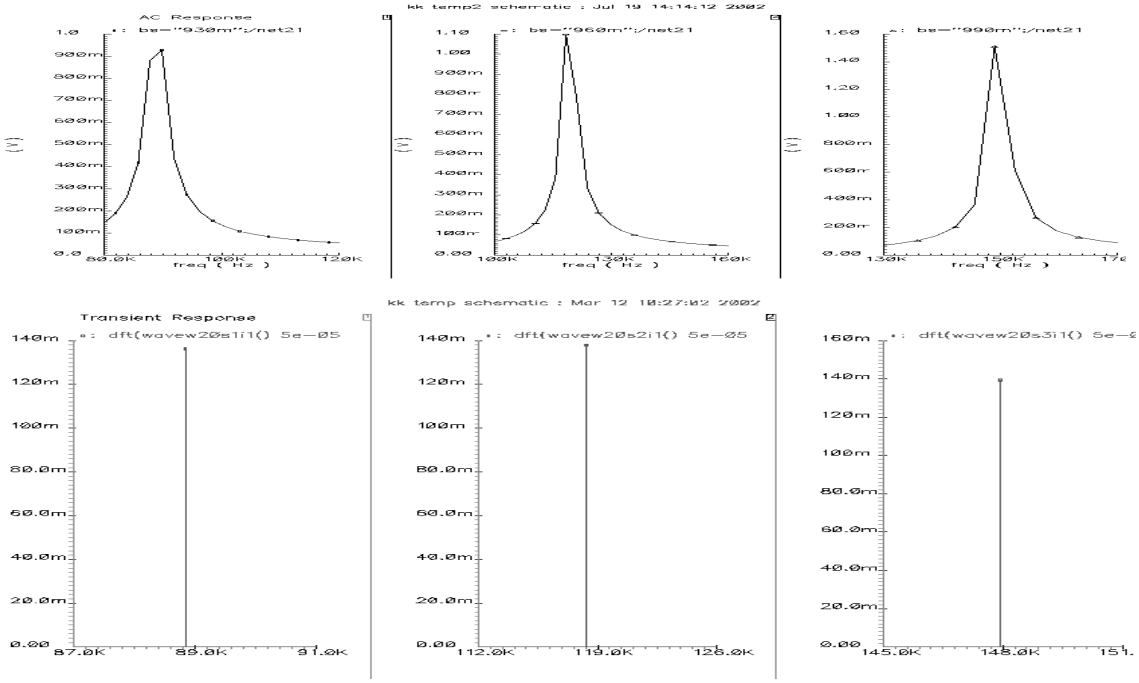

Figure 7. Filter and VCO Frequency simulations

shown the transistor level schematic used for the implementation.

The rectifier circuit of Fig. 8 (b), provides a positive current, that induces small voltage variations in the input node of the comparator, thus provoking a shifting in its output voltage. This is how variations in the OTA currents are converted into an adjustable tuning voltage to accomplish the negative feedback in the oscillator. Notice that due to the fact that the feedback in the oscillator depends on the transconductances of the feedback OTA's (gm_3 and gm_4) if gm_3 value is fixed (settling its control voltage by using an external reference), modifying the feedback coefficient is naturally performed by changing gm_4 value.

As can be shown in Fig.8(c), the rectifier in Fig.8 (b) has been implemented using two half-wave rectifiers, [8], and a differential input has been proposed. To have the comparator working properly the transistors M1 and M2 in Fig.8(c) have been located in the limit between cut-off and conduction. Finally, three inverters have been added to scale the voltage shifting in the output node of the comparator and to centre it around the desired value.Thus, the circuit's output is a voltage changing according to the variation of the OTA current in a range of 0.93V to 0.99V.

Table 1 shows the different tuning frequency ranges corresponding to the diverse values of the capacitors and the limiting values for the ranges of gm_1 and gm_2 transconductances and the tuning voltage. As can be seen there, an overlapping between the frequency channels has been forced to ensure the availability of the whole range in case of errors caused by imperfections in the final design.

Table 1: Tuning frequency ranges

C1,C2 (pF)	Vtuning (V)	gm (μV/A)	f (kHz)
2.25	0.93-0.99	1.316-2.224	87.1-151.4
1.5			128.8-218.8
1			186.2-316.2
0.66			295.1-501.3

An important verification is to check that the PLL operates properly. To guarantee this, the PLL is simulated with different signals of the digital clock at its input. To know if the PLL is performing well it is required to verify that the frequency of the VCO is the same that the reference one. Fig. 9 shows the signals UP and DOWN obtained when the

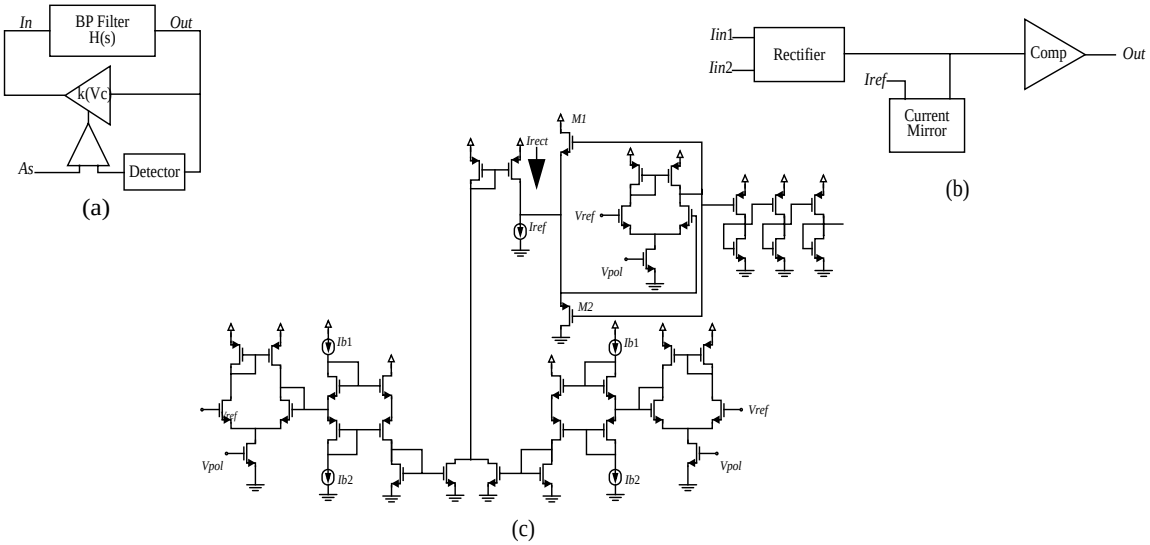

Figure 8. (a) Compensation circuitry for the VCO, (b) System level structure of the AGC, (c) AGC schematic.

reference's frequency and the VCO frequency are compared in the digital phase detector, the tuning voltage and the comparator's output.

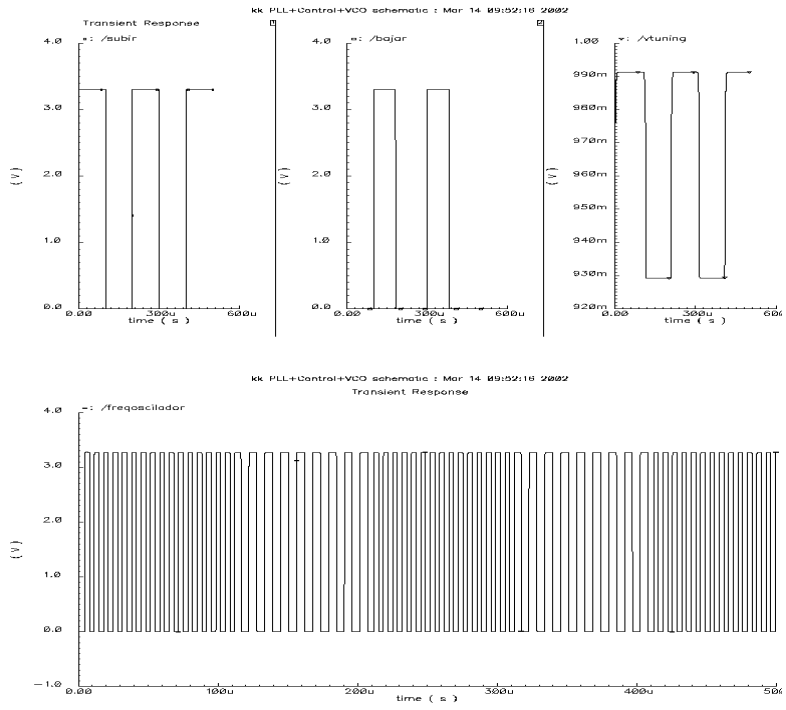

Figure 9. PLL's behaviour

4.CONCLUSIONS

The LFM of a mixed-signal ASIC to control the in-house communications with external control units has been present-

ed. This module occupies an area of 2.5mm^2, with a maximum power consumption of 9.3mW. The quality of the design has been settled by several experimental results that confirm the capabilities of the circuit.

Adding the functionality of the presented module to the existing HFM allows the creation of a cheap network to control in-house appliances.

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