A ΣΔ modulator for a programmable-gain, low-power, high-linearity automotive sensor interface

José M. de la Rosa*, Fernando Medeiro, Belén Pérez-Verdú, Rocío del Río and Angel Rodríguez-Vázquez

Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC)
Edificio CICA-CNM, Avda Reina Mercedes s/n, 41012-Sevilla, SPAIN

ABSTRACT

This paper describes the design and electrical implementation of a 0.35μm CMOS 17-bit@40kS/s Sigma-Delta Modulator (ΣΔM) forming part of a sensor interface for automotive applications. First of all, the paper discusses the most important limiting factors and design considerations applicable to a high-resolution ΣΔM for sensor interfaces. After an exhaustive comparison among multiple ΣΔM architectures in terms of resolution, speed and power dissipation, a third-order (2-1) cascade ΣΔM is chosen. For a better fitting to the characteristics of different sensor outputs, the ΣΔM here includes a programmable set of gains (0.5, 1, 2, and 4). The gain programmability is implemented by a reconfigurable capacitor array of unitary capacitors. In order to relax the amplifier dynamics requirements for the different modulator gains, switchable capacitor arrays are used for all the capacitors in the first integrator. The design of the modulator building blocks is based upon a top-down CAD methodology which combines simulation and statistical optimization at different levels of the modulator hierarchy. Behavioural simulations considering transistor-level circuit parasitics shows a Dynamic Range (*DR*) over 105dB for all cases of the modulator gain.

Keywords: Analog-to-digital converters, sigma-delta modulators, automotive sensor interfaces.

1. INTRODUCTION

Since the introduction in the late 1970s of microprocessor-based automotive engine-control modules that regulated gas emissions, there has been an ever increasing penetration of electronic control systems in the automotive industry. In these systems, sensors play a critical role, covering a wide range of data capturing functions in multiple parts of the vehicle, such as the engine, powertrain and braking[1]. In recent years, the number of applications is increasingly growing with the combined use of sensors and Integrated Circuits (ICs) using the so-called MicroElectroMechanical (MEM) technologies[2]. These technologies have made possible a new generation of "smart" sensors that combine digital signal processing and communication with the environment on a single chip or within the same package. In the case of automotive components, MEM sensors must operate under very adverse environmental conditions with extreme temperatures ([–40°C, 175°C]), mechanical shocks (50 – 500g on the vehicle), electromagnetic interferences, etc[1-3].

Therefore, the measuring circuit driving the sensor, normally formed by a low-noise preamplifier and an Analog-to-Digital Converter (ADC) (see Fig.1), must be very accurate and robust in order to handle the typically weak sensor output signals (ranging from μVs to hundreds of mVs) in the hostile conditions mentioned above[4-7]. This is aggravated in most

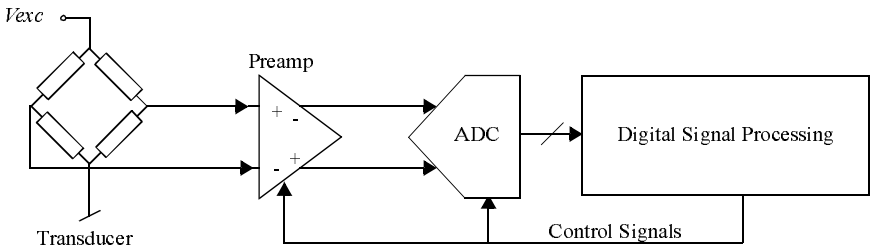

Figure 1. Conceptual block diagram of a "smart" sensor chip.

* jrosa@imse.cnm.es; phone +34955056666; fax +34955056686; www.imse.cnm.es

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applications as a consequence of the offset voltage due to the excitation voltage supplying most transducers. In practice, that offset voltage is subject to temperature and manufacturing process variations, thus causing a shift in the signal range provided by the sensor. Hence, the measuring circuit must accommodate the complete range of possible offsets and real signals. The same problem arises in multi-purpose sensors. In such devices, a programmable gain preamplifier is used to boost the sensor signal to a workable level where the ADC digitizes it and the rest of processing is carried out in the digital domain[6].

In this scenario, the use of ADCs based on Sigma-Delta Modulators (ΣΔMs) is convenient for several reasons. On the one hand, the noise-shaping performed by ΣΔMs allows to achieve high resolution (typically 16-17bits) in the band of interest (10-20kHz), with less power consumption than full Nyquist ADCs[8-9]. On the other hand, the action of feedback renders ΣΔMs very linear, and high-linearity is a must for automotive applications. Besides, in some of these applications the principle of the sensing devices fits in with the topology of the ΣΔM, thus allowing partial or total integration of the sensor in the converter structure[10-11]. Last but not least, the robustness of ΣΔMs with respect to circuit imperfections make them suitable to include programmable gain without significant performance degradation[7]. This feature allows to accommodate the complete range of possible offsets and information signals in a sensor interface with relaxed specifications for the preamplifier circuitry.

This paper describes the design and implementation of a third-order cascade (2-1) ΣΔM with programmable gain in a 0.35μm CMOS technology – the type of technology commonly employed for automotive applications (deep submicron is mostly employed for telecom). According to precise simulations which take into account transistor-level performance and technological parasitics, the ΣΔM here is capable of handling signals up to 20-kHz bandwidth with 17-bit resolution for all cases of modulator gain (0.5, 1, 2 and 4), considering a temperature range of $[-40°C, 175°C]$ with a worst-case power consumption of 25mW. To achieve these features, a top-down CAD methodology has been followed which combines simulation and statistical optimization at different levels of the modulator hierarchy[9].

The paper is organized as follows. Section 2 briefly reviews the fundamentals, architectures and major circuit limitations of ΣΔMs, paying special attention to the most critical limiting factors in sensor interface applications. Section 3 applies the design considerations derived from Section 2 to choose the most appropriate architecture to be implemented in the programmable gain sensor interface in terms of resolution, speed and power dissipation. Section 4 describes the design of the building blocks at the transistor-level to achieving the required specifications. Finally, Section 5 shows several behavioural simulation results including electrical performance of building blocks and technological parasitics.

2. FUNDAMENTALS AND CIRCUIT LIMITATIONS OF ΣΔMs

Fig.2 shows the conceptual block diagram of a ΣΔ ADC which includes three basic components: an anti-aliasing filtering, a ΣΔM, and a digital decimator[8-9]. The signal is oversampled and quantized in the modulator. This block also filters the quantization error, by shaping its Power Spectral Density (PSD) in such a way that most of its power lies outside of the signal band, where the error is eliminated by digital filtering. The modulator output – coded into a reduced number of bits – is passed through the decimator, where, after filtering all the components out of the signal band, data are decimated to reduce the sampling frequency, f_S, down to the Nyquist frequency, f_N. The result is the signal coded in a large number of bits and clocked at f_N.

Among the converter blocks, the modulator is the hardest to design, since oversampling simplifies the anti-aliasing filter requirements and the decimator is a pure digital block whose design can be highly structured and automated[8]. As shown in Fig.2, the modulator output, y, is substrated from its input, x, which has been sampled at a rate much larger than f_N. The result is filtered by $H(z)$, and passed through a quantizer, which usually has a reduced number of levels. If the gain of $H(z)$ is high in the band of interest, and low outside of it, the quantization error is attenuated within the band due to the feedback loop.

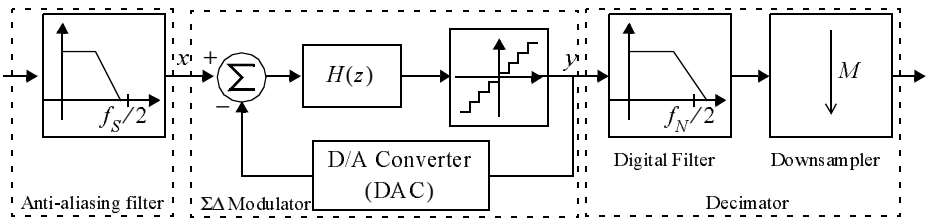


Figure 2. Block diagram of an oversampling ΣΔ ADC.

Assuming that the quantization error can be modelled as an additive, white noise source, e, the Z-transform of y is given by:

$$Y(z) = S_{TF}(z)X(z) + N_{TF}(z)E(z) \tag{1}$$

where $X(z)$ and $E(z)$ are the Z-transform of the input signal and quantization noise, respectively; $S_{TF}(z)$ and $N_{TF}(z)$ are the respective transfer functions of the input signal and quantization noise, given by

$$S_{TF}(z) = \frac{H(z)}{1+H(z)} \qquad N_{TF}(z) = \frac{1}{1+H(z)} \tag{2}$$

In case of *lowpass* signals like that handled by sensors interfaces, the modulator loop filter, $H(z)$, is properly chosen to obtain the following transfer functions

$$S_{TF}(z) = z^{-L} \qquad N_{TF}(z) = (1-z^{-1})^{L} \tag{3}$$

thus implementing the noise shaping concept illustrated in Fig.3 for different values of the modulator order, L. In this figure, the input signal is a sinewave of amplitude $X = X_{FS}/4$, with X_{FS} being the full-scale range of the quantizer.

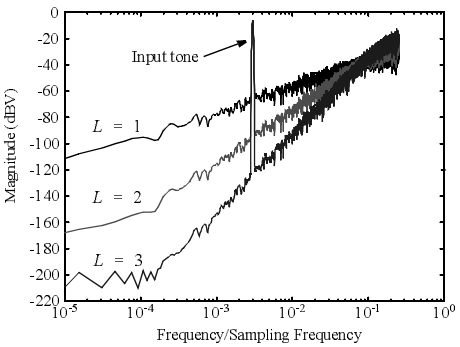


Figure 3. Noise shaping concept in ΣΔMs.

The *in-band* quantization noise power can be calculated by integrating the output noise PSD within the signal band, B_w, giving:

$$P_Q = \int_0^{B_w} 2S_Q|N_{TF}(f)|^2 df \cong \frac{\pi^{2L}\Delta^2}{12(2L+1)M^{(2L+1)}} \tag{4}$$

where $S_Q = \Delta^2/(12f_S)$ is the PSD of the quantization noise, Δ is the quantization step, and $M \equiv f_S/(2B_w)$ is the *oversampling ratio*. From (4), and assuming that the modulator input is a sinewave of amplitude X, the Signal-to-Noise Ratio (SNR) at the output results in:

$$SNR = \frac{X^2}{2P_Q} = \frac{6(2L+1)M^{(2L+1)}}{\pi^{2L}\Delta^2}X^2 \tag{5}$$

The modulator Dynamic Range (DR) is obtained by making $X = X_{FS}/2$ in the above expression. For an N-bit quantizer, $\Delta = X_{FS}/(2^N - 1)$, and hence

$$DR = \frac{3(2^N-1)^2(2L+1)M^{2L+1}}{2\pi^{2L}} \tag{6}$$

2.1 Main ΣΔM architectures

The simplest way of implementing an L*th*-order ΣΔM consists of including L Forward-Euler (FE) integrators before the quantizer as illustrated in Fig.4(a), usually referred to as L*th*-order single-loop ΣΔM. An important limitation of these architectures is their tendency to instability for $L > 2$. An alternative to single-loop ΣΔMs are the cascade architectures (also named multi-stage or MASH) whose generic block diagram is shown in Fig.4(b). Their functioning is based on the cascade connection of low-order modulators ($L \leq 2$), whose stability is guaranteed by design. The quantization noise generated in one stage is then re-modulated by the next one, and later cancelled in the digital domain. As a result, one obtains the modulator input plus the quantization noise of the last stage, attenuated by a shaping function of order equal to the number of integrators in the cascade.

Usually, the first stage of cascade ΣΔMs is a second-order single-loop and the remaining stages are first-order modulators. For that reason, these architectures are often referred to as 2-1^{L-2} ΣΔMs. As an illustration Fig.4 shows two cascade modulators using the mentioned stage distribution. Fig.4(c) is a 2-1 cascade modulator, which as demonstrated later, is a good candidate to be included in the sensor interface. Fig.4(d) is a 2-1^2 with *multi-bit* (mb) quantization only in the

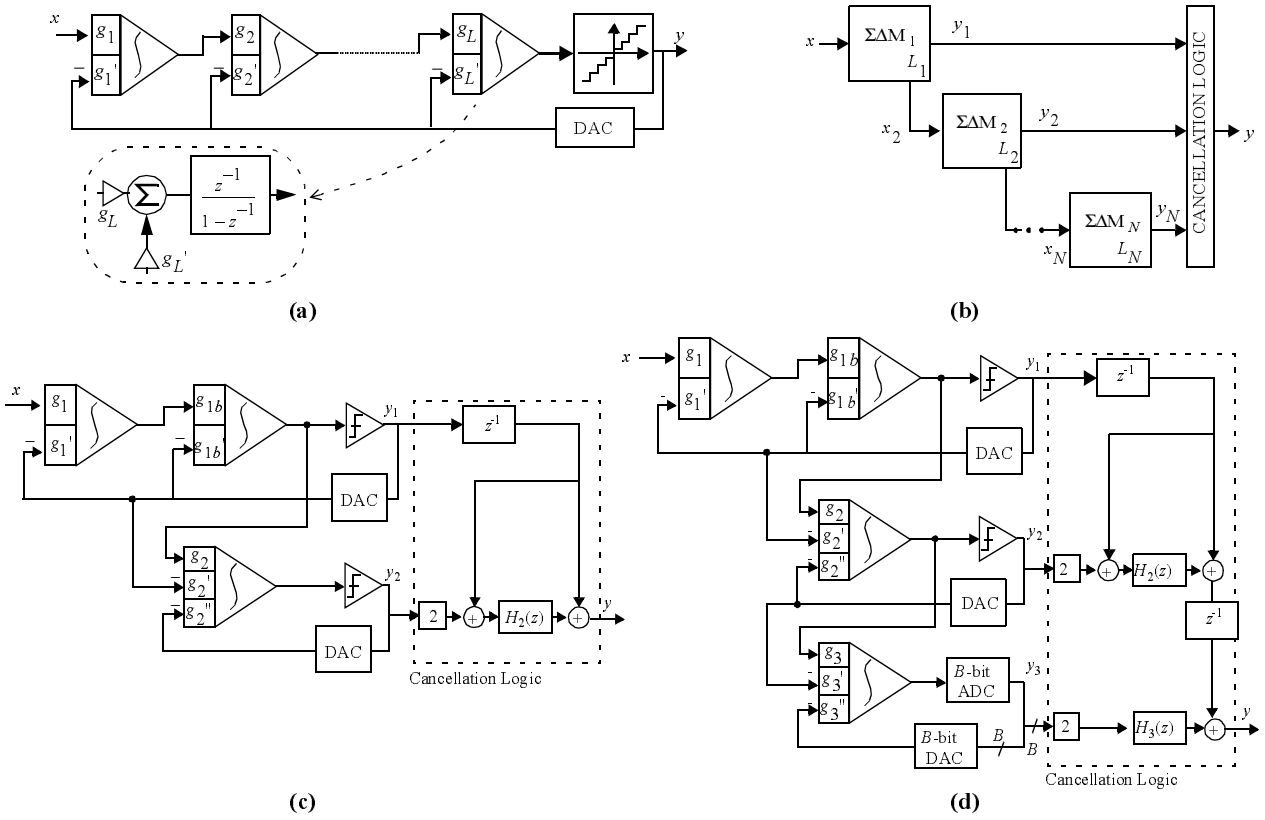


Figure 4. Main ΣΔM architectures. (a) *Lth*-order single-loop. (b) *Lth*-order cascade. (c)-(d) Practical realizations.

last stage (2-1^2 mb). In such a way, the DAC non-linearity error is attenuated by a shaping function and filtered out by the digital decimator. The values of the integrator weights are the following[12]:

$$g_{1a} = g_{1a}' = 0.25;\ g_{1b} = 1, g_{1b}' = 0.5;\ g_k = 1, g_k' = 0.5, g_k'' = 0.5 \qquad k = 2, \ldots, L-1 \tag{7}$$

and the digital blocks are $H_k(z) = (1 - z^{-1})^k, \quad k = 2 \ldots L-1$.

2.2 Circuit limitations and design considerations

In the discussion above, ΣΔMs have been considered ideal except for the inherent quantization error. However, in practical implementations, the in-band error power of whatever ΣΔM can be expressed as the summation of the contributions due to several circuit error mechanisms[9],

$$P_{\text{in-band}} \cong P_Q + P_{cn} + P_{nl} + P_{st} \tag{8}$$

where right-hand side terms stand for quantization error, circuit noise, non-linearity error, and defective settling error powers, respectively. Although depending on the modulator type the basic P_Q (see eq. (4)) can be altered by circuit imperfections, the most important impact of such circuit imperfections is to be found in the remaining contributions in (8). For modest performance, the circuit requirements to render $P_{cn} + P_{nl} + P_{st} \ll P_Q$ are not demanding. However, this is not the case for really challenging specifications, like those required in sensor interfaces, where the achievement of high resolution forces designers to work on the edge of feasibility. In these designs, the quantization error usually plays a secondary role.

For obvious reasons, out of the circuit imperfections above, dynamic limitations are not an issue in low-frequency sensor applications. On the contrary, circuit noise contribute 90% of the in-band error power in a typical design, thus deserving especial attention in this section.

Consider the two-branch SC FE integrator in Fig.5, that assumes that the signal sampling capacitor, C_{11}, can be different from the feedback sampling capacitor, C_{12}, in order to create a modulator input-output gain $\xi = C_{11}/C_{12}$. In this circuit the noise contributors are the OTA (thermal + flicker noise) and the switch on-resistance (thermal noise). Also, potential noise coming from the reference voltage (V_{ref}) generation block must be accounted for, which overall will be a mixture of white and flicker noise. Whereas flicker noise can be very efficiently removed from the signal band by applying chopper techniques[5-6], for example, the low-frequency white noise PSD is boosted by the well-know aliasing mechanism: due to dynamic requirements, the equivalent noise bandwidths for these contributions are well in excess of half the sampling frequency, thus causing aliasing of their PSD. A careful analysis shows that the input-equivalent white noise PSD per fully-differential branch can be approximated (at low frequencies) by,

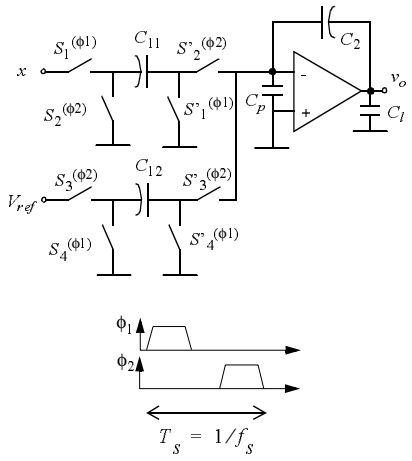


Figure 5. Two-branch SC integrator.

$$S_{in,C_{11}}(f) \cong \frac{4kT}{C_{11}f_S} + \frac{4kT(1+n_t)}{3C_{eq,i}f_S}; \qquad S_{in,C_{12}}(f) \cong \frac{4kT}{C_{12}f_S} + \frac{4kT(1+n_t)}{3C_{eq,i}f_S} + \frac{kT}{C_{12}f_S}\cdot\frac{R_{eq,ref}}{2R_{on}} \tag{9}$$

where k is the Boltzman constant, T is the absolute temperature and R_{on} is the switch-on resistance. The first term corresponds to the contribution of all the switches in each branch, the second one is for the OTA contribution, where

$$C_{eq,i} = C_p + C_{12}(1+\xi) + C_l\left[1 + \frac{C_p + C_{12}(1+\xi)}{C_2}\right] \tag{10}$$

is the OTA equivalent load during the integration phase (ϕ_2 high). In estimating the white noise PSD of the OTA, the contributions of MOS devices other than the input ones are compiled in the factor n_t, which equals the summation of the respective transconductance ratios. The third term in $S_{in,C_{12}}$ represents the noise coming from the DAC reference voltages, V_{ref}, with $R_{eq,ref}$ being its equivalent noise resistance.
By neglecting contributions other than the first integrator's, the ΣΔM output white noise power is obtained:

$$P_{wn} \cong \frac{4kT}{MC_{12}}(1+\xi) + \frac{4kT(1+n_t)}{3MC_{eq,i}}(1+\xi)^2 + \frac{kT}{MC_{12}}\frac{R_{eq,ref}}{2R_{on}\xi^2} \tag{11}$$

In obtaining (11), the OTA noise contributions in (9) have been considered fully correlated because it is the same circuitry and its noise is sampled at the same instant. From this point, some recommendations can be made for the design of a high-resolution ΣΔM:

- For given M and ξ, choose the feedback sampling capacitor, C_{12}, large enough to make the first term in (11) smaller than the maximum allowed in-band error power.
- The previous recommendation assumes that second and third contributions in (11) are less important, which requires that both the OTA and switch dynamic performances are not oversized.

Another fact clearly visible in (11) is that the output white noise power depends on the ΣΔM gain, ξ. The first two terms increase with ξ, while the third one decreases. The overall trend for P_{wn} is to increase with ξ. Also, as (10) shows, the OTA equivalent load increases with ξ, thus requiring more demanding dynamics and, hence, dissipating more power. The immediate conclusion is that the ΣΔM gain should be as close as possible to unity. In fact, if $\xi = 1$ the second branch in Fig.5 is not necessary thus reducing even more P_{wn} and, consequently, $C_{eq,i}$. This choice, commonly found in literature[6], puts the ball back into the preamplifier's court, rendering its design more complicate and the overall programmability less flexible.

3. ARCHITECTURE SELECTION AND HIGH-LEVEL SIZING

Comparing eqs. (4) and (11), it can be seen that, for each ΣΔM architecture, there will be a value of M for which $P_Q \cong P_{wn}$. In order to illustrate this, Fig.6 shows the effective resolution measured from three ΣΔMs (4th-order 3bit, 3rd-order 1bit, and 2nd-order 1bit, all of them with the same front-end integrator) as a function of M. Differences among curves are justified by the different modulator orders and the fact that one of them is multi-bit. However, note that in each curve there is a change in the slope which coincides with the point beyond which the in-band error power is dominated by the first integrator white noise, and quantization error is not an issue any more. This is the reason why the three curves converge for sufficiently high M. Once in this region, doubling M generates a mere 3dB decrease in error power (i.e., 0.5-bit increase in effective resolution). In Fig.6, the only way to shift up the white-noise-limited region is to increase the value of the sampling capacitors. Our experience and other design evidences in the open literature show that efficient ΣΔMs are those located slightly inside this region: that is, with some equilibrium between P_Q and circuit-derived error power. Intuitively, this is due to the following rationale: (a) if for the oversampling ratio selected, P_Q clearly dominates the in-band error power (design located at the high-slope region of the curves in Fig.6), the building block specifications are bound to be oversized; (b) otherwise, (for design located deep in the low-slope regions), probably L or B (or both) could have been reduced without significant impact on resolution.

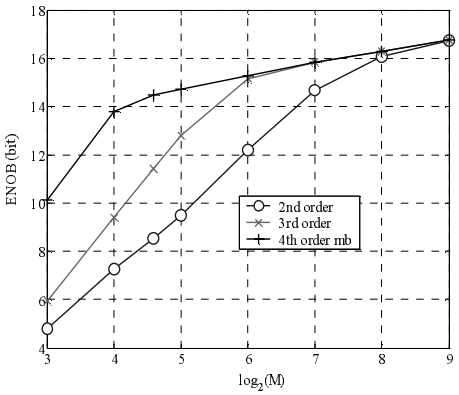


Figure 6. Effective resolution vs. oversampling ratio.

Contrary to high-frequency applications (e.g., communications), in sensor applications we can take maximum advantage of the maneuverability of M, making use of a highly-oversampled ΣΔM to fulfil the high-resolution requirements. This will push our design to the right in Fig.6, so that high-order and/or multi-bit architectures seem to be impractical. However, note that, if for a certain low-frequency application, the resolution does not have to be that high, thus requiring less oversampling, it will be sensible to try high-order and/or multi-bit solutions, as the equilibrium point between quantization error and circuit error moves to the left in Fig.6.

In order to quantitatively evaluate these qualitative considerations, an approximate (iterative) procedure can be implemented making use of the equations in the previous section to estimate the implementation cost of different architectures. For the sake of brevity, we will only sketch the main steps:

- For given values of L, M, N, V_{ref} and ξ, calculate P_Q and select C_{12} so that $P_Q + P_{wn}$ is smaller than the maximum allowed in-band error power.
- Estimate $C_{eq,i}$ from (10). Then, a linear settling model with settling constant $C_{eq,i}/g_m$ can be used to estimate the OTA transconductance required, since it takes a number $\ln(2^{ENOB})$ of time constants to settle within Effective Number Of Bits ($ENOB$) resolution.
- Relate the OTA g_m with the OTA power dissipation, for which the candidate OTA topology must be known a priori. A suitable selection is extremely linked to the fabrication process: supply voltage, minimal device length, etc. Sensible choices are a folded-cascode OTA up to 3-V supply, and a two-stage amplifier below 2.5V.
- Once the first integrator power dissipation is estimated, that of the remaining integrators (in practice with less demanding specifications) can be estimated as a fraction of it. The overall static power of the modulator is then obtained by adding up all the contributions.

Of course, fine-tuning of this procedure is required for more realistic estimations, including the impact of other non-ideal effects (such as finite and non-linear OTA DC-gain, slew-rate, errors in the multi-bit quantizers, etc.), power dissipation in other blocks, as well as the dynamic power dissipation[12]. In addition, the power dissipation and silicon area of the required decimation filter must be included in the trade-off towards architecture selection.

3.1 Modulator architecture

The design considerations described above have been applied to design a 17-bit effective resolution, 40-kS/s ΣΔM

for an automotive sensor interface requiring Signal-to-(Noise + Distortion) Ratio ($SNDR$) > 100dB within a temperature range of ([−40°C, 175°C]). The intended technology is a 3.3-V 0.35μm CMOS, with M-i-M capacitors available. In order to obtain the best ΣΔM that fulfils these specifications, the architecture selection procedure sketched above has been used and a large number of architectures have been compared using the following Figure-Of-Merit (FOM),

$$FOM = \frac{Power}{2^{\mathrm{ENOB}} \times DOR} \times 10^{12} \tag{12}$$

which measures the energy needed per conversion in pJ[13].

Table 1 shows the outcome of the comparison for ΣΔMs with 1-bit quantization, showing the best cases (sorted in terms of FOM) for each case of the modulator gain. In addition to the FOM, the modulator order (L), the oversampling ratio (M), and the power consumption are also included in Table 1. Note that the third-order 2-1 cascade architecture obtains the best result except for the case of $\xi = 4$. In this case the best FOM is obtained by a 2nd-order single-loop ΣΔM with $M = 512$, the third-order being the second one in the ranking. However, the 2-1 architecture has been preferred to the 2nd-order architecture because the latter requires $M = 512$, i.e. a 20.4 MHz sampling frequency, – discarded for several practical reasons, among the others: a less relaxed design of building blocks and switching noise coming from the digital part[14].

Fig. 7 shows the block diagram of the selected architecture together with the values for the analog coefficients. Note that the first integrator contains two differential input branches: one of them is for the sensor signal, in which double sampling is used to achieve an extra signal gain of 2, without increasing circuit noise[15]. The second branch receives the DAC outputs. Making use of the spare connection of the second branch, an external DC signal (V_{off}) can be applied during ϕ_1 to center the sensor signal in the modulator full-scale range. This solution renders unnecessary a third branch for offset compensation with the subsequent thermal noise saving.

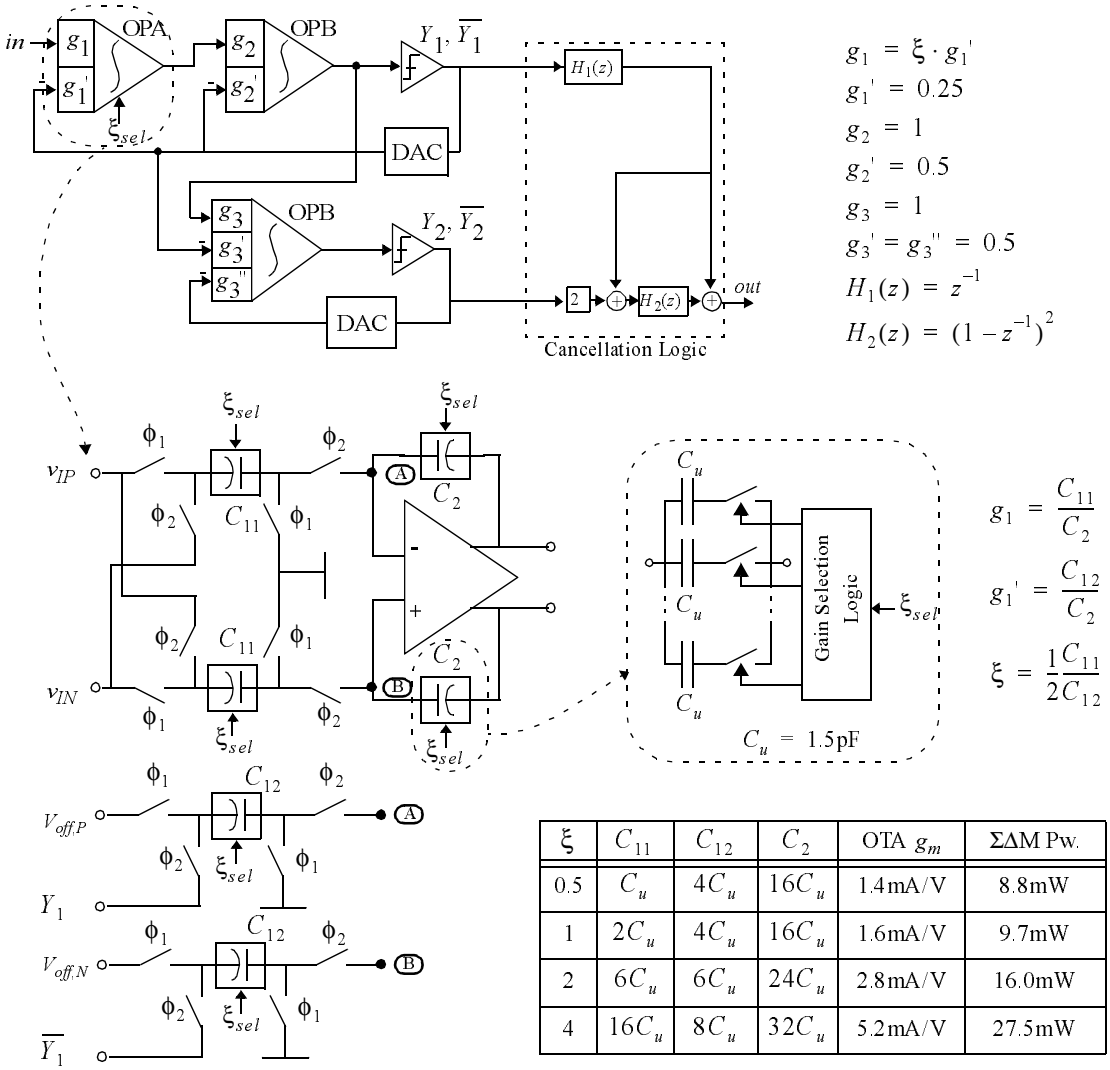
The programmable gain ($\xi = 0.5, 1, 2$ and 4) has been mapped onto switchable capacitor arrays, each of them formed by a variable number of unitary capacitors. Such numbers and the unitary value (also shown in Fig.7) are selected for minimum power dissipation, bearing in mind the circuit noise limitation and the high temperature required for this sensor interface, (175°C). In order to keep the amplifier dynamic requirements as relaxed as possible, we propose to switch the number of unitary capacitors forming all the capacitances involved (not only the ones forming the sampling capacitors). The rationale behind this proposal is the following:

- For low gain cases the capacitor sampling the signal (C_{11}) must be small compared to the V_{ref} and offset compensation sampling capacitor (C_{12}). According to (11), the input-referred thermal noise power appears multiplied by ($1+C_{12}/C_{11}$), which means that it will be amplified with respect the unity gain case.
- For large gains the situation is the opposite. Now thermal noise power is reduced with respect to the unity gain case, which allows us to decrease the capacitance values. This strategy also relaxes the minimum required amplifier dynamics because its equivalent load capacitance will be also decreased. Furthermore, by manipulating the tail current of the first OTA, the estimated power dissipation of the complete ΣΔM (tabulated in Fig.7) adjusts to the specific application.

Table 1: Outcome of the ΣΔM architecture selection

ΣΔM Gain, ξ	Order (L)[a]	Oversampling Ratio (M)	Pow. Cons. (mW)	FOM (pJ/conversion)
0.5	3	128	6.77	1.291
	3	256	8.12	1.548
	4	128	8.27	1.578
1	3	128	8.48	1.618
	3	256	9.77	1.863
	4	128	10.32	1.969
2	3	128	12.69	2.422
	3	256	13.85	2.641
	2	512	13.88	2.647
4	2	512	23.24	4.432
	3	128	24.21	4.618
	3	256	25.02	4.772

a. All ΣΔMs in this table are cascade architectures except for $L = 2$.



ξ	C_{11}	C_{12}	C_2	OTA g_m	ΣΔM Pw.
0.5	C_u	$4C_u$	$16C_u$	1.4mA/V	8.8mW
1	$2C_u$	$4C_u$	$16C_u$	1.6mA/V	9.7mW
2	$6C_u$	$6C_u$	$24C_u$	2.8mA/V	16.0mW
4	$16C_u$	$8C_u$	$32C_u$	5.2mA/V	27.5mW

Figure 7. Modulator architecture with switchable gain.

- In order to simultaneously handle the modulator gain ($2C_{11}/C_{12}$) and the first integrator feedback weight (C_{12}/C_2 always equal to 0.25), the value of all capacitances must be changed by re-arranging the number of unitary capacitors forming them.

3.2 High-level sizing

The ΣΔM in Fig.7 has been high-level sized, i.e, the modulator specifications have been mapped onto building-block specifications using statistical optimization for design parameter selection, and compiled equations (capturing non-ideal building block behaviour) for evaluation. This process is fine-tuned by behavioural simulation using ASIDES, an advanced behavioural simulator of SC ΣΔMs. At this step, non-idealities are covered more accurately than in the case of using compiled equations. Also, worst cases for speed (the largest capacitor values) and for thermal noise (the highest temperature and the lowest capacitor values) are contemplated.

The results of this sizing process are summarized in Table 2, in which OPA denotes the opamp used at the first integrator in the chain and OPB refers to the opamps used at the second- and third- integrator in the modulator chain (see Fig.7). The data in Table 2 define the specifications of the building blocks, which are the starting point for electrical sizing.

Table 2: Results of high-level sizing for the 2-1 ΣΔM with programmable gain

SPECS: 17bit@40kS/s@2V_p			2-1 Arch.	Unit
MODULATOR	Oversampling ratio		128	
	Sampling frequency		5.12	MHz
	Reference voltages		±2.0	V
	Estimated Power Consumption	Gains 0.5+1+2+4	27.5	mW
		Gains 0.5+1+2	16	mW
		Gains 0.5+1	9.7	mW
		Gain 1+2	16	mW
INTEGRATORS	Integration capacitor	Gain 0.5	24	pF
		Gain 1	24	pF
		Gain 2	36	pF
		Gain 4	48	pF
	Unitary capacitor		1.5	pF
	Sigma (assumed from tech.)		0.1	%
	Capacitor non-linearity (assumed from tech.)		25	ppm/V^2
	Bottom parasitic capacitor (assumed from tech.)		5	%
	Switch ON-resistance		<650	Ω
OPAMPS	DC-gain	OPA	68	dB
		OPB	63	dB
	DC-gain non-linearity		15%	V^{-2}
	GBW	OPA (44.2pF load)	17	MHz
		OPB (8.9pF load)	15	MHz
	Slew-rate	OPA (44.2pF load)	17	V/μs
		OPB (8.9pF load)	28	V/μs
	Output swing		±2.5	V
COMPARATORS	Hysteresis (max.)		30	mV

4. DESIGN OF BUILDING BLOCKS

The modulator building blocks, namely, amplifiers, comparators and switches have been conveniently selected and sized according to the requirements given in Table 2. Design considerations on each of these blocks as well as their electrical performance using HSPICE are detailed in this section.

4.1 Amplifiers

The key features for the design of the amplifiers are their open-loop DC-gain, dynamic requirements and output swing, where the last one becomes especially critical in a low voltage implementation. Nevertheless, the set of integrator weight used for the ΣΔM in Fig.7 allow us to relax the output swing requirements to be slightly larger than the reference voltages – 2V in this case –, which is feasible when operating with 3.3-V supply in differential mode.

Note from Table 2 that the requirements for the OPA are more aggressive than those for the OPB since the contribution of the latter to the total in-band error power is attenuated by increasing powers of the oversampling ratio. This recommends, in order to avoid oversizing and optimize the power consumption, to obtain two different designs: one for the OPA and other one for the OPB.

For this purpose, the transistor-level sizing tool FRIDGE[9] was used to explore the potential of several OTA fully-differential topologies. The search criteria were the achievement of the specifications for OPA and OPB with minimum power dissipation and reduced circuit complexity. After this exploration, a single-ended folded-cascode architecture, shown in Fig.8(a), was selected for both amplifiers. Note that an N-type input pair has been considered because a twin-well technology is used, and hence, the body effect can be removed in NMOS. The Common-Mode Feed-Back (CMFB) net has been implemented using a SC circuit, which provides fast and linear operation with small power dissipation.

Table 3 summarizes the electrical performance of both amplifiers in terms of target values imposed during the optimization procedure in FRIDGE to the main parameters affecting the modulator specifications. The corresponding values of these parameters, obtained by electrical simulations using HSPICE, are shown for typical conditions (typical process parameters, nominal supply voltage and room temperature). Finally, Table 3 shows also the worst-case value obtained for each of the parameters in a technology corner analysis.

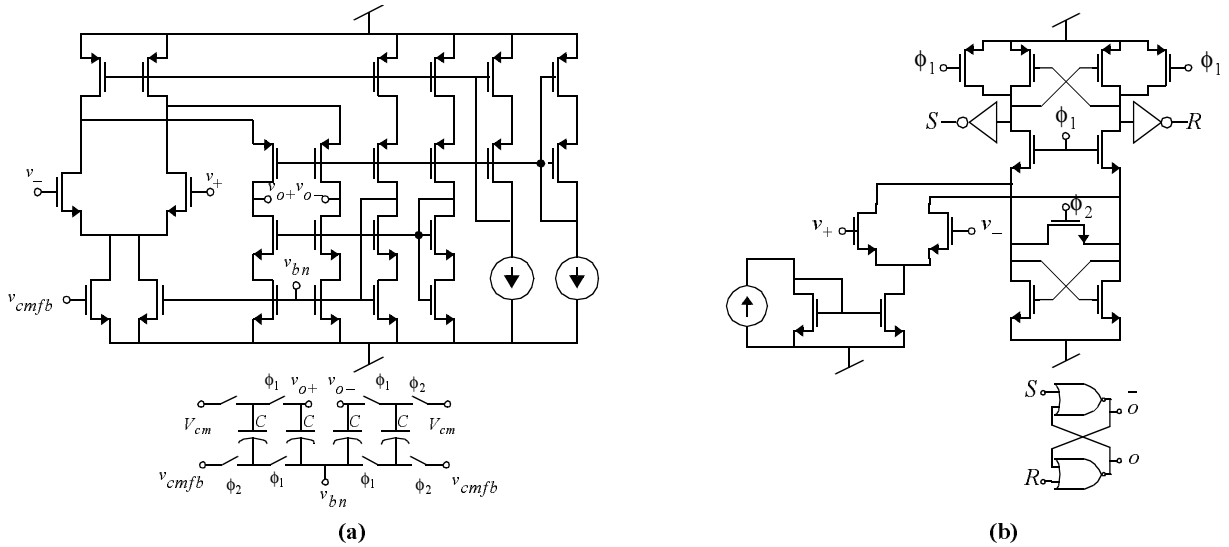


Figure 8. Building block schematics. (a) Folded-cascode amplifier with SC CMFB net. (b) Comparator.

4.2 Comparators

In order to fulfil the requirements for the 1-bit quantizer (comparator) given in Table 2, a regenerative latch including a preamplifying stage was selected – shown in Fig.8(b). The role played by the preamplifier is to improve the resolution of the comparator, which can be severely degraded in practice due to dissymmetries between the latch parameters.

MonteCarlo simulations and corner analysis have been done for characterizing the comparator performance after its full sizing. Table 4 summarizes the comparator features, showing the worst-cases for hysteresis and resolution time, together with the power dissipation.

Table 3: Electrical performance of the opamps (HSPICE)

	OPA (45pF load)		OPB(9pF load)	
Model	Typical	Worst-Case	Typical	Worst-Case
DC-gain (dB)	74.0	71.09	68.3	68.3
GB (MHz)	22.6	15.8	34.4	23.8
PM (°)	86.4	85.5	83.5	81.4
Slew-Rate (V/μs)	22.1	21.1	38.1	35.7
Output Swing (V)	±2.75	±2.5	±2.75	±2.5
Transc. (mA/V)	6.3	4.5	1.95	1.35
Power consumption (mW)	7.1	7.2	2.3	2.4

Table 4: Electrical performance of the comparators (HSPICE)

Parameter	Typical	Worst-case
Offset (mV)	0.75	9.92
Hysteresis (mV)	0.03	0.12
Resol. time, T_{RLH} (ns)	4.1	8.6
Resol. time, T_{RHL} (ns)	3.9	6.15
Power Consumption (mW)	0.43	

4.3 Switches

The value of the finite switch on-resistance, R_{on}, is mainly constricted by dynamic considerations. Incomplete settling originated by transmission gates is traditionally reduced by making $R_{on}Cf_S \ll 1$, with C being the sampling capacitor. In our design, it has been evaluated that $R_{on} < 650\Omega$ can be tolerated with no degradation of the modulator performance. This range can be obtained (considering technology corners) using CMOS switches with aspect ratios of 6.5/0.35 for the NMOS and 23.5/0.35 for the PMOS, operating with the nominal 3.3-V supply.

However, in low-voltage technologies, given that the threshold voltage of the MOS transistors is not scaled down in the same amount as the supply voltage, the voltage range in which R_{on} keeps a nearly constant value decreases. The sampling process with such an on-resistance causes dynamic distortion – the more evident the larger the sampling capacitor.

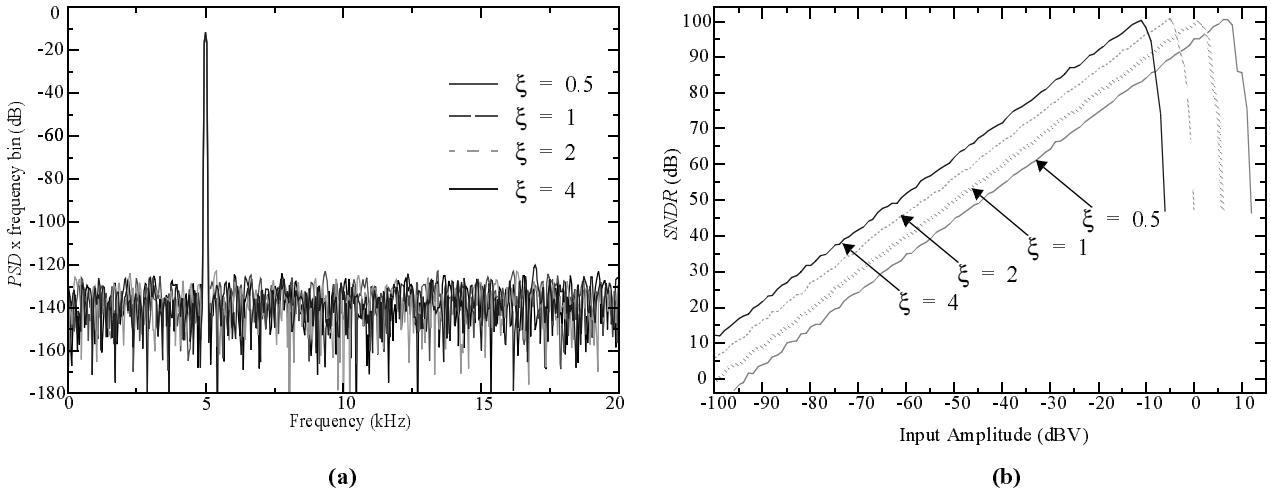
In sensor interfaces, high-linearity is a must. Therefore, the non-linear sampling effect in the first integrator has to be carefully taken into account, especially in the case of $\xi = 4$, in which $C = 24\text{pF}$. In this case the CMOS switch size given above causes harmonic distortion which can severally degrade the sensor interface performance. To avoid this, the switches used in the first integrator have been sized in order to obtain an $SNDR$ over 17bits. This is achieved by increasing the aspect ratio of the CMOS switches in the front-end integrator to 29.1/0.35 and 105.9/0.35 for the NMOS and the PMOS transistors, respectively.

5. SIMULATION RESULTS

The modulator in Fig.7 has been simulated using ASIDES. Simulations were done considering the highest temperature in the sensor interface (175°C), which corresponds to the worst-case for thermal noise. Besides, the worst-case electrical performance of building blocks described in Section 4 were used and realistic models for the M-i-M capacitors available in the intended technology were included in the simulation, considering both mismatch and non-linearity effects.

Other important effect included in the simulations is the DC-gain non-linearity, which must be carefully taken into account in (low-voltage) high-linear ΣΔMs like those used in sensor interfaces. In a typical design, the open-loop DC-gain of the amplifier varies with the DC output voltage, reaching its maximum for centred voltage (around the operating point) and decreasing as the output approaches one of the rails. In order to obtain accurate estimations for the impact of this effect, we have resorted to a look-up table procedure from opamp DC curves obtained by electrical simulation, whose data were included in ASIDES through a fast-convergence iterative procedure.

Fig.9(a) shows the output spectra for all cases of the modulator gain, ξ, corresponding to an input tone of frequency 5kHz and an amplitude at the SNR-peak. Fig.9(b) shows a set of $SNDR$-vs-amplitude curves for the different values of ξ. In all cases, the SNR-peak, which moves to left as ξ increases, is higher than 100dB. The DR is always over 105dB, corresponding to 17-bit resolution.



(a) (b)

Figure 9. Simulation results. (a) Output spectra for all cases of the modulator gain. (a) $SNDR$-vs-amplitude.

6. CONCLUSIONS

The design of a 0.35μm CMOS programmable-gain ΣΔM forming part of an automotive sensor interface has been described. Main design considerations have been discussed and applied to choose the most appropriate modulator architecture in terms of resolution, speed and power dissipation. As a result a 2-1 cascade architecture has been selected and their building blocks were designed based upon a top-down CAD methodology which combines simulation and statistical optimization at different levels of the modulator hierarchy. Behavioural simulations considering main circuit errors and technology corners show an effective resolution equal to 17 bits in a 20-kHz signal bandwidth for all cases of the modulator gain.

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