A 0.35 μm CMOS 17-bit@40-kS/s cascade 2-1 ΣΔ modulator with programmable gain and programmable chopper stabilization.

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ABSTRACT

This paper describes a 0.35μm CMOS chopper-stabilized Switched-Capacitor 2-1 cascade ΣΔ modulator for automotive sensor interfaces. For a better fitting to the characteristics of different sensor outputs, the modulator includes a programmable set of gains (x0.5, x1, x2, and x4) and a programmable set of chopper frequencies (fs/16, fs/8, fs/4 and fs/2). It has also been designed to operate within the restrictive environmental conditions of automotive electronics (-40ºC, 175ºC).

The modulator architecture has been selected after an exhaustive comparison among multiple ΣΔM topologies in terms of resolution, speed and power dissipation. The design of the modulator building blocks is based upon a top-down CAD methodology which combines simulation and statistical optimization at different levels of the modulator hierarchy.

The circuit is clocked at 5.12MHz and consumes, all together, 14.7mW from a single 3.3-V supply. Experimental measurements result in 99.77dB of Dynamic Range (DR), which combined with the gain programmability leads to an overall DR of 112dB. This puts the presented design beyond the state-of-the-art according with the existing bibliography.

Keyword list: ΣΔ modulator, chopper stabilization, gain programmability

1. INTRODUCTION

In last years has been increased the use of sensors for many applications at different parts in the vehicles, such as the engine, powertrain and braking [1]. Therefore, the number of applications is increasingly growing with the combined use of MicroElectroMechanical (MEM) sensors and Digital Signal Processors (DSPs) on a single chip or within the same package [2]. These "smart" sensors must operate under very adverse environmental conditions with extreme temperatures ([–40°C,175°C]), mechanical shocks, electromagnetic interferences, etc. Therefore, the A/D interface driving the sensor, normally formed by a low-noise preamplifier and an Analog-to-Digital Converter (ADC) as illustrated in Fig. 1, must be very robust in order to handle the typically weak sensor output signals (ranging from μVs to hundreds of mVs) in very hostile environments [3,4]. This is aggravated in most applications as a consequence of the offset voltage due to the excitation voltage (v_{exc}) supplying most transducers. In practice, that offset voltage is subject to temperature and manufacturing process variations, thus causing a shift in the signal range provided by the sensor. Hence, the sensor A/D interface must accommodate the complete range of possible offsets and real signals. In such devices, a programmable gain preamplifier is normally used to boost the sensor signal to a workable level where the ADC digitizes it and the rest of processing is carried out in the digital domain [3].

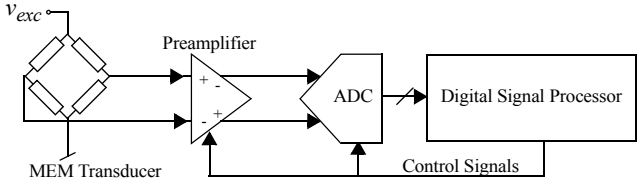

Fig.1: Conceptual block diagram of a "smart" sensor chip.

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In this scenario, the use of ADCs based on Sigma-Delta Modulators (ΣΔMs) is advisable for several reasons. On the one hand, the noise-shaping performed by ΣΔMs allows to achieve high resolution (16-17bits), in the band of interest (10-20kHz), with less power consumption than full Nyquist ADCs [6]. On the other hand, the action of feedback renders SDMs very linear, and high-linearity is a must for automotive applications. Last but not least, the robustness of ΣΔMs with respect to circuit imperfections make them suitable to include programmable gain without significant performance degradation [4]. This feature allows to accommodate the complete range of possible transducer offsets and information signals in a sensor interface with relaxed specifications for the preamplifier circuitry.

This paper describes a programmable-gain, chopper-stabilized, third-order cascade (2-1) ΣΔM in a 3.3V, 0.35μm CMOS technology. The design of the circuit is made by using an advanced top-down methodology that combines simulation and statistical optimization at different levels of the hierarchy. Experimental results show correct operation in the 20kHz BandWidth (Bw) with 110dB overall Dynamic Range (DR) and 113dB DR within Bw=10kHz. These figures locate this circuit instance at the edge of the state-of-the-art, with the added value of being one of the few high-resolution ΣΔM-based ADCs with embedded programmable-gain reported to date.

2. ARCHITECTURE SELECTION AND BLOCK SIZING

The technology used in the design of a *40-kS/s* ΣΔM for an automotive sensor interface requiring $DR \geq 110dB$ within a temperature range of ([*-40ºC,175ºC*]) is a 3.3V, 0.35μm CMOS, with Metal-insulator-Metal (M-i-M) capacitors available. In order to obtain the best ΣΔM that fulfils these specifications with the minimum power consumption, a large number of architectures have been compared in terms of the estimated power consumption and silicon area, considering the impact of main circuit error mechanisms and technology parasitics. This comparison is summarize in Table 1 for ΣΔMs with *1-bit* quantization. Note that the third-order 2-1 cascade ΣΔM shown in Fig. 2, with M=128 obtains the best result except for $\xi = 4$. In this case the lowest power consumption is obtained by a 2nd-order single-loop ΣΔM with *M=512*, but this arquitecture has been discarded for several practical reasons: a less relaxed design of building blocks and switching noise coming from the digital part.

Table 1: Outcome of the ΣΔM architecture selection

ΣΔM Gain, ξ	Order (L)[a]	Oversampling Ratio (M)	Estimated Power Consumption (mW)
0.5	3	128	6.77
	3	256	8.12
	4	128	8.27
1	3	128	8.48
	3	256	9.77
	4	128	10.32
2	3	128	12.69
	3	256	13.85
	2	512	13.88
4	2	512	23.24
	3	128	24.21
	3	256	25.02

a. All ΣΔMs in this table are cascade architectures except for $L = 2$.

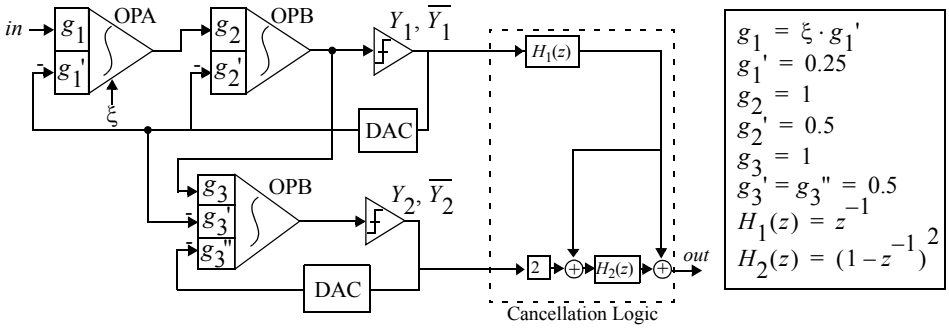


Fig.2: Conceptual block diagram of the programmable-gain 2-1 cascade SC ΣΔM.

Fig. 3 shows the fully differential SC schematic of the selected ΣΔM architecture. The first stage of the modulator includes two SC integrators – both of them with two differential input branches –, and switches controlled by the comparator output are employed to feed the quantized signal back. Note that in the first integrator one of input branches is for the input signal, in which double sampling is used to achieve an extra signal gain of 2, without increasing circuit noise [5]. The second branch receives the Digital-to-Analog Converter (DAC) outputs. Making use of the spare connection of the second branch, an external DC signal (V_{off}) can be applied during ϕ_1 to center the sensor signal in the modulator full-scale range, doing unnecessary a third branch for offset compensation with the subsequent thermal noise saving.

The second stage of the modulator incorporates an integrator with only two input branches, although three different weights are implemented – g_3, g_3', and g_3'' (see Fig. 2). This can be done because the selection of weights in the designed modulator allows the distribution of weight $g_3 = 1$ between the two integrator branches $g_3' = 0.5$ and $g_3'' = 0.5$.

The modulator operation is controlled by two non-overlapped clock-phases. The integrators input signals are sampled during phase ϕ_1. During phase ϕ_2 the algebraic operations are performed and results are accumulated in the feedback capacitor of each integrator. In order to attenuate the signal-dependent clock-feedthrough, delayed versions of the two phases – ϕ_{1d} and ϕ_{2d} – are also provided. As illustrated in Fig. 3, this delay is incorporated only to the falling edges of the clock-phases – i.e., to the turn-off of the switches –, while the rising edges are synchronized in order to increase the effective time-slot for the modulator operations [7]. The comparators are activated at the end of phase ϕ_2 – using $\overline{\phi_{2d}}$ as a strobe signal – to avoid any possible interference due to the transient response of the integrators outputs in the beginning of the sampling phase. This timing guarantees a single delay per clock-cycle. In addition to the master clock phases, ϕ_1 and ϕ_2, additional phases are required to control the chopper switches used in the first integrator to attenuate flicker noise. These chopper phases are controled by a master clock with a programmable frequency.

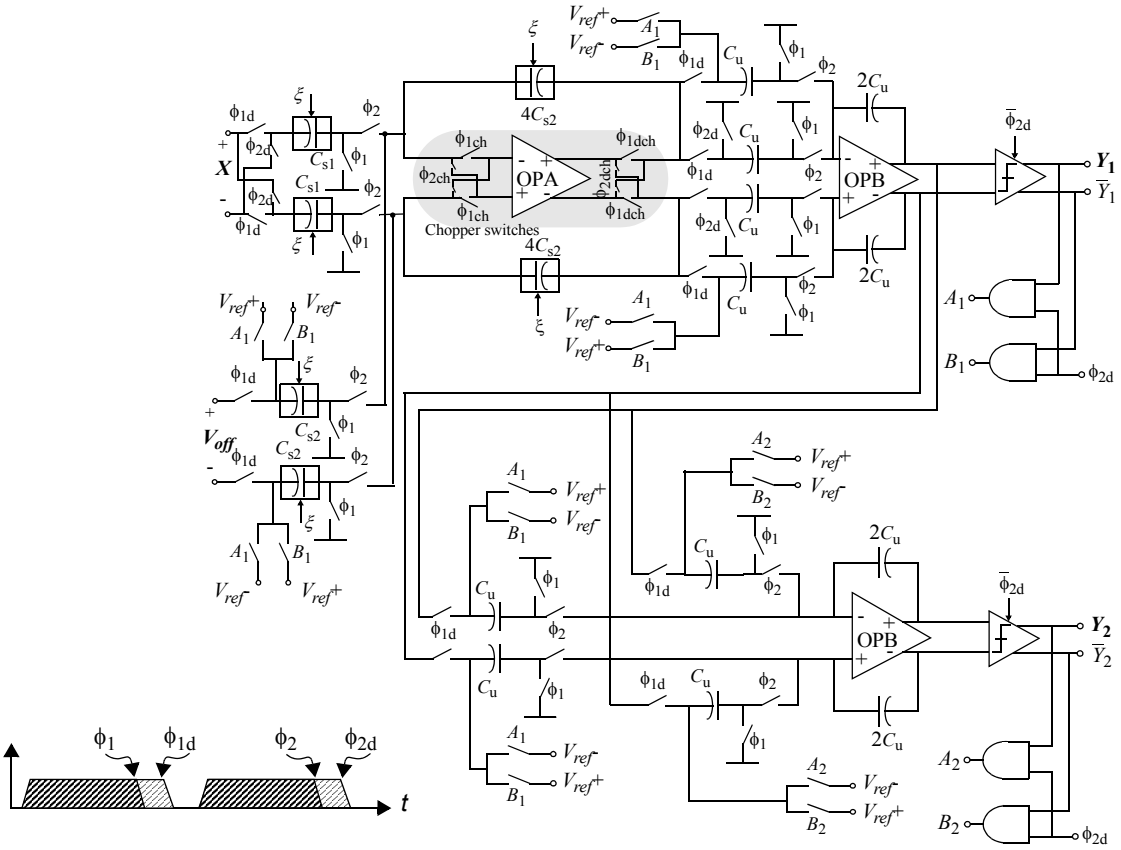


Fig.3: SC fully differential schematic of the 2-1cascade SC ΣΔM in this paper.

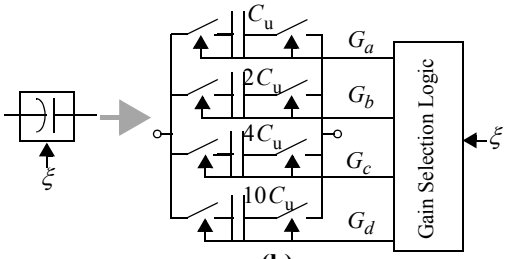
The programmable gain (ξ = 0.5, 1, 2 and 4) has been mapped onto switchable capacitor arrays, each of them formed by a variable number of unitary capacitors (C_{11}=1.5pF) as shown in Fig. 4. Such numbers are selected for minimum power dissipation, bearing in mind the circuit noise limitation and the highest temperature required for this sensor interface (*+175ºC*). In order to keep the amplifier dynamic requirements as relaxed as possible for all cases of the modulator gain, we propose to switch the number of unitary capacitors forming all the capacitances involved – not only the ones forming the sampling capacitors.

The ΣΔM in Fig. 3 has been high-level sized, i.e, the modulator specifications have been mapped onto building-block specifications using statistical optimization for design parameter selection, and compiled equations (capturing non-ideal building block behavior) for evaluation. This process is fine-tuned by behavioral simulation using an updated version of ASIDES, an advanced behavioral simulator of SC ΣΔMs [8]. At this step, non-idealities are covered more accurately than in the case of using compiled equations. Also, worst cases for speed (the largest capacitor values) and for thermal noise (the highest temperature and the lowest capacitor values) are contemplated.

The outcome of this sizing process is summarized in Table 2, where OPA denotes the opamp used at the first integrator in the chain and OPB refers to the opamps used at the second- and third- integrator in the modulator chain (see Fig. 3). The data in Table 2 define the specifications of the building blocks, which are the starting point for block sizing described in Section 3.

ξ	C_{s1}	C_{s2}	C_o	G_a	G_b	G_c	G_d
0.5	C_u	$4C_u$	$16C_u$	1	0	0	0
1	$2C_u$	$4C_u$	$16C_u$	0	1	0	0
2	$6C_u$	$6C_u$	$24C_u$	0	1	1	0
4	$16C_u$	$8C_u$	$32C_u$	0	1	1	1

(a)



(b)

Fig.4: Programmable capacitors in the first integrator. (a) Capacitor arrays. (b) C_{s1} implementation.

Table 2: High-level sizing of the programmable-gain 2-1 ΣΔM

SPECS: 110-dB@40kS/s@2V_p			Value	Unit
INTEGRATORS	Integration capacitor	Gain 0.5	24	pF
		Gain 1	24	pF
		Gain 2	36	pF
		Gain 4	48	pF
	Unitary capacitor		1.5	pF
	Sigma		0.1	%
	Capacitor non-linearity		25	ppm/V^2
	Bottom parasitic capacitor		5	%
	Switch ON-resistance		<650	Ω
OPAMPS	DC-gain	OPA	68	dB
		OPB	63	dB
	DC-gain non-linearity		15%	V^{-2}
	GBW	OPA (44.2pF load)	17	MHz
		OPB (8.9pF load)	15	MHz
	Slew-rate	OPA (44.2pF load)	17	V/μs
		OPB (8.9pF load)	28	V/μs
	Output swing		±2.5	V
COMPARATORS	(Hysteresis + Offset) (max.)		30	mV
	Resolution time		50	ns

3. DESIGN OF THE BUILDING BLOCKS

The modulator building blocks, namely, amplifiers, comparators, switches and capacitors have been conveniently selected and sized according to the requirements given in Table 2. Design considerations on each of these blocks as well as their electrical performance using HSPICE are detailed in this section.

3.1 Amplifiers

The key features for the design of the amplifiers are their open-loop DC-gain, dynamic requirements and output swing, where the last one becomes especially critical in a low voltage implementation. Nevertheless, the set of integrator weight used for the ΣΔM in Fig. 3 allow us to relax the output swing requirements to be slightly larger than the reference voltages – 2V in this case –, which is feasible when operating with 3.3V supply in differential mode.

Table 2 shows that the OPA has more demanding requirements than the OPB, the reason being that the contribution of the latter to the total in-band error power is attenuated by increasing powers of the oversampling ratio. Thus, to reduce power consumption, they should be considered as different items to design purposes. To achieve this goal an improved version of the transistor-level sizing tool FRIDGE [8] was used to explore the potentials of a wide catalog of fully differential OTA topologies. At the outcome, a single-stage folded-cascode architecture, shown in Fig. 5, was selected as the optimum choice for both amplifiers. N-channel input transistors were employed to take advantage of the twin-well technology feature in removing the body effect of NMOS transistors. The Common-Mode Feed-Back (CMFB) net has been implemented using a SC circuit, which provides fast, linear operation with small power dissipation.

Table 3 shows the full sizing and biasing of OPA and OPB, by indicating the multiplicity factor for each transistor. Table 4 summarizes the electrical performance of both amplifiers regarding the target values imposed during the FRIDGE optimization procedure. Parameter values in this table, obtained by electrical simulations using HSPICE, are shown for typical conditions (typical process parameters, nominal supply voltage and room temperature) as well as for worst-cases

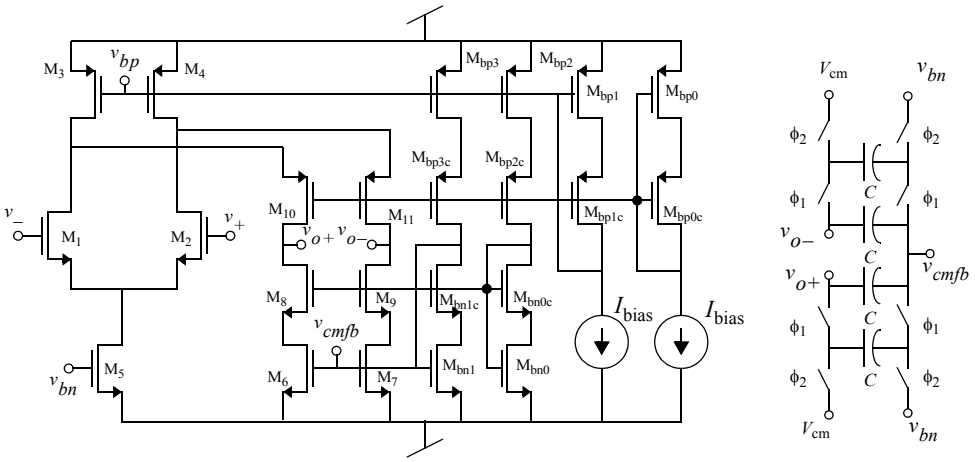


Fig.5: Fully differential folded-cascode amplifier used in the ΣΔ modulator.

Table 4: Electrical performance of the opamps (HSPICE)

	OPA (45pF load)		OPB(9pF load)	
Model	Typical	Worst-Case	Typical	Worst-Case
DC-gain (dB)	74.0	71.09	68.3	68.3
GB (MHz)	22.6	15.8	34.4	23.8
Phase Margin (º)	86.4	85.5	83.5	81.4
Slew-Rate (V/μs)	22.1	21.1	38.1	35.7
Output Swing (V)	±2.75	±2.5	±2.75	±2.5
Transc. (mA/V)	6.3	4.5	1.95	1.35
Power consumption (mW)	7.1	7.2	2.3	2.4

in a corner analysis – considering fast and slow device models, ±10% variation in the 3.3V supply, and temperatures in the range ([-40ºC,+175ºC]).

The amplifier nonlinear features (mainly nonlinear DC gain and dynamics) deserve special attention in a high-linear implementation. When the amplifier output swings, the drain-to-source voltage of the output transistors changes, and so does the output impedance. This effect, illustrated in Fig. 6 for the OPA and OPB in the nominal conditions, translates into a dependence of the open-loop DC gain on the output voltage, so that the DC gain reaches its maximum at the central point and decreases as the output approaches the rails. Such a non-linearity is traditionally modeled by second-order polynomial dependence of the gain of the output voltage 6, but this is only valid for small voltage excursions around the central point. On the contrary, in the proposed 3.3-V implementation, it is expected that small-gain regions of the DC curve (shadowed areas in Fig. 6) are often visited during normal operation of the modulator. In order to accurately account for this nonlinearity in behavioral simulations, we have resorted to table look-up procedure from amplifier DC curves obtained by electrical simulation. A similar approach has been employed for validating the actual transient response of the front-end integrator.

3.2 Comparators

The specifications for the single-bit quantizers – comparators – at the end of the first and second stages of the modulator are given in Table 2. Among them, a low resolution time around 50ns and a hysteresis lower than 30mV can be pointed up. In order to cope with these specifications, a regenerative latch including a pre-amplifying stage was selected for the comparator [9].

Fig. 7 shows the selected topology of the comparator. It consists of a NMOS differential input pair ($M_{1\text{-}2}$), a CMOS regenerative latch circuit and a RS flip-flop. The latch circuit is composed of a NMOS flip-flop ($M_{3\text{-}4}$) with a pair of

Table 3: Sizing and biasing of the opamps

SIZES		
Transistor	OPA (μm/μm)	OPB (μm/μm)
$M_{1,2}$	5x(40/0.5)	2x(25/0.5)
$M_{3,4}$	8x(65.6/0.5)	8x(25.5/0.5)
M_5	8x(42.5/0.5)	8x(10.7/0.5)
$M_{6,7}$	5x(32/0.5)	5x(8/05)
$M_{8,9}$	8x(31.05/0.6)	8x(5.65/0.45)
$M_{10,11}$	8x(64/0.5)	8x(30.20/0.45)
M_{bp0}	8.85/0.5	4/0.5
$M_{bp1,2,3}$	65.6/0.5	25.5/0.5
$M_{bpc0,1,2,3}$	64/0.5	30.20/0.45
M_{bn0}	4.45/0.5	1.9/0.5
M_{bn1}	42.5/0.5	10.7/0.5
$M_{bnc1,2}$	31.05/0.6	5.65/0.45
Biasing		
I_{bias} (μA)	110	36.7

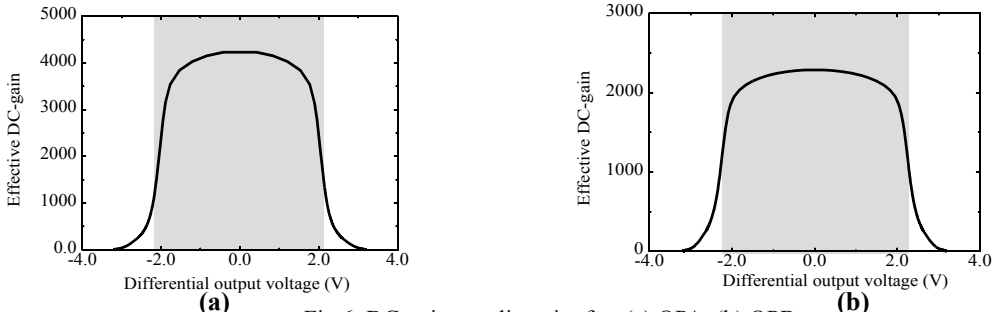


Fig.6: DC-gain non-linearity for: (a) OPA, (b) OPB.

NMOS switches ($M_{9\text{-}10}$) for strobing and a NMOS switch (M_{17}) for resetting, and a PMOS flip-flop ($M_{5\text{-}6}$) with a pair of PMOS precharge switches ($M_{7\text{-}8}$).

The comparator is activated at the end of the integration phase, solving the difference of the integrators outputs. At the beginning of the next integration phase, the outputs of the latch are forced to the low state and the RS flip-flop maintains the comparator output until the next strobbing of the latch. As shown in Fig. 7, different voltage supplies have been used for the pre-amplifier and for the regenerative latch – V_{DDAA} and V_{DDAD}, respectively. This has been done in order to reduce the comparator sensitivity to injected digital switching noise and supply bounce effects.

The circuit in Fig. 7 has been designed according to the required high-level specifications, while the input capacitance and the power consumption should be kept as low as possible. Table 5 shows the sizes of the transistors and the value of the bias current.

Multiple MonteCarlo simulations and corner analysis have been done for characterizing the comparator performance during its full sizing. Table 6 summarizes the electrical performance, showing the worst-cases for hysteresis, offset and resolution time together with the power dissipation. As expected, the resolution is dominated by mismatching, the offset being the dominant limitation factor with a worst-case value of 9.92mV – according to the specifications given in Table 2.

3.3 Switches

The main design issue of switches is their finite switch on-resistance, R_{on}, which is mainly constricted by dynamic considerations. Incomplete settling originated by transmission gates is traditionally reduced by making $R_{on}C_{s1}f_S \ll 1$. In our design, it was previously evaluated (see Table 2) that R_{on} in the range of 650Ω can be tolerated with no degradation of

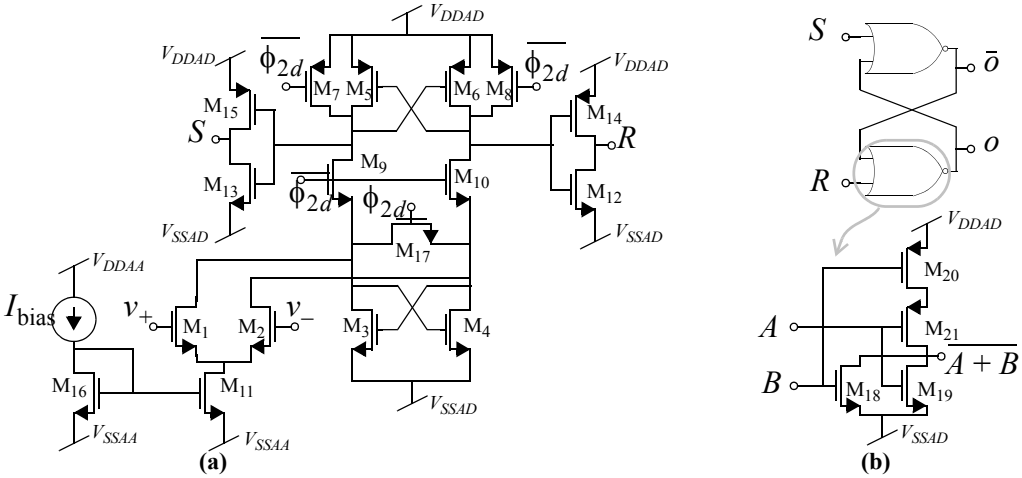


Fig.7: Schematic of the comparator. a) Preamplifier + latch. b) RS flip-flop.

Table 5: Sizing and biasing of the comparators

MOST	W/L (μm/μm)
$M_{1,2}$	20/0.5
$M_{3,4}$	4/2
$M_{5,6}$	16/2
$M_{7\text{-}10,12\text{-}15,17}$	1.5/0.35
$M_{11,16}$	8/1
M_{18}	6.3/0.35
M_{19}	4.2/0.35
$M_{20,21}$	11.9/0.35
I_{bias}	55μA

Table 6: Electrical performance of the comparators (HSPICE)

Parameter	Typical	Worst-case
Offset (mV)	0.75	9.92
Hysteresis (mV)	0.03	0.12
Resol. time, T_{RLH} (ns)	4.1	8.6
Resol. time, T_{RHL} (ns)	3.9	6.15
Power Consumption (mW)	0.43	

the modulator performance. In our technology process, this value can be obtained using CMOS switches with aspect ratios of 6.5/0.35 for the NMOS transistor and 23.5/0.35 for the PMOS, operating with the nominal 3.3-V supply.

However, in low-voltage technologies, given that the threshold voltage of the MOS transistors is not scaled down in the same amount as the supply voltage, the voltage range in which R_{on} keeps a nearly constant value decreases. This is illustrated in Fig. 8 by showing the R_{on} of several CMOS switches as a function of the signal level. The sampling process with such an on-resistance causes dynamic distortion [10] – the more evident the larger the sampling capacitor and the signal frequency.

In sensor interfaces, high-linearity is a must. Therefore, the non-linear sampling effect in the first integrator (which is the block that samples the signal in our system) has to be carefully taken into account, especially in the case of $\xi = 4$, in which C_{s1}=24pF. In this case the CMOS switch size given above causes harmonic distortion which can severally degrade the performance of the sensor interface. However, resorting to larger aspect ratios to solve this problem increases parasitics and power dissipation, whereas including clock-bootstrapping strategies [11] increases complexity and leads to a less robust design.

For this reason, the sampling process in the first SC integrator in Fig. 9(a), has been extensively studied using the sampling circuit in Fig. 9(b). Electrical simulations have been done using corner analysis for a 0dBV@20kHz sine-wave input signal, obtaining that the worst value of the Total Harmonic Distortion (THD) generated by the analog switches is -100dB, which agrees with required specifications. This implies that the sizing used for the CMOS switches –aspect ratios of 29.1/0.35 for the NMOS transistor and 105.9/0.35 for the PMOS– ensures a distortion low enough for the present application, and suggest that clock-boosting or similar techniques are not required in the technology used.

3.4 Capacitor arrays

Capacitors have been implemented using the M-i-M structures available in our technology process. Using this topology, the 1.5-pF unitary capacitor is required to make the integrator weights is approximately 31.6 μm x 31.6 μm size. The estimated mismatch for this capacitor is $\sigma(\Delta C/C) = 0.1\%$. As mismatch error is one of the most important limiting

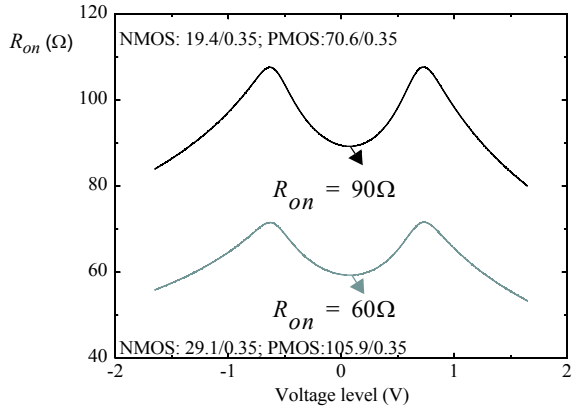


Fig.8: DC characteristic of several analog CMOS switches.

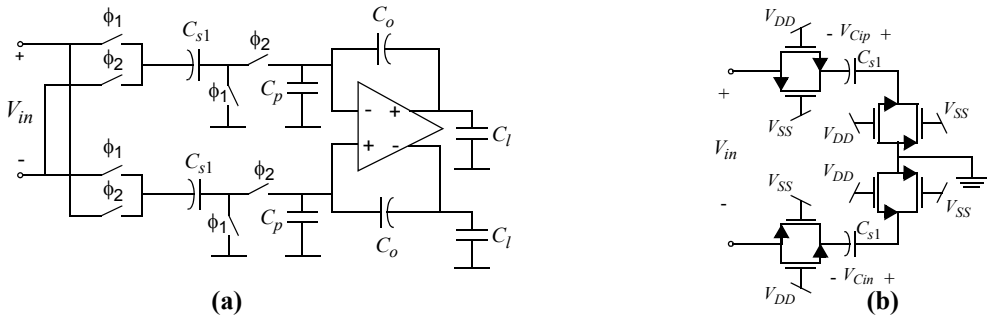


Fig.9: Analog switches: (a) fully differential SC integrator, (b) Circuit under evaluation.

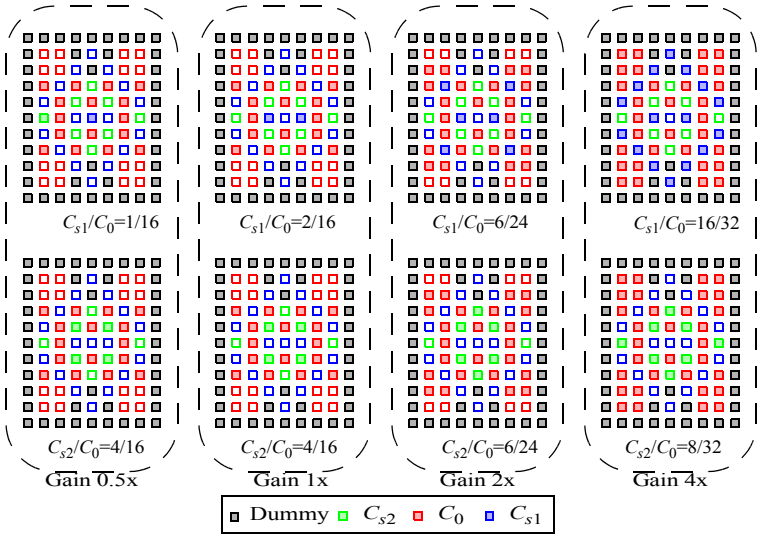


Fig.10: Conceptual layout of programmable capacitor array of the fiont-end integrator.

factors in cascade architectures, common centroid structures have been used in the layout. In the case of the first integrator, all the capacitors (C_{s1}, C_{s2} and C_O in Fig. 3) are made up of unitary capacitors which are connected or disconnected depending on the case of the modulator gain (see Fig. 4). In this case a programmable common-centroid structure, symbolically shown in Fig. 10, has been used while the matching of weights g_2', g_3', g_3'', is just based on closely placed capacitors.

3.5 Auxiliary blocks

In addition to the building blocks described in previous subsections, there are other on-chip auxiliary blocks required in practice for the implementation of the programmable-gain ΣΔ modulator, namely: clock-phase generator, master-bias current generator and gain-selection logic. These blocks will not describe in this paper.

4. EXPERIMENTAL RESULTS

The modulator has been designed and fabricated in a single-poly, five-metal, 0.35μm CMOS technology. The complete modulator occupies an area of 5.7mm^2 (pads included) and dissipates 14.7mW from a single 3.3-V supply. The chip is encapsulated in 64-pin plastic quad flat package. Double-bonding techniques and multiple pins are used for the power supplies in order to reduce supply bounce.

The circuit has been tested using a PCB that includes intensive filtering and decoupling strategies, as well as proper impedance termination to avoid reflections of high-frequency signals. The performance of the modulator was evaluated using a high-resolution (-100dB THD) sinusoidal source to generate the input signal and a digital data acquisition unit to generate the clock signal and to acquire the bit streams of the first and second stages of the ΣΔM. The same unit controlled the supply and reference voltages. After the acquisition, performed automatically by controlling the test set-up through proprietary C routines, data were transferred to a workstation to perform the digital postprocessing using MATLAB. The digital filtering was performed with a *Sinc* filter, implemented by software.

Fig. 11 shows a measured 65536-point Kaiser-windowed fast Fourier transform (FFT) of the modulator output, clocked at 5MHz and considering a -12dBV, 5kHz input sinewave, a modulator gain of ($\xi = 1$) and a chopper frequency equal to $f_{ch}=f_s/2$. The effect of varying the chopper frequency is illustrated in Fig. 12(a) by showing several output spectra corresponding to $f_{ch} = f_s/16, f_s/4, f_s/2$. Note that, the lower f_{ch} the more flicker noise appears in the signal bandwidth, thus degrading the modulator performance. This is better illustrated in Fig. 12(b) where the Signal-to-(Noise+Distortion) Ratio (SNDR) vs. signal amplitude is represented for $\xi = 1$ and different cases of f_{ch}. It can be noted that the best performance is achieved when $f_{ch}=f_s/2$. For that reason, in the following, all measurements will be given for this value of f_{ch}.

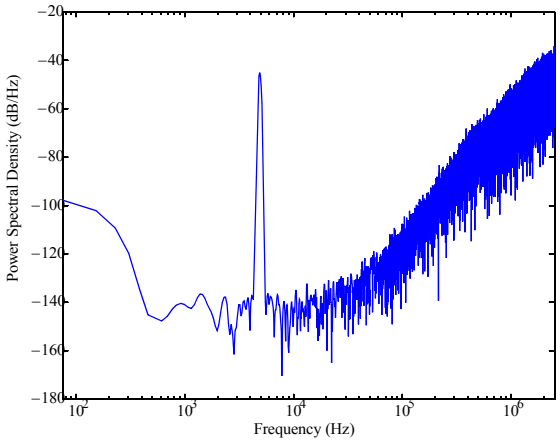


Fig.11: Measured modulator output spectrum for a −12-dBV@5-kHz input signal, $\xi = 1$ and $f_{ch} = f_s/2$.

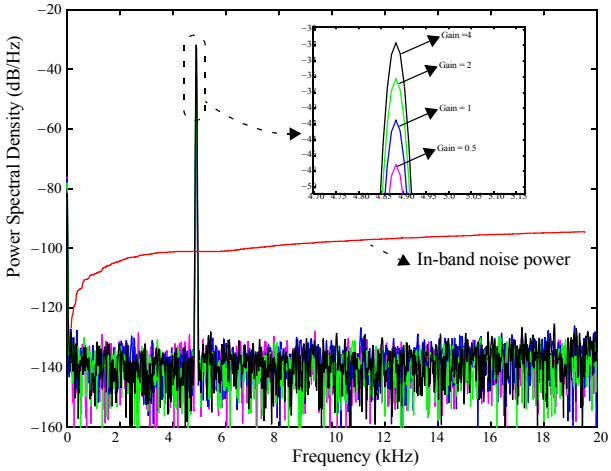
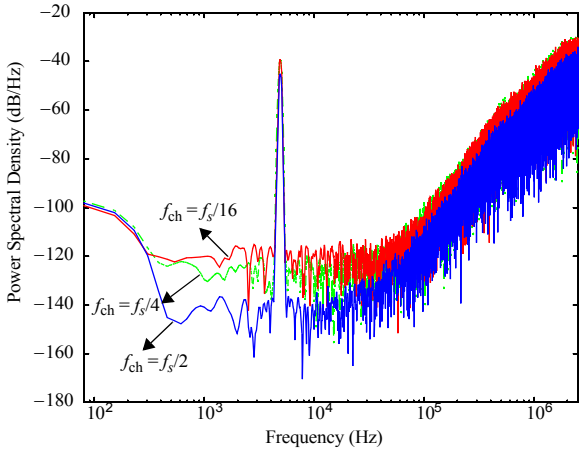
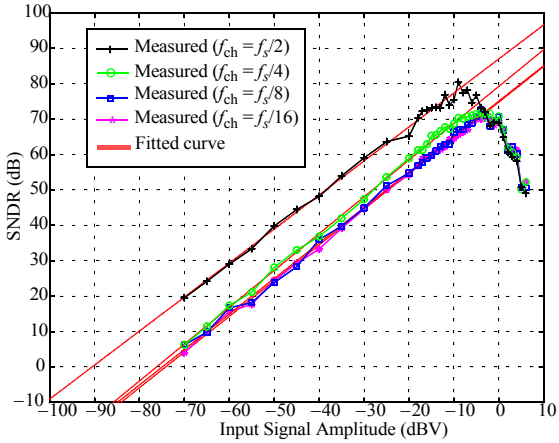


Fig.13: Measured modulator in-band (20-kHz) spectra corresponding to different gain cases.



(a)



(b)

Fig.12: Effect of chopper frequency on measured results: (a) Output spectra and (b) SNDR vs. signal amplitude.

Fig. 13 shows several in-band (20-kHz) output spectra corresponding to the four different cases of the modulator gain ($\xi = 0.5,1,2,4$) when a -20dBV@5kHz input signal is applied. The in-band spectrum shows a performance very similar to the expected simulated output spectra. Indeed, the in-band noise power is about -96dB, corresponding to almost 16-bit resolution. This resolution can be notably improved by the effect of the modulator gain. This is illustrated in Fig. 14 where the measured Signal-to-Noise Ratio (SNR) and SNDR are represented against the input amplitude. The input-referred DR is approximately 104dBV, i.e 110dB below FS (dBFS) reference voltage ($V_{ref}=2V$).

Note from Fig. 14 that in most cases of the modulator gain, the SNR/SNDR-peak is reached at approximately 10-dBFS signal amplitudes. Indeed, the in-band noise power increases at those amplitudes as illustrated in Fig. 15. Behavioral simulations reveal that this non-linear phenomenon is due to an incorrect operation of the chopper circuitry that seems to be caused by the effect of dielectric relaxation in the M-i-M capacitors of the first integrator [12]. This effect, normally not properly characterized in most technology processes, may lead to an underestimation of the in-band noise power during the design process, specially in high-resolution ADCs. Indeed, reducing the reference voltage from 2V (nominal) to 1V, the SNR-peak improves in approximately ~5dB for all cases of the modulator gain as illustrated in Fig. 16.

The noise-shaping degradation is more severe at the edge of the signal bandwidth as illustrated in Fig. 11 and Fig. 13. Therefore, the performance near FS might be improved if a smaller signal-bandwidth is taken. This is shown in Fig. 17 by plotting the SNR vs. input signal amplitude for different cases of the modulator gain and reference voltages. Note that, in

addition to the obvious resolution improvement due to doubling the oversampling ratio, the modulator behavior near FS is better than in Fig. 23.

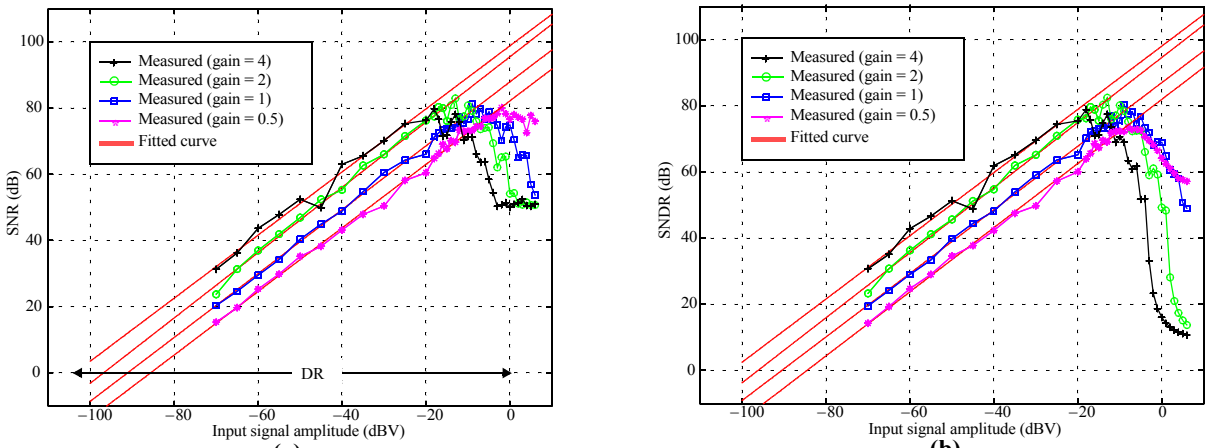


Fig.14: (a) SNR and (b) SNDR as a function of the signal amplitude for different cases of the modulator gain.

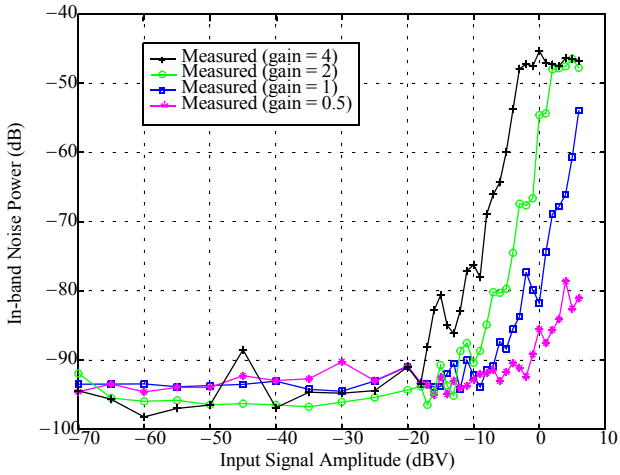


Fig.15: In-band noise power as a function of the input signal amplitude.

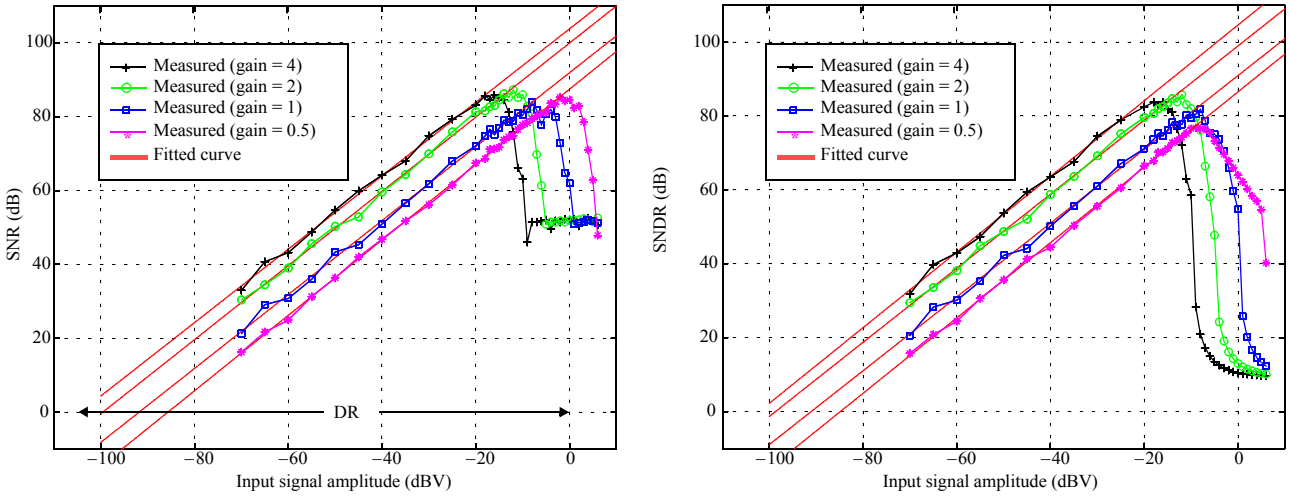


Fig.16: (a) SNR and (b) SNDR as a function of the signal amplitude for V_{ref}=1V.

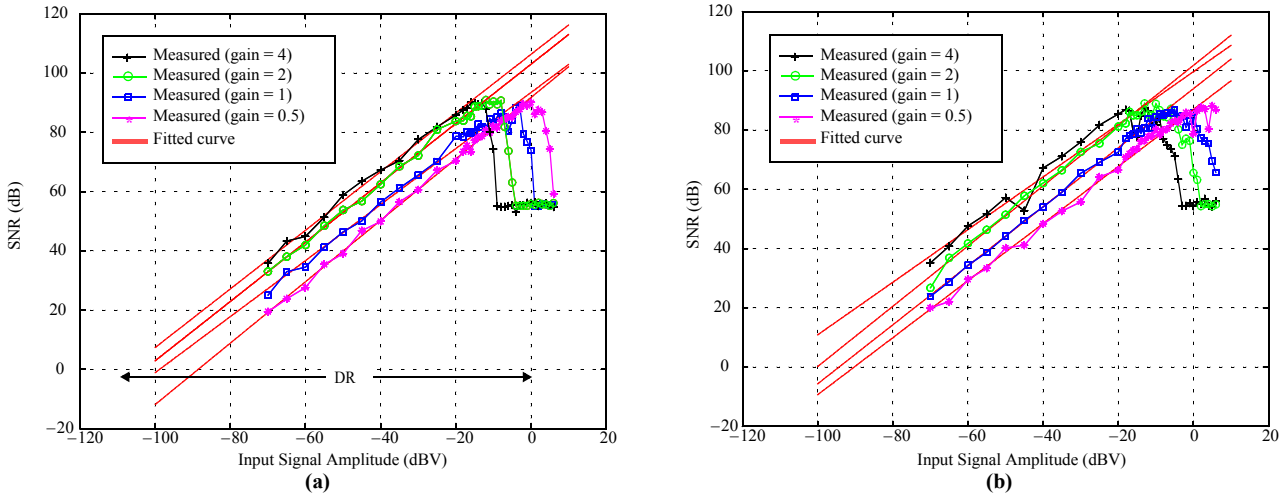


Fig.17: SNR vs. signal amplitude for 10-kHz bandwidth. (a) V_{ref}=1V (b) V_{ref}=2V.

5. CONCLUSIONS

A 0.35µm CMOS programmable-gain cascade 2-1 ΣΔM forming part of an automotive sensor interface has been described. Main design considerations have been discussed and applied to select the most appropriate modulator architecture in terms of resolution, speed and power consumption. The circuit has been designed based upon a top-down CAD methodology that combines simulation and statistical optimization at different levels of the modulator hierarchy. Experimental results show that the dynamic range can be highly enhanced by the action of gain programmability. This combined effect places the presented chip at the edge of the state-of-the-art ΣΔMs.

6. REFERENCES

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