A Sub-μW Reconfigurable Front-End for Invasive Neural Recording

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***Abstract*—This paper presents a sub-μW ac-coupled reconfigurable front-end for the purpose of neural recording. The proposed topology embeds in it filtering capabilities allowing it to select among different frequency bands inside the neural signal spectrum. Power consumption is optimized by designing for bandwidth-specific noise targets that take into account the spectral characteristics of the input signal as well as the noise bandwidths of the noise generators in the circuit itself. An experimentally verified prototype designed in a 180 nm CMOS process draws a maximum of 815 nW from a 1 V source. The measured input-referred spot-noise at 500 Hz is 75 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ while the integrated noise in the 200 Hz - 5 kHz band is 4.1 $\mu\mathrm{Vrms}$.**

***Index Terms*—neural front-end, neural recording, ultra-low power, reconfigurable.**

I. Introduction

Observing brain signals at the cortical level has become a fundamental tool for a number of tasks ranging from basic neuroscience research to brain-machine interfaces. This procedure is normally performed by a multichannel sensing front-end in contact with an array of penetrating electrodes. This scheme offers the highest temporal and spatial resolution out of any other implantable solution [1]. The available extracellular signals at the cortical level are the action potential (AP) and the local field potential (LFP). The AP is a high-frequency (200 Hz - 5 kHz) signal that reflects the dynamics of a single neuron while the low-frequency (1 Hz - 500 Hz) LFP encodes the activity of a group of them. Usually, an offset-rejecting front-end amplifier designed for low-noise and high-gain acquires both signals (i.e. the entire neural bandwidth) per-channel. In addition, many applications necessitate spectral selectivity, which is normally done by subsequent filter stages either in the digital or analog domain. Considering that these specifications have to be met in a context of low-power availability and that the density of recording channels is increasing, it is no surprise that this is an open research problem. Neural front-ends generally consume above 2 μW/channel [2]–[4] while those that implement some form of spectral selectivity consume at least two-times that [5]–[7]. In this work we employ a two-fold strategy for power reduction: first, instead of including additional filters, filtering capabilities are embedded in the front-end. This is made possible by implementing a reconfigurable topology. Second, instead of defining an integrated noise target for the entire neural bandwidth, we determine signal-specific noise targets. This eludes any tendency to overdesign and translates directly to power savings.

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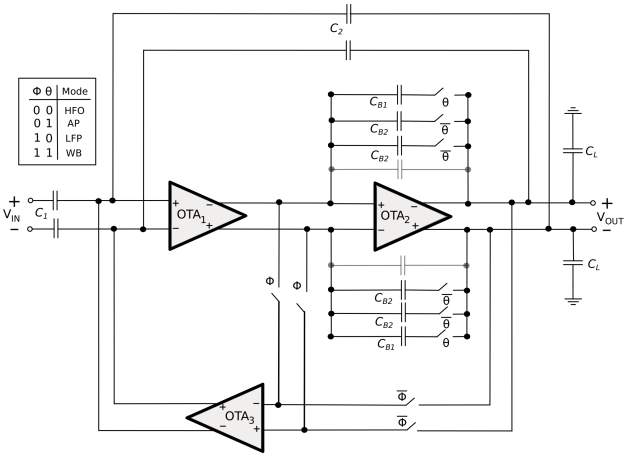

Fig. 1. Proposed reconfigurable front-end.

II. Proposed reconfigurable front-end

Figure 1 shows the proposed capacitively-coupled neural amplifier with reconfigurable topology. The idea is that four different circuit configurations, each with its own frequency bandwidth, can be accessed through digitally-controlled switching. Thus, each circuit configuration is tuned to a specific frequency band without heavily impacting the power consumption. The configuration modes are named after the bandwidth they are set to: wideband (WB), LFP, AP and high-frequency oscillations (HFO) [8]. The gain for all modes of operation is $\mathrm{C}_1/\mathrm{C}_2$. The reconfigurable modes are as follows.

A. Wideband Mode

The circuit enters the WB mode that covers both the local field and action potential frequency bands (Fig. 2(a)) at $\phi = 1$ and $\theta = 1$. The low-frequency corner is given by:

$$f_{L(WB)} \simeq \frac{gm_3}{2\pi C_2 A_2}. \quad (1)$$

Here, $\mathrm{A}_2 = \mathrm{gm}_2/\mathrm{gds}_2$ while gm_2 and gds_2 are the transconductance and conductance of OTA_2, respectively. gm_3 is the

transconductance of OTA_3. The high-frequency corner is:

$$f_{H(WB)} \simeq \frac{gm_1}{2\pi C_{B1}}, \tag{2}$$

where gm_1 is the transconductance of OTA_1.

B. Local Field Potential Mode

The LFP mode of operation is accessed at $\phi = 1$ and $\theta = 0$ (Fig. 2(b)). The low-frequency corner is the same as the WB mode. The high-frequency corner is given by:

$$f_{H(LFP)} \simeq \frac{gm_1}{2\pi C_{B2}}. \tag{3}$$

Thus, the bandwidth is reduced considering $\mathrm{C_{B2}} > \mathrm{C_{B1}}$.

C. Action Potential Mode

The AP mode (Fig. 2(c)) reconfigures the feedback of the circuit at $\phi = 0$ and $\theta = 1$ meaning that OTA_3 connects to the output of OTA_2. This has the following effect on the low-frequency corner:

$$f_{L(AP)} \simeq \frac{gm_3}{2\pi C_2}. \tag{4}$$

Equation (4) shows that by discarding A_2, $f_{L(AP)}$ is boosted to a higher frequency. The high-frequency corner is described by (2) as well since $\mathrm{C_{B1}}$ is set as the feedback capacitor.

D. High-Frequency Oscillations Mode

The amplifier enters HFO mode (Fig. 2(d)) at $\phi = 0$ and $\theta = 0$. The bandwidth is set by a combination of the AP low-frequency corner and the LFP high-frequency corner. The low-frequency corner is thus described by (4) while (3) describes the high-frequency corner.

III. Input Signal Aware Noise Optimization

The conventional design strategy is to set the noise of the amplifier ($\overline{v_{ni}^2}$) through the control of the thermal noise of the largest overall contributor (OTA_1) by way of gm_1 as follows,

$$\overline{v_{ni,th,OTA_1}^2} = \frac{4kT}{gm_1}\Delta f, \tag{5}$$

where k is the Boltzmann constant and T is the temperature. This method leads a fortiori to increased power consumption since gm_1 has to compensate for other low-frequency noise contributions of which it has no influence on (Fig. 3(a)):

$$\overline{v_{ni}^2} = \overline{v_{ni,th,OTA_1}^2} + \overline{v_{ni,1/f,OTA_1}^2} + \overline{v_{ni,th,OTA_3}^2}. \tag{6}$$

The proposed noise optimization strategy takes into account the characteristics of the input signal in order to generate power-efficient noise targets. The point is that the amplitude of the wideband neural signal is not uniform [9] [10]: the LFP band shows a $1/f^x$ magnitude decay while the AP remains flat (Fig. 3(b)). The neural signal at low-frequencies exhibits milivolts-order amplitudes while higher frequency amplitudes are in the microvolt order of magnitude. Thus, the signal to noise ratio (SNR) is larger at lower frequencies. An accurate

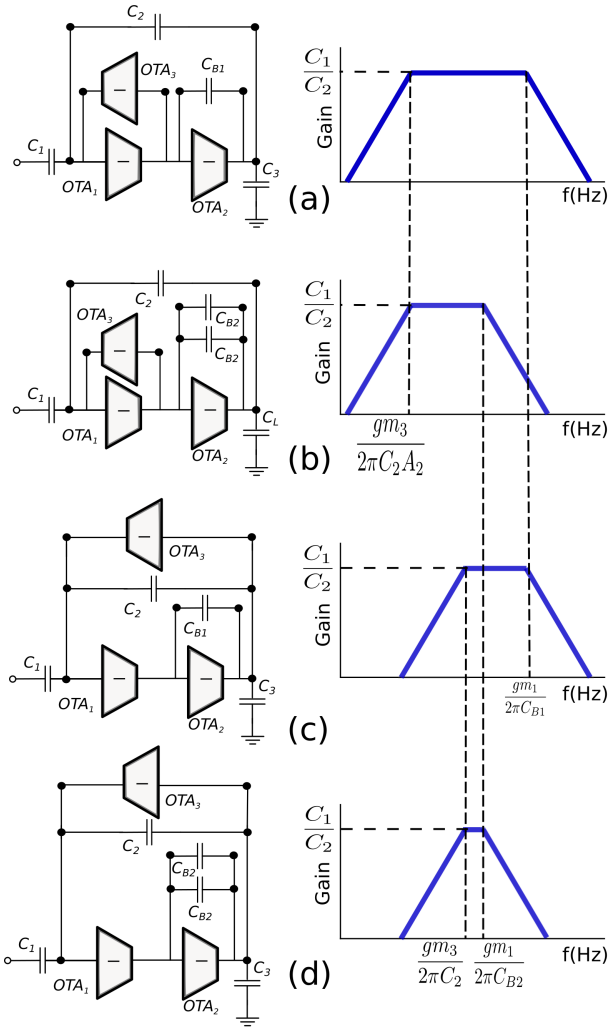

Fig. 2. Reconfigurable Modes. (a) Wideband mode (b) Local field potential mode (c) Action potential mode (d) HFO mode.

recording can be guaranteed if we ignore the low-frequency noise contributions and select a spot-noise target at the worst-case SNR (measured around 500 Hz by [11]) for the WB and LFP modes. An input referred spot-noise of 80 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ guarantees sufficient SNR for amplitudes as low as 20 μV. The proposed spot-noise target is reached mostly by gm_1 since there is less low-frequency noise impact at 500 Hz. This strategy saves significant amounts of power since gm_1 is set by the largest bias current in the front-end. Meanwhile, the noise target for the AP mode remains the same (i.e. the usual <5 μVrms [2]) and is fully controlled by gm_1.

IV. Transistor Level Implementation

Current reuse amplifiers biased in weak inversion were used for OTA_1 and OTA_2 (Fig. 4(a)). These OTAs generate the transconductance of a complementary input pair from half the current as they are biased by the same source. The design starts by biasing OTA_1 to meet the spot noise target. Flicker noise introduced by OTA_1 can be minimized by increasing the transistor pair area up to a certain point (i.e.

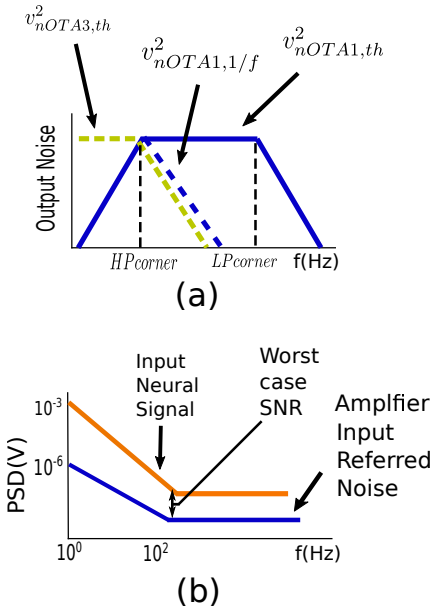

Fig. 3. (a) Noise bandwidths of the proposed front-end for the WB mode. (b) PSD of a typical front-end noise and input signal.

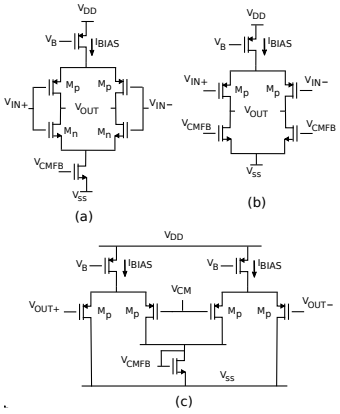

Fig. 4. a) OTA_1 and OTA_2. b) OTA_3. c) Common-mode feedback.

area specifications). The bandwidth of the amplifier is set by C_{B1} or C_{B2} . Total power consumption is kept low by biasing OTA_2 with the least amount of current possible while keeping stability and high enough open-loop gain. Its impact on (1) should also be considered. Amplifier OTA_3 (Fig. 4(b)) is biased with an extremely small picoampere current in order to set f_L=1 Hz in the WB and LFP modes. The common-mode feedback circuit used for every OTA is shown in Fig. 4(c). The sizing of C_1/C_2 should consider the gain target (40 dB) and its impact on area and input impedance.

V. Benchtop Testing

Results from experimental verification (Fig 5(a)) are presented in this section. The circuit was designed in a 180 nm process (Fig 5(b)) biased by a 1 V supply. Measured power consumption was 803 nW. An additional current bias tuning in OTA_3 was included to optimize the high-pass corner. The

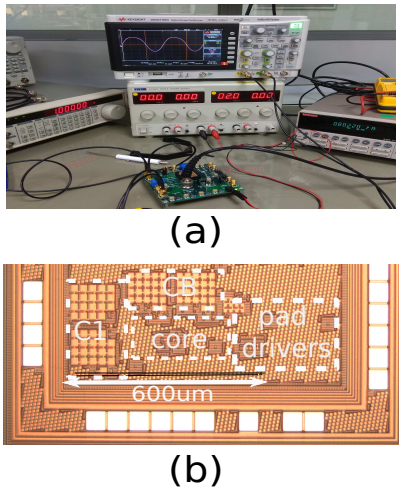

Fig. 5. a) Benchtop setup. b) Physical view.

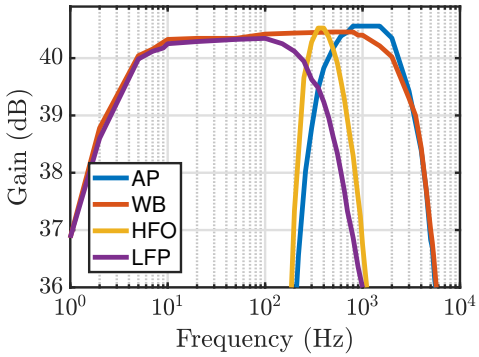

Fig. 6. Frequency Response.

four selectable bandwidths are shown in Fig. 6. The WB mode covers the 1 Hz - 5 kHz band, AP mode covers 200 Hz - 5 kHz, LFP mode 1 Hz - 700 Hz and the HFO 200 Hz - 950 Hz. The AP and HFO modes show a power consumption of 815 nW due to an increase in the current bias of OTA_3. The input-referred spot noise at 500 Hz is 75 $nV/\sqrt{Hz}$ (Fig. 7) for the WB and LFP modes while the integrated noise in the AP mode is 4.1 μVrms (Fig. 8). The measured CMRR for 100 mVpp sine inputs at 50 Hz for the LFP and WB modes was 58 dB. This test was repeated at 400 Hz and 1 kHz for the HFO and AP modes respectively yielding >68 dB CMRR in both cases. PSRR was measured by introducing a 100 mVpp sinusoid to the supply input. The measured PSRR was 54 dB for the WB and LFP modes at 50 Hz. This same test found that the PSRR for the AP and HFO modes was 64 dB at 1 kHz and 65 dB at 400 Hz, respectively. The specifications are summarized in Table I and compared with the state of the art.

VI. Conclusions

This work presented a neural front-end with a reconfigurable topology that draws a maximum of 815 nW. This power consumption is 50 % less than previously reported works with similar aim and specifications. Unlike other sub-μW neural front-ends, our low power consumption is achieved

TABLE I
PERFORMANCE SUMMARY

	[2]	[5]	[6]	[3]	[4]	This work
Process / Year	65 nm / 2017	130 nm / 2017	130 nm / 2017	180 nm / 2018	500 nm /2018	180 nm / 2018
VDD (V)	1.2	1.2	1	1.8	3.3	1
Power (μW)	2	4.7	11	4.5	28	0.803 (LFP,WB) , 0.815 (HFO,AP)
High-pass corner	0.2 Hz - 4 Hz	0.5 Hz / 300 Hz / 500 Hz / 1 kHz	20 Hz	0.7 Hz	13 Hz	1 Hz / 200 Hz
Low-pass corner	5 kHz	1 kHz / 10 kHz	15 kHz	9.3 kHz	9.8 kHz	700 Hz / 950 Hz / 5 kHz
Gain (dB)	26	34-68	44	35	49.5	40.4
Offset rejection	-	AC-coupled	-200 mV $\sim$ 100 mV	AC-coupled	$<$ 50 mV	AC-coupled
Noise	AP=7 μVrms[5] LFP=80 nV/$\sqrt{\text{Hz}}$ @ 200Hz	6.36 μVrms[2]	3.0 μVrms [3]	3.2 μVrms[4], 60 nV/$\sqrt{\text{Hz}}$	1.88 μVrms[5]	AP Mode = 4.1 μVrms 75 nV/$\sqrt{\text{Hz}}$ @ 500 Hz (Wideband)
CMRR (dB)	-	$>$60dB	-	76dB	87dB	58dB (WB,LFP), 68dB(AP,HFO)
THD	-74 dB @ 20 mVp, 1 kHz	0.4% @ 10 mVpp	0.8% @ 1mVrms, 1 kHz	0.07% @ 1mVpp	1% @ 0.7 mVpp	$<$1% @ 1mVp

integrated bandwidth: [1](300Hz-10kHz) [2](10Hz - 17kHz) [3](1 Hz -10kHz) [4](0.03Hz- 25kHz)

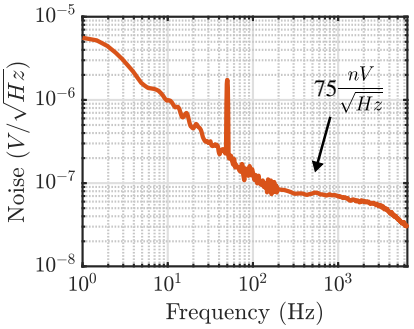

Fig. 7. Input-referred noise for the WB mode.

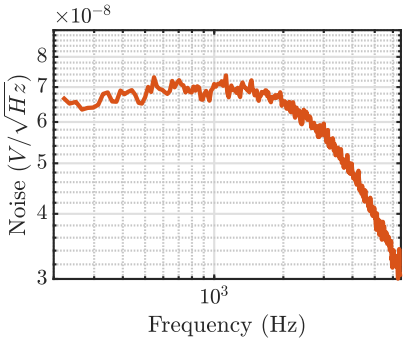

Fig. 8. Input referred noise for the AP mode.

without sacrificing input swing (through extreme voltage bias reduction), gain precision (by the use of open-loop amplifiers) and CMRR or PSRR (by employing single-ended structures). To the best of our knowledge, the use of double bandwidth-specific noise targets with the goal of reducing power consumption has not been reported previously. Future work will further the characterization of the rest of the specifications of the circuit.

ACKNOWLEDGEMENTS

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