

Transformer based front-end for a low power 2.4 GHz transceiver

Jens Masuch, Manuel Delgado-Restituto and Ángel Rodríguez-Vázquez
Institute of Microelectronics of Seville (IMSE-CNM-CSIC) - University of Seville
Email: {masuch,mandel,angel}@imse-cnm.csic.es

Abstract—A low power transceiver architecture for the 2.4 GHz ISM band using a 1.0 V supply is presented. It employs a transformer to convert the $100\ \Omega$ antenna impedance to almost $1\ \text{k}\Omega$ and so facilitates a low power transmitter and receiver. The simulated post-layout output power of the differential class-E power amplifier is 2.0 dBm with a drain efficiency of 28.4%. The direct-conversion receiver achieves a very low power consumption of 420 μW and a noise figure of 15.0 dB.

I. INTRODUCTION

Body area networks (BAN) using miniature sensors are expected to allow for a lot of new applications of wireless communication. They range from entertainment and automation to health care or human interface devices. In many of these applications, the need for ultra-low power consumption is priority since network nodes are supplied by small batteries or even rely on autonomous energy scavenging techniques.

Facilitating this trend, the Bluetooth SIG has recently published a low energy extension that allows short range communication with very low power consumption [1]. Bluetooth low energy also operates in the 2.4 GHz ISM band but with fewer channels at an increased spacing of 2 MHz. The modulation type is frequency shift keying (FSK) with a data rate of 1 Mbps and a modulation index of $0.5 \pm 10\%$. The standard demands for receiver sensitivity of $-70\ \text{dBm}$ or better. This translates into a tolerable noise figure (NF) of 24 dB assuming a bandwidth of 1 MHz and a signal-to-noise ratio (SNR) of 20 dB.

This paper presents a transceiver architecture intended for the new standard. In section II the transceiver architecture is presented while section III describes the circuit level implementation of the blocks. Finally, simulation results are given in section IV.

II. ARCHITECTURE

In order to increase the battery life time of the sensor node the power consumption of the transceiver must be reduced as much as possible. As a consequence the direct conversion architecture is often used for this kind of short-range wireless applications [2]–[4]. There is just one step of frequency conversion and so there are few blocks working at the radio frequency.

The block diagram of the proposed low power transceiver is shown in Fig. 1. The low requirements on the noise performance imposed by the Bluetooth low energy standard allow to use a passive receiving path. Signal amplification is

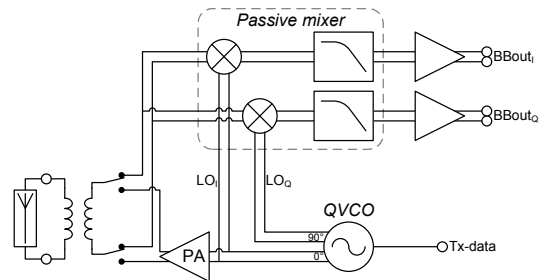


Fig. 1. Block diagram of the proposed transceiver

shifted completely into the baseband where it can be realized with less power consumption. The noise figure of this approach is defined by the losses in the passive down-conversion and the noise performance of the baseband amplifier.

A quadrature voltage controlled oscillator (QVCO) generates the I and Q phases of the carrier frequency and directly drives the switches of the passive mixer. In this setup the capacitive load of the mixer is tuned out by the inductor of the LC-QVCO [4], [5].

The transmitting path is also reduced to the minimum number of blocks. The FSK modulation defined by the Bluetooth low energy standard allows direct modulation of the VCO. The required frequency deviation of $\pm 225 \dots 275\ \text{kHz}$ can be realized using small-sized PMOS transistors as varactors [6]. Direct modulation of the QVCO makes an up-conversion mixer unnecessary and the constant envelope transmit signal allows an efficient nonlinear power amplifier.

Switching type class-E power amplifiers are known for their very good efficiency. Losses are minimized because the current peaks in the switching transistor occur when the drain-source voltage is almost zero. Moreover, class-E configuration achieves high efficiency because the drain voltage can ideally rise up to 3.56 times the supply voltage [7]. However, in order to operate the power amplifier in class-E mode for low output power levels of about 0 dBm the load resistance seen by the PA must be approximately $1\ \text{k}\Omega$. Therefore, a transformer is used to boost the antenna impedance. The transformer also provides single-ended to differential conversion if a single-ended antenna is used. Differential PAs generate smaller current peaks on the supply line than single-ended PAs, and such peaks appear at twice the operating frequency. This facilitates the decoupling of the PA from the remainder of

TABLE I
TRANSFORMER PARAMETERS

Parameter	PA/mixer coil	antenna coil
Number of turns	6	2
Windings in parallel	1	2
Serial inductance	11.6 nH	1.56 nH
Serial resistance	18.0 Ω	3.2 Ω
Coupling factor	0.85	
Area	0.116 mm ² (340 μ m x 340 μ m)	

the circuit.

The impedance conversion of the transformer is also beneficial for the receiver design because it provides passive voltage gain and the switches of the passive mixer can have a higher on-resistance.

III. IMPLEMENTATION

The transceiver front-end has been designed in a 130 nm RF CMOS process using 6 metal layers (1 thick top metal) and MIM capacitors. The supply voltage is set to 1.0 V.

A. Transformer

Impedance transformation is achieved using a step-up transformer with a 2-turn coil at the antenna port and a 6-turn coil at the internal port. In order to minimize the insertion loss the coupling factor k between the coils has to be maximized [8]. Therefore, the coil connected to the antenna consists of two parallel windings of two turns each. This also reduces the serial resistance in this coil. On the internally connected coil a high inductance is needed to support the high impedance level on this port. The transformer is drawn as a planar structure using the thick top metal layer 6 and the thin metal layer 5 of the process.

Characterization of the electrical behavior has been with the 2.5-D electromagnetic solver Momentum. The resulting s -parameter set was then fitted to a direct form model of the transformer [8] with the most important parameters presented in Table I.

B. QVCO with direct modulation

The QVCO is based on a previous work [9] using parallel coupling. Thanks to the high differential inductance of 10.2 nH in each tank it achieves an amplitude of 0.2 V at the four output I/Q phases with a very low current consumption of approximately 350 μ A.

During transmission mode only the in-phase component of the carrier is needed and therefore one core of the QVCO is deactivated. In this mode the QVCO is also used to directly generate the FSK modulation of the carrier. The high tank inductance leads to a differential capacitance of only 170 aF that has to be switched. Such a small switchable capacitance can be implemented using almost minimum sized PMOS transistors as varactors with digital control voltage [6].

In order to obtain a positive and negative frequency deviation from the carrier simply two differential varactors are used

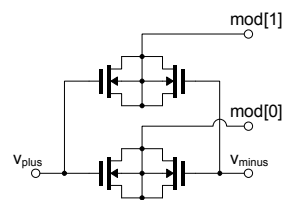


Fig. 2. PMOS varactor pair used for direct modulation of the VCO

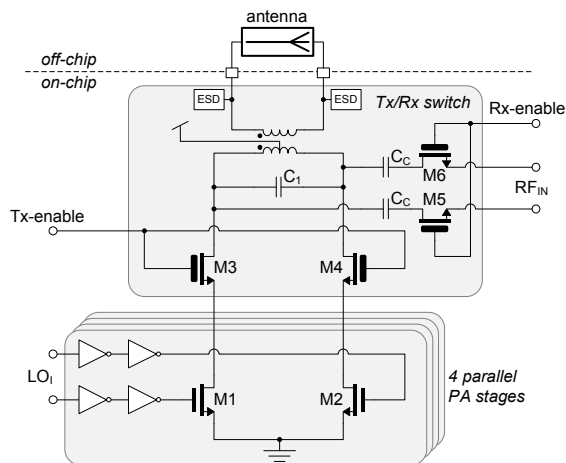


Fig. 3. Tx/Rx switch with class-E power amplifier

in parallel (Fig 2). Setting both modulation inputs (mod[0:1]) to V_{DD} leads to the higher differential capacitance and hence to a negative frequency deviation. On the other hand, setting both inputs to ground results in a positive frequency shift. The intermediate state with one input at ground and one at V_{DD} is needed to tune the VCO to the center frequency within a phase locked loop (PLL). During transmission the PLL is opened to allow direct modulation of the VCO.

The accuracy of the frequency shift heavily depends on the process variation, i.e. the offset frequency varies as much as $\pm 25\%$. Therefore, an array of 5 differential varactor pairs has to be added to the LC tank in order to select the pair with the desired frequency shift by calibration. Within the industrial temperature range of $-40^{\circ}\text{C} \dots 85^{\circ}\text{C}$ the variation fortunately is much smaller ($\approx \pm 2\%$) so that no further calibration versus temperature is needed.

C. Power amplifier

The proposed differential power amplifier is shown in Fig. 3 together with the Tx/Rx-switch. The thin oxide output transistor M1 and M2 are driven by inverters and thus operate as switches. If all parallel stages are activated the power amplifier works in class-E mode and achieves its peak efficiency and highest output power level. The concept of 4 stages in parallel has the advantage that for a reduced output power setting also the power consumption in the drivers is reduced.

The Tx/Rx switch uses thick oxide transistors in order to withstand the class-E voltage waveforms of up to 2.4 V at

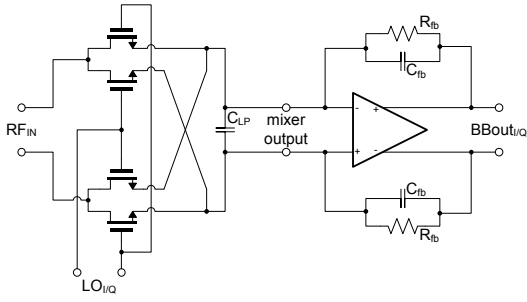


Fig. 4. Passive current-driven mixer with baseband transimpedance amplifier

their drains. Also in case of an ESD event the voltage at this points can rise up to three times higher than at the antenna input due to the impedance conversion of the transformer.

D. Receiver

In a direct-conversion receiver the low frequency $1/f$ noise is of special concern because the down-converted signal appears around DC. Since the noise density is proportional to the DC current a passive mixer with zero bias current achieves very good noise performance and a low $1/f$ corner frequency [10]. Therefore, a passive current driven mixer as shown in Fig. 4 is used in the receiver.

The noise performance of the passive mixer itself is basically defined by its conversion gain. Due to its passive behavior the conversion gain is always negative and directly increases the noise figure of the receiver. The conversion gain is improved if the transistors work as switches with a low on-resistance. This can be achieved by using wide transistors with large over drive voltage. However, larger overdrive voltage leads to an increased power consumption in the driving QVCO or even requires a buffering stage. Low on-resistance can also be achieved using wide transistors leading to an increased parasitic coupling capacitance from the mixer input to the QVCO. This would make the QVCO more susceptible to frequency pulling at high RF input levels. Therefore, in order to limit power consumption and VCO pulling the implemented passive mixer is driven by a low amplitude of 0.2 V and uses relatively small transistors.

The output of the passive mixer is loaded by the baseband transimpedance amplifier and by a MIM-capacitor ($C_{LP} = 20pF$) to remove the RF components. The amplifier presents a low impedance load ($\approx 500k\Omega$) to the mixer and converts the input current to an output voltage with a gain of $R_{fb} = 15k\Omega$. Parallel feedback capacitors C_{fb} form together with the feedback resistors R_{fb} the channel filter with a low pass corner frequency of 650 kHz.

The operational amplifier contains a differential PMOS pair for amplification followed by a buffering stage to drive the load which is mainly formed by the feedback network. Each stage works with a bias current of approximately 100 μA resulting in a total current consumption of 210 μA per baseband amplifier including biasing and common mode feedback. The common mode voltage at the input and output of the baseband amplifier

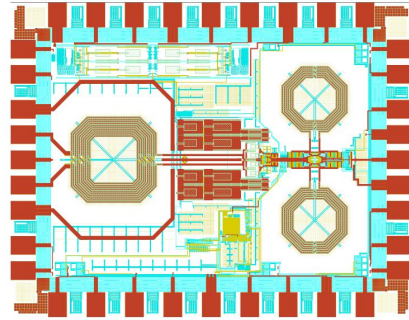


Fig. 5. Layout of the transceiver frontend test chip (die size 1.4 x 1.1 mm)

TABLE II

SIMULATED POST-LAYOUT PERFORMANCE OF THE POWER AMPLIFIER

Parameter	Value		
Supply voltage	1.0 V		
number of active stages	1	2	4
DC supply current incl. driver	2.5 mA	4.3 mA	6.2 mA
PA drain efficiency	16.0%	24.8%	28.4%
Output power (fundamental tone)	-4.2 dBm	-0.1 dBm	2.0 dBm

is set to 0.2 V in order to allow sufficient overdrive voltage in the Rx-switches (M5, M6 in Fig. 3).

IV. SIMULATION RESULTS

The complete frontend was simulated with a differential 100 Ω antenna including parasitics extracted from the layout (Fig. 5) using the SpectreRF simulator. ESD structures and a QFN36 package model have also been included in the simulation to account for losses in the antenna IOs. At the baseband outputs the amplifiers are loaded by 100 fF capacitors to account for the load imposed by subsequent stages.

The simulated power amplifier performance is summarized in Table II. It shows a peak drain efficiency at the highest output level setting of 28.4%. Including the power consumption of the QVCO with all its biasing current steered to one of the two cores, the overall efficiency of the transmitter is expected to be 24.1%.

The spectrum of the differential baseband output voltage is shown in Fig. 6 at an input level of -70 dBm. This input level coincides with the required sensitivity stated in

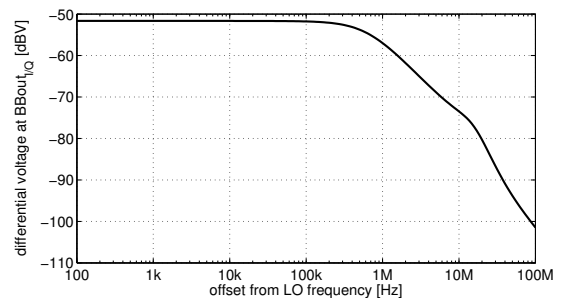


Fig. 6. Differential baseband output voltage at an input power of -70 dBm

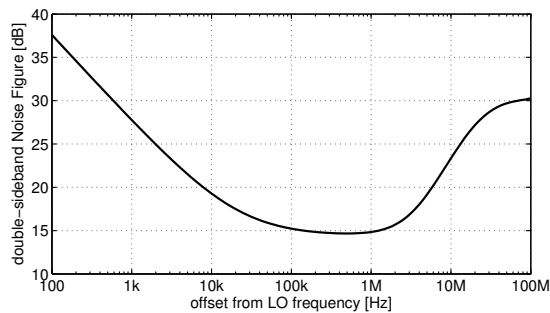


Fig. 7. Noise Performance of the receiver

the Bluetooth low energy standard. It leads to a signal-to-noise ratio (SNR) of 26.2 dB in each baseband channel and therefore leaves plenty of margin for the FSK demodulator. The overall noise figure is plotted in Fig. 7. Below the 1/f corner frequency of 20 kHz the baseband amplifier dominates the noise performance while at higher frequencies both the passive mixer and the baseband amplifier equally contribute to the total noise.

Fig 8 shows the simulation of the receiver linearity at high input levels excluding the baseband amplifier. The input referred 1-dB compression point and 3rd order intercept point are -15.3 dBm and -5.7 dBm respectively. Therefore, the RF signal has to be attenuated to reach the Bluetooth specification of -10 dBm as the maximum input signal power. Such a attenuation can be simply implemented by a transistor by-passing a portion of the current at the input of the mixer. The receiver performance is summarized in Table III.

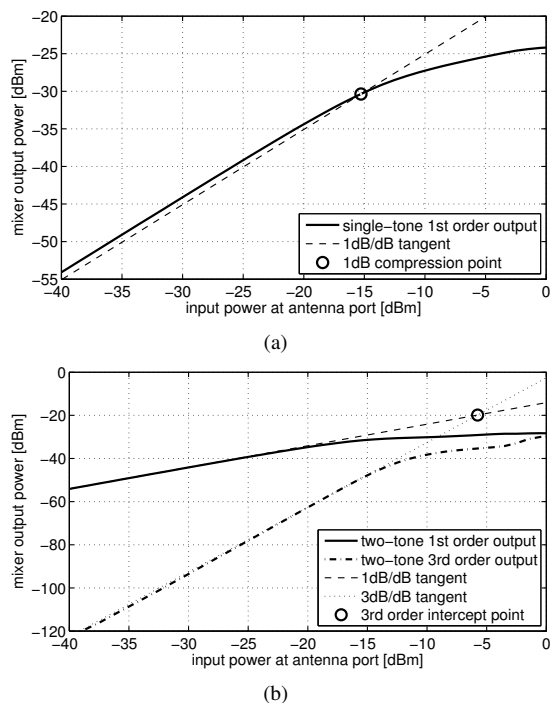


Fig. 8. Linearity of the receiver (without baseband amplifier): (a) 1dB compression point, (b) 3rd order intercept point

TABLE III
SIMULATED POST-LAYOUT PERFORMANCE OF THE RECEIVER

Parameter	Value
Supply voltage	1.0 V
RX current consumption	420 μ A
Passive conversion gain	-13.9 dB
Baseband voltage gain	32.6 dB
integrated Noise Figure (10...500kHz)	15.0 dB
1dB compression point (input referred)*	-15.3 dBm
3rd order intercept point (input referred)*	-5.7 dBm

* without baseband amplifier

V. CONCLUSIONS

A low-power transceiver architecture has been presented that is capable of conforming the Bluetooth low energy specification. The antenna impedance is up-converted by a transformer which allows the design of an efficient class-E power amplifier for low output power levels and a supply of 1.0 V. In the receiver the power consumption has been minimized as much as possible while sacrificing noise performance. Still the performance is sufficient for wireless sensor networks or body area networks.

ACKNOWLEDGEMENTS

This work has been supported by the Spanish Ministry of Science & Innovation under grant TEC2009-08447, the Junta de Andalucía under grant TIC-02818 and the 2007-2013 FEDER Programme.

REFERENCES

- [1] *Bluetooth Specification, Volume 6 (Low Energy Controller)*, Bluetooth SIG Std., Rev. 4.0, Dec 2009.
- [2] S. Hae-Moon *et al.*, "A Low Power Fully CMOS Integrated RF Transceiver IC for Wireless Sensor Networks," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 15, no. 2, pp. 227-231, 2007.
- [3] A. C. W. Wong *et al.*, "A 1 V Wireless Transceiver for an Ultra-Low-Power SoC for Biotelemetry Applications," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 7, pp. 1511-1521, 2008.
- [4] C. Bernier *et al.*, "An ultra low power 130nm CMOS direct conversion transceiver for IEEE802.15.4," in *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE, 2008*, pp. 273-276.
- [5] B. W. Cook, A. Berny, A. Molnar, S. Lanzisera, and K. S. J. Pister, "Low-Power 2.4-GHz Transceiver With Passive RX Front-End and 400-mV Supply," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 12, pp. 2757-2766, 2006.
- [6] R. B. Staszewski, H. Chih-Ming, D. Leipold, and P. T. Balsara, "A first multigigahertz digitally controlled oscillator for wireless applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 51, no. 11, pp. 2154-2164, 2003.
- [7] P. Reynaert and M. Steyaert, *RF Power Amplifiers for Mobile Communications*. Dordrecht, The Netherlands: Springer, 2006.
- [8] J. R. Long, "Monolithic transformers for silicon RF IC design," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 9, pp. 1368-1382, 2000.
- [9] J. Masuch and M. Delgado-Restituto, "Low power 2.4 GHz quadrature generation for Body Area Network applications," in *Circuits and Systems, 2010. ISCAS 2010. IEEE International Symposium on*, 2010, pp. 493-496.
- [10] E. Sacchi *et al.*, "A 15 mW, 70 kHz 1/f corner direct conversion CMOS receiver," in *Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003*, 2003, pp. 459-462.