A Low-Power Programmable Neural Spike Detection Channel With Embedded Calibration and Data Compression

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***Abstract*—This paper reports a programmable 400 μm pitch neural spike recording channel, fabricated in a 130 nm standard CMOS technology, which implements amplification, filtering, digitization, analog spike detection plus feature extraction, and self-calibration functionalities. It can operate in two different output modes: 1) signal tracking, in which the neural signal is sampled and transmitted as raw data; and 2) feature extraction, in which the spikes of the neural signal are detected and encoded by piece-wise linear curves. Additionally, the channel offers a foreground calibration procedure in which the amplification gain and the pass-band of the embedded filter can be self-adjusted. The amplification stage obtains a noise efficiency factor of 2.16 and an input referred noise of 2.84 μV_{rms} over a nominal bandwidth of 167 Hz–6.9 kHz. The channel includes a reconfigurable 8-bit analog-to-digital converter combined with a 3-bit controlled programmable gain amplifier for adjusting the input signal to the full scale range of the converter. This combined block achieves an overall energy consumption per conversion of 102 fJ at 90 kS/s. The energy consumed by the circuit elements which are strictly related to the digitization process is 14.12 fJ at the same conversion rate. The complete channel consumes 2.8 μW at 1.2 V voltage supply when operated in the signal tracking mode, and 3.1 μW when the feature extraction mode is enabled.**

***Index Terms*—Biomedical circuit, biopotential amplifier, feature extraction, low-power ADC, multichannel recording, neural recording system, spike detection.**

I. Introduction

NEURAL sensors consisting of a *Multi-Electrode-Array* (MEA) and a signal-acquisition *front-end* are crucial for the diagnosis and treatment of neural diseases as well as for brain-machine interfacing [1]–[5]. The trend today is to place together the electrodes and the front-end electronics, and to *wirelessly* transmit outside the brain the digitally encoded information derived from the captured neural activity [6]–[13]. This system embedding trend poses significant challenges to the design of the front-end electronics, besides the requirement to handle very weak signals. One of the most relevant challenges is *low-power* dissipation. It is needed to extending the life time of the implants and precluding tissue to be damaged due to excessive heating. This quest for low-power dissipation not only demands for the use of ultra-low power techniques in the design of the front-end electronics but also calls for the minimization of the amount of data to be sent in order to reduce the power budget of the communications. Accordingly, many recently reported neural sensor front-ends not only provide the means for the acquisition, amplification, filtering and digitization of the recorded activity but also include digital processing stages for data compression before transmission. Thus, in neural sensors for the acquisition of Action Potentials (AP), or spikes, it is more and more common to find feature extraction processors for their characterization [8], [9], [11], [14]–[16].

In its simplest form, neural spike feature extractors only transmit the temporal position of the spikes [8], [9]. However, for some applications this is not enough [1]–[3] and some kind of spike sorting technique must be employed. This problem can be overcome by transmitting the information of the complete spike [11]—not adequate if a big multi-electrode array is considered. Seeking to extract, and hence transmit, just the essential information required to classify spikes, techniques such as *principal component analysis* or *discrete wavelet transforms* can be employed [7]. However, they have the cost of high computational complexity [14]. Other alternative techniques, better suited for low-power close-to-sensor embedding, are based on the extraction of the amplitudes, time widths and peak positions of the spikes [15], [16]. This paper reports a neural spike detector channel chip in which relevant spike features are codified in digital domain by approximating the spike waveform by a Piece-Wise Linear (PWL) curve, as presented by the authors in [17]. As will be shown, this technique yields more than two orders of magnitude data compression as compared to raw spike information.

Besides this feature extractor, the distinctive properties of the channel architecture reported in this paper are conferred by the extensive usage of *digitally-assisted* analog circuits for reconfiguration and calibration. This has allowed to fully incorporate all needed functionalities (Band-Pass filter and Low Noise Amplifier (BP-LNA), Programmable Gain Amplifier (PGA), Analog-to-Digital Conversion (ADC), spike detector and feature extractor) within the pitch of commercially available MEAs, namely 400 μm $\times$ 400 μm [8]. As there is no need for off-channel processing or multiplexing tasks (they

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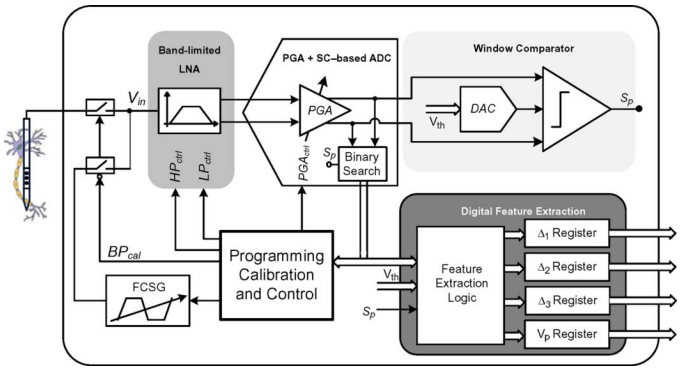


Fig. 1. Block diagram of the neural channel architecture.

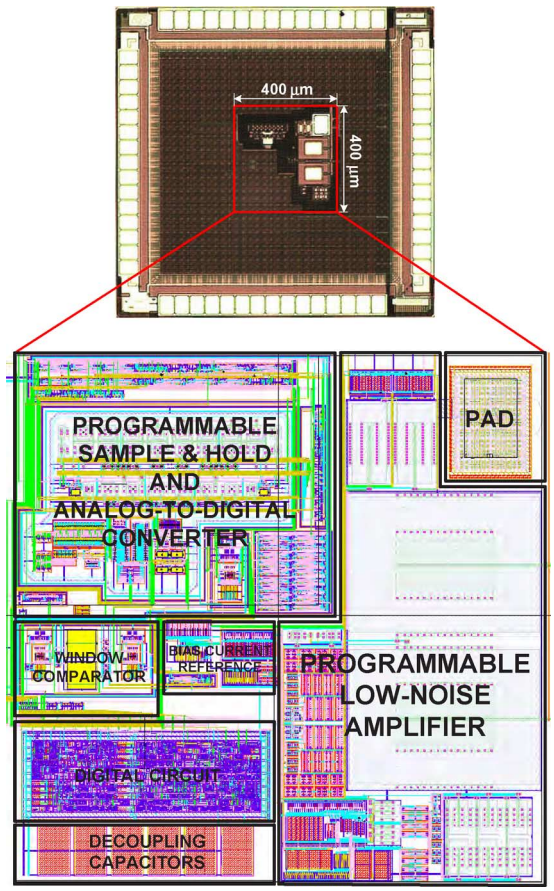


Fig. 2. Layout and microphotograph of the neural spike recording channel.

are required in other reported architectures [7]–[10], [13]), building arbitrarily large multi-channel arrays can be easily done by placing channel instances side by side and serializing their outputs for transmission through the wireless link.

The channel, whose basic architecture has been announced in [18], is reported and demonstrated in this paper through a CMOS chip in 130 nm technology. This channel chip has two *output* modes which are referred to as *signal tracking* mode and *feature extraction* mode. In the signal tracking mode, the neural signal is converted and transmitted as raw data at 22.5 kS/s output rate. In the feature extraction mode, the system detects the spikes and approximates their waveforms on-the-fly to obtain an output feature vector of 24 or 56-bit, depending on the spike shape. Additionally, the channel chip implements a foreground calibration mechanism to self-adjust the amplification and filtering characteristics of the read-out circuit. The chip supply voltage is 1.2 V and its power consumption is 2.8 μW in the signal tracking mode and 3.1 μW in the feature extraction mode.

The paper is structured as follows. Section II explains the architecture of the presented neural sensor channel. The LNA and ADC designs are detailed in Sections III and IV, respectively. Experimental results are reported in Section V, while Section VI includes the conclusions.

II. Neural Sensor Channel Architecture

Fig. 1 shows the architecture of the neural sensor channel chip and Fig. 2 shows a microphotograph of the chip and a detailed floorplan of the channel.

The chip consists of a band-limited fully-differential BP-LNA, a reconfigurable binary search based ADC which embeds a PGA, a switched-capacitor window comparator, a spike feature extractor and some digital circuitry for programming, calibration and control. Additionally, it includes a frequency-controlled signal generator (FCSG) to drive the channel during the foreground adjustment of its passband characteristics. Two low-distortion, low-resistance CMOS switches are used to selectively connect the input of the BP-LNA block to the electrode, during read-out operation, or to the FCSG generator, during calibration. These switches are implemented on deep n-wells to improve the noise isolation from the silicon substrate.

The digital core of the channel works at a master clock frequency of 800 kHz. It is responsible to define the state of the remaining blocks of the channel in accordance to the selected configuration. On the one hand, the digital core points out which blocks remain idle at each operation mode and powered them off, either totally or partially, by means of *power gating* techniques. On the other hand, it incorporates *clock division* and *clock gating* strategies, so that non-idle blocks work at the minimum clock frequency able to comply with the selected operation mode. Altogether, these power saving methods deals to a reduction in the current consumption of the complete channel of more than 30%.

The different operation modes and associated channel configurations are described below.

A. Calibration

Only the BP-LNA, the ADC, the FCSG and some digital circuitry are active during calibration. The ADC operates at 22.5 kS/s with 8-bit resolution.

Calibration starts by adjusting the passband characteristics of the BP-LNA to counteract CMOS process variations. Two programming bits $(HP_{ctrl}\langle 1:0\rangle)$ are used to calibrate the High-Pass (HP) pole of the bandpass filter, while two other $(LP_{ctrl}\langle 1:0\rangle)$ control the position of the Low-Pass (LP) pole. The goal is to tune the filter passband from about 200 Hz to 7 kHz, corresponding to the spectral range of neural spikes. The HP and LP poles are calibrated one after the other using the

same adjustment procedure. It consists in driving the BP-LNA with the output of the FCSG, tuned to the target HP or LP pole frequency, and keeping track of the attenuation from midband gain observed at the output of the ADC for the different programming sets. That configuration which obtains a voltage attenuation closer to 3 dB, situation in which the driving tone and pole position exactly coincide, is selected.

Afterwards, the gain of the PGA is adjusted. The goal is to scale the ADC input signal so that it maximally covers the full scale range of the converter without overflows. Three programmable bits ($PGA_{ctrl}\langle 2:0\rangle$) are provided to set the PGA gain from 0 to 18 dB at discrete steps of 3 dB. In this phase the input of the BP-LNA is connected to the microelectrode, thus capturing neural activity, and the FCSG block is powered off. The calibration procedure follows a binary search algorithm in which the bits of PGA_{ctrl} are sequentially set, from the most- to the least-significant bit, seeking for the largest gain possible free from ADC saturation.

The values of HP_{ctrl}, LP_{ctrl} and PGA_{ctrl} thus obtained are collected in a local memory which is later accessed and restored during readout operation.

For a more detailed description of the circuits and operations involved in the calibration flow, readers are referred to [19].

B. Signal Tracking Mode

In this operation mode the raw neural data is extracted with no additional digital processing. Hence, the signal captured by the neural electrode is first conditioned by the BP-LNA and then digitized into a 8-bit word by the ADC operating at 22.5 kS/s throughput rate. The output of the ADC is serially read out at a rate of 200 kHz for a real-time external reconstruction of the neural waveform.

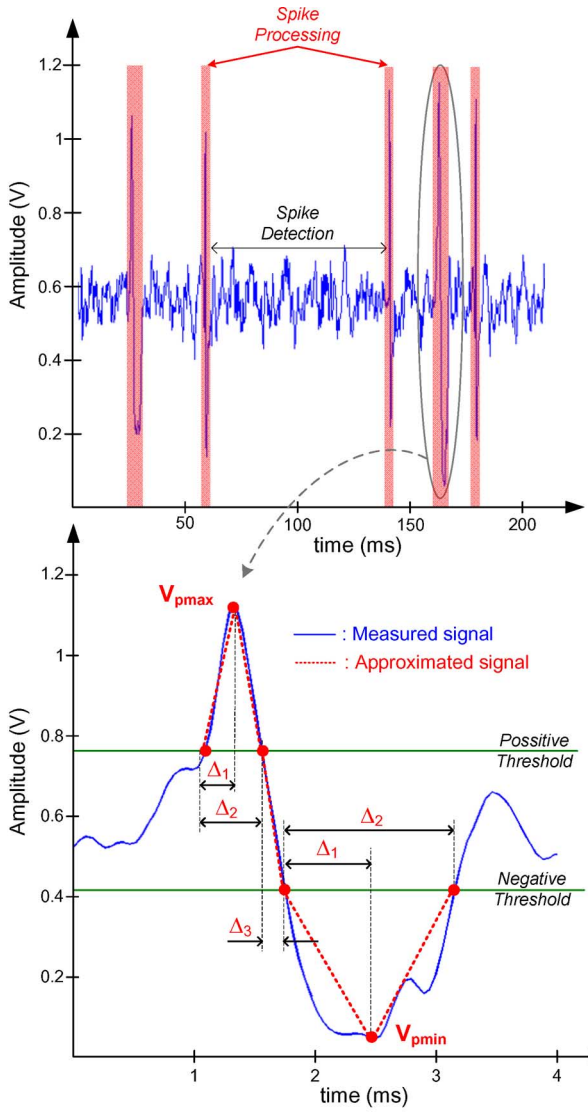
C. Feature Extraction Mode

In this mode a data reduction process is realized aiming to compress the amount of information to be transmitted by the channel. Instead of sending the complete raw data, only some features extracted from the detected spikes are actually transferred. This mode encompasses two phases, namely: *spike detection* phase and *spike processing* phase.

During the *spike detection* phase, the output of the PGA is directly processed by the window comparator at a clock frequency of 100 kHz, whereas the binary search block, responsible for the ADC conversion, is switched-off for power saving (see Fig. 1). The window comparator detects when the magnitude of the PGA output exceeds a given threshold value, V_{th}. In such a case, control signal S_p turns on (it remains in the low state, otherwise), the window comparator is disabled, and the *spike processing* phase starts. The threshold value V_{th} is externally provided in digital format and an in-channel 8-bit Digital-to-Analog Converter (DAC) is used to obtain its analogue counterpart.

During the *spike processing* phase, the feature extraction process is performed. To that end, the spike waveform is approximated on-the-fly by a first-order PWL representation, as illustrated in Fig. 3. *Monophasic* spikes, with just one single positive or negative peak, are represented with three variables: two time segments, for the peak position (Δ_1) and for the overall duration of the spike (Δ_2); and one voltage, for its peak amplitude (V_p). *Biphasic* spikes, with one positive and one negative peak, require two sets of the aforementioned variables (one per phase) and an additional measurement of the separation between the phases, Δ_3. All these variables are codified into 8-bit digital vectors to give an overall data load of 24 or 56 bits, depending on the spike shape. Potential waveform fluctuations during the spike phases are not accounted for in the PWL approximation; only the absolute maximum or minimum values are considered in the spike representation.

The feature extraction process is realized in digital domain and, therefore, the binary search block of Fig. 1 is enabled to digitize the incoming signal. A conversion rate of 90 kS/s is selected in this case. The digital PWL extractor comprises a 8-bit



	V_{peak}	Δ_1	Δ_2
Possitive peak	"11101110" (1.12 V)	"00010010" (180 us)	"00111110" (620 us)
Negative peak	"00001010" (49 mV)	"01010010" (820 us)	"10000011" (1310 us)

Fig. 3. Piece-Wise Linear spike approximation. In this example, Δ_3 is "00001101".

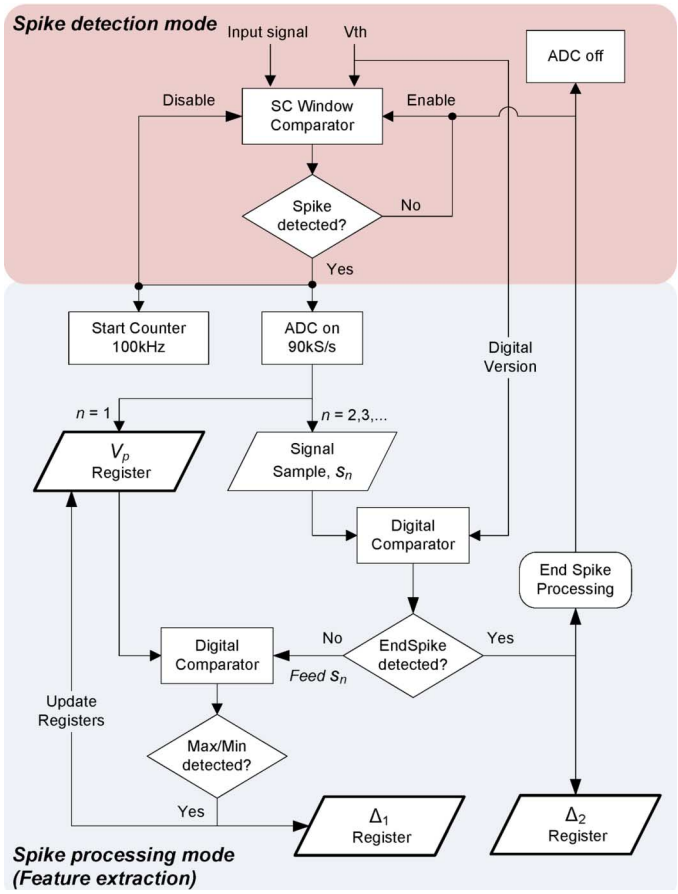


Fig. 4. Functional flow in of the digital system.

synchronous counter, digital comparators and a small finite state machine for control purposes. The counter, working at 100 kHz and enabled by the S_p signal, is used to measure the time segments Δ_1, Δ_2 and, eventually, Δ_3. The comparators are used to determine the peak positions and threshold crossings. Finally, a set of 8-bit registers are used to store the PWL variables. The algorithm is illustrated in Fig. 4 (only in the case of monophasic spikes, for simplicity). The performance of the proposed spike detection and feature extraction approaches are detailed in the Appendix.

III. Low-Noise Amplifier Band-Pass Filter

The BP-LNA block is used to boost the weak signals detected by the microelectrodes and filter out the undesired frequency components. The spectral content of neural spikes are typically comprised in the frequency range from 200 Hz to 7 kHz and their amplitudes can be as low as tens of μV. This compels the acquisition circuitry to exhibit an input-referred noise well below 5 μV_{rms} and a dc gain larger than 30 dB [8]. In order to cope with these challenging specifications, different candidate topologies for the BP-LNA block have been proposed, namely: the so-called *capacitive feedback network*, [20]–[25], the *miller integrator feedback network* [26], and the *capacitive amplifier feedback network* [27]. These topologies have been compared by the authors in [28], where it is demonstrated that the capacitive feedback solution offers the best trade-off between power,

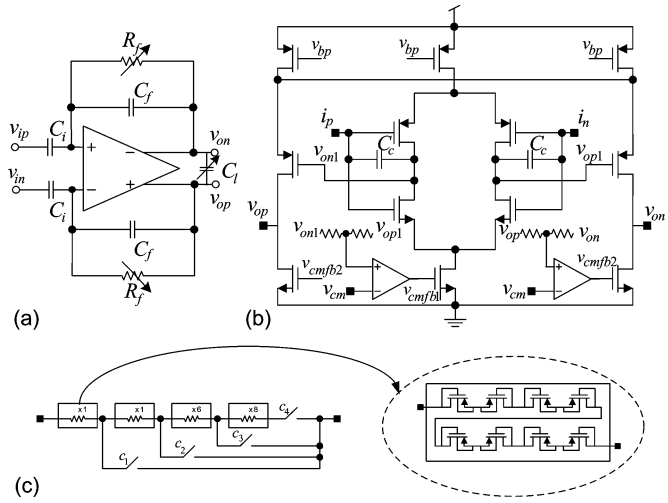


Fig. 5. Band-Pass Low-noise amplifier. (a) Schematic. (b) Transistor-level OTA implementation. (c) Programmable feedback pseudo-resistor.

area and noise efficiency. Accordingly, the proposed BP-LNA essentially follows the capacitive feedback structure as well.

Fig. 5(a) shows the schematic of the BP-LNA which introduces three main modifications to the original proposal in [20]. First, it uses a fully-differential architecture to increase the dynamic range of the amplifier and improve the PSRR and CMRR performance. Second, the Operational Transconductance Amplifier (OTA), shown in Fig. 5(b), uses a high output-swing two-stage topology with feedforward capacitive compensation in the first stage. And third, the first stage of the OTA uses a complementary input differential pair to reuse the tail current and nearly double the achieved transconductance [29].

Two continuous-time Common-Mode FeedBack (CMFB) circuits are used to set the dc common-mode output voltages of the OTA stages. In both cases, the CMFB circuit consists in a resistive divider connected to the outputs of the respective stages, and a common-mode sense amplifier driven by a common-mode voltage reference V_{cm}. This voltage is generated in-channel so as to maximize the output swing of the OTA.

Assuming that the two stages of the OTA are modeled by single-pole networks, the transfer function of the architecture in Fig. 5(a) is characterized by a midband gain, $A_m = C_i/C_f$, two zeros and three poles. The zeros are one at the origin, due to the ac-coupling through the input capacitance C_i, and the other at high frequency, due to the feedforward path through the capacitance C_f. Regarding poles, one of them, f_{HP}, is responsible for the HP corner of the bandpass transfer characteristic of the BP-LNA and it is due to the feedback network around the OTA, i.e.,

$$f_{HP} \approx \frac{1}{2\pi \cdot R_f \cdot C_f}. \tag{1}$$

The other two poles are due to the internal structure of the OTA, as well as the feedback and load capacitances. In the proposed BP-LNA, the OTA has been designed in such a way that these poles, responsible for the LP corner of the bandpass characteristic, are real and nominally identical. Accordingly, there is a double pole at a frequency, f_{LP}, approximately given by

$$f_{LP} \approx \frac{1}{\pi} \cdot \frac{g_{m2} \cdot C_f}{C_c \cdot C_{t2}} \approx \frac{1}{4\pi} \cdot \frac{g_{m1} \cdot \beta_c}{C_i} \tag{2}$$

which induces a 40 dB/dec magnitude roll-off in the transfer characteristic—beneficial to reduce the in-band integrated noise. In the above expression, g_{m1} and g_{m2} are the transconductances of the first and second stage, respectively; $\beta_c = C_c/(C_c+C_{t1})$, where C_{t1} is the capacitance at the output node of the first stage and C_c is the compensation capacitance; and $C_{t2} = C_l + C_{po2}$, where C_l is the load capacitance and C_{po2} is the parasitic capacitance at the output of the OTA.

The input-referred rms noise of the architecture in Fig. 5(a) can be calculated as

$$V_{rms} = \sqrt{2 \cdot \frac{S_{OTA} \cdot BW_{OTA} + S_{Rf} \cdot BW_{Rf}}{A_m^2}} \tag{3}$$

where S_{OTA} and BW_{OTA} are, respectively, the output-referred noise spectral density and the equivalent noise bandwidth of the OTA; and S_{Rf} and BW_{Rf} are likewise defined for the feedback resistor R_f.

Assuming that the input transistors of the OTA operate in weak inversion, the output-referred noise spectral density of the OTA, S_{OTA}, is approximately given by

$$S_{OTA} \approx \frac{4KT \cdot n}{2g_{m1}} \tag{4}$$

where n is the transistor slope factor. Regarding the equivalent noise bandwidth of the OTA, it can be approximated, after some algebra, by the expression

$$BW_{OTA} \approx \frac{A_{o1}(\beta C_c + C_f)^2 \cdot g_{m2}}{4\beta^2 C_f \left[C_{eq} C_f + A_{o1} C_c (C_f + C_{t2})\right]} \tag{5}$$

where $\beta = C_f/C_f + C_i + C_p$ and $C_{eq} = C_i + C_p + C_{t2}/\beta$ are, respectively, the feedback factor and the equivalent input capacitance of the BP-LNA; C_p stands for the total parasitic capacitance at the input node of the OTA; and A_{o1} is the dc gain of the first stage.

For the feedback resistance, $S_{Rf} = 4KT \cdot R_f$ and the noise equivalent bandwidth can be approximated as $BW_{Rf} \approx 1/4C_f R_f$. Replacing these equations as well as (4) and (5) into (3), it can be found that

$$V_{rms} \approx \sqrt{\frac{k \cdot T \cdot \gamma}{C_i} \cdot \left(\frac{C_f}{C_i} + \frac{\beta_c \cdot \left(1 + \frac{C_c}{C_i}\right)^2 \cdot n}{8} \right)}. \tag{6}$$

A methodology similar to [30], [31] has been applied to select the best implementation in terms of power consumption, area occupation and noise performance. During the design procedure, some relevant technological parameters are extracted and stored in look-up tables. This information is then combined with the above equations to get an optimized sizing of the different LNA devices according to the selected targets. The outcome of this process was a BP-LNA instance with $A_m = 47.5$ dB, $C_f = 125$ fF, $C_c = 350$ fF and $C_i = 30$ pF.

In this design, the OTA shows an open-loop dc gain of 90 dB and a gain-bandwidth product of 5.75 MHz for a load capacitance of 5 pF. The BP-LNA is unconditionally stable under PVT (process corner, voltage supply, operating temperature) variations.

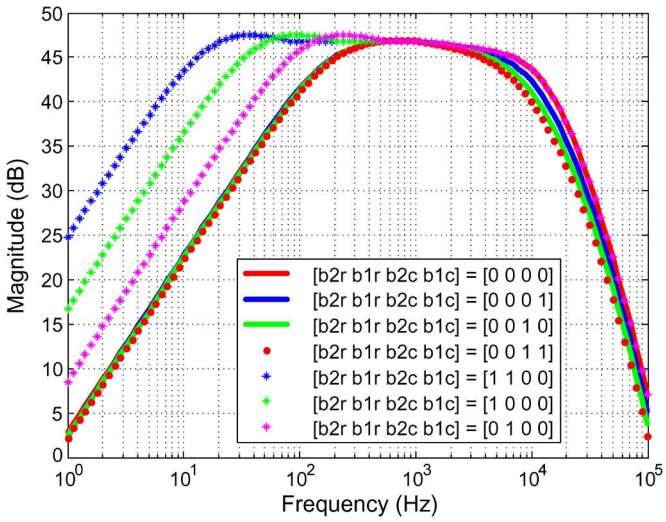


Fig. 6. BP—LNA measured frequency response for the different pole position configurations.

Due to the low frequency specified for the HP pole (1), very large feedback resistances must be employed in the BP-LNA. They have been implemented with pseudo-resistors based on pMOS transistors in deep subthreshold, as shown in Fig. 5(c) [29]. In order to improve linearity, the feedback resistor is implemented by the series connection of at least eight of these pseudo-resistors.

The frequencies of the HP and LP poles are process-dependent. Indeed, our PVT simulations show that the HP pole may vary by more than 200%, whereas the variations of the LP pole may be in the order of 40%. To cope with this situation, both the feedback resistance and load capacitance of the BP-LNA are made digitally adjustable with programming words $HP_{ctrl} = [b2r, b1r]$ and $LP_{ctrl} = [b2c, b1c]$, respectively. These words are automatically estimated by following the calibration procedure described in Section II-A. Programming the feedback resistance is accomplished by altering the number of serially connected pseudo-resistors, as shown in Fig. 5(c). Similarly, the load capacitance is programmed by properly adding capacitors in parallel. Basic component sizes, either pseudo-resistors or capacitors, in these programmable arrays have been properly scaled so as to uniformly cover the variation ranges estimated by PVT simulations.

The performance of the BP-LNA has been validated through measurements from the chip. Fig. 6 shows the measured frequency response of the BP-LNA for the different HP and LP tuning configurations. The midband gain is about 47.5 dB in all cases. The HP pole can be adjusted from 11.5 to 167 Hz, whereas the tuning range for the LP pole is from 4.8 to 9.8 kHz. After calibration (see Section II-A), the nominal bandwidth of the BP-LNA is established as 167 Hz–6.9 kHz. Unless otherwise stated, measurements were obtained with this nominal bandwidth configuration. It is worth observing the programming range of the HP pole is not wide enough to include the target position of 200 Hz. This reveals the transistors models provided by the foundry for deep subthreshold operation are not accurate enough. In practice, it would have been convenient to extend the

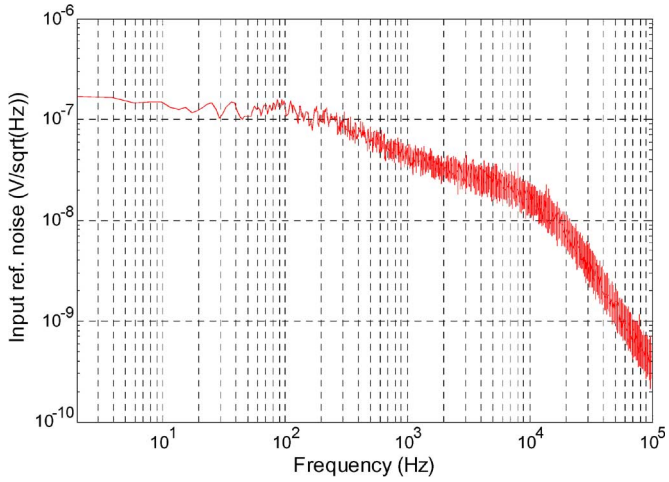


Fig. 7. Measured input-referred noise voltage spectral density of the BP-LNA.

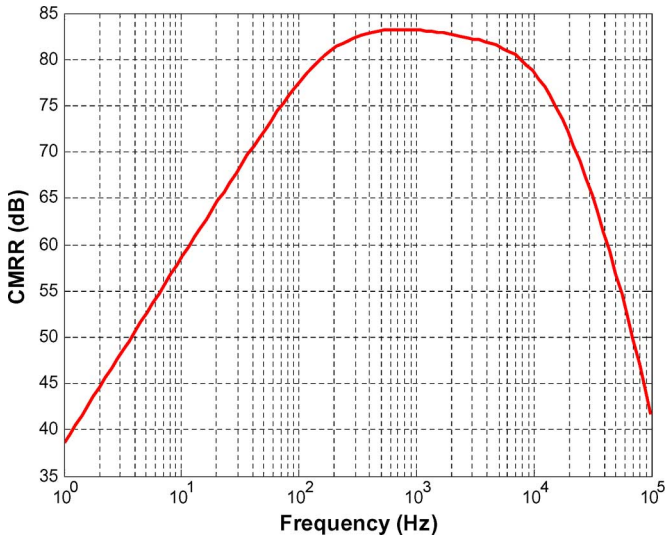


Fig. 8. Measured BP-LNA CMRR.

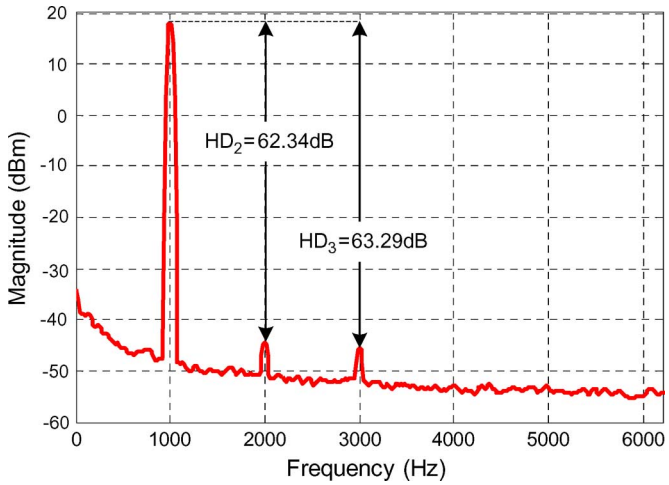


Fig. 9. Measured BP-LNA output distortion.

programming range even beyond the estimations derived from PVT simulations.

Fig. 7 shows the input-referred noise spectral density of the BP-LNA. The rms value of the input referred noise is 3.8 $\mu\mathrm{V}_{rms}$, integrated from 1 Hz to 100 kHz, and 2.84 $\mu\mathrm{V}_{rms}$ over the nominal passband. Fig. 8 shows the CMRR of the BP-LNA, which obtains more than 83 dB in the passband. Unfortunately, the experimental setup does not permit to measure the PSRR; simulation results obtain values larger than 70 dB, though. As an illustration of the linearity performance, Fig. 9 plots the frequency response of the BP-LNA for a 1 kHz input tone with 2 mV_{pp} amplitude. As can be seen, the second and third harmonics are more than 60 dB below the fundamental. For 4.1 mV_{pp} amplitude, the THD of the BP-LNA degrades to about 1% because of the OTA saturation onset.

The current drawn by the BP-LNA is 1.6 μA, thereby resulting into a power consumption of 1.92 μW from a 1.2 V supply voltage. The Noise Efficiency Factor (NEF) of the BP-LNA, defined as [32]

$$NEF = V_{rms} \cdot \sqrt{\frac{2I_{tot}}{\pi \cdot U_t \cdot 4kT \cdot BW}} \tag{7}$$

amounts 2.16 over a noise integration bandwidth of 1 Hz–100 kHz, and 1.62 over the filter passband. Table I summarizes the performance of the BP-LNA in perspective with other recent publications.

IV. PGA and ADC

Programmable gain and data conversion are embedded into a single block. It is a sort of *reconfigurable*-ADC in which the functionality (either S&H or ADC), signal gain and sampling frequency are digitally-programmable. Such flexibility is crucial for saving area and power—the most important constraints of our neural channel chip.

To confront the design of the ADC one may think of using *Successive Approximation Register* (SAR) architectures with *capacitive-based* DACs. Actually, these architectures are well suited for low-power, medium resolutions ADCs [33]–[36] and have been extensively employed for neural recording applications [6]–[10]. However, because of the large number of unitary elements required by capacitive DACs, these architectures are not appropriate in scenarios with strong area constraints, as it is the case of this design where the whole channel must fit in a pitch of 400 μm.[1] Alternative architectures must be devised instead.

The proposed ADC follows a binary search algorithm for data conversion employing the SC architecture of Fig. 10(a) [37]. The circuit consists in two active blocks, a S&H programmable gain amplifier/integrator (which uses a single operational amplifier) and a comparator, as well as a conventional SAR register (not shown in the figure). Circuit operation is as follows. The signal is first sampled and stored in the integrator by transferring

[1]The total capacitance required by conventional binary weighted arrays is $2^N C_u$, where N is the resolution of the converter and C_u is the value of the unitary capacitor—ultimately determined by noise, linearity and matching considerations. Even using specific techniques for area reduction, e.g. array splitting with attenuation capacitors, the smaller SAR converters proposed so far, with requirements on resolution and speed similar to those in this design, have an area occupation larger than 0.05 mm^2. Our proposal obtains more than 30% area reduction, including the programmable gain amplifier which not only serves the purposes of data conversion but also amplification adjustment.

TABLE I
STATE-OF-THE-ART COMPARISON OF THE BP-LNA MEASURED PERFORMANCE

	[6]	**[10]**	**[20]**	**[21]**	**[23]**	**[25]**	**[26]**	**[29]**	**This work**
Voltage Supply (V)	1	3	5	2.8	1.8	3	1.8	1	1.2
Technology (μm)	0.35	0.35	0.5	0.5	0.18	1.5	0.18	0.13	0.13
Fully differential	No	Yes	No	No	No	No	No	Yes	Yes
Input ref. noise (μV_{rms})	4.43	6.08	2.2	3.06	3.5	7.8	5.6	1.95	3.8
Noise int. bandwidth (Hz)	1-12k	500-10k	N/A	10-70k	10-100k	0.1-10k	1-100k	0.1-25.6k	1-100k
Bandwidth (Hz)	217-7.8k	10-5k	0.025-7.2k	45-5.32k	10-7.2k	50-9.1k	98.4-9.1k	23m-11.5k	167-6.9k
Gain (dB)	45.7	33	39.5	40.85	39.4	39.3	49.52	38.3	47.5
CMRR (dB)	58	60	83	66	70.1	N/A	50	63	83
PSRR (dB)	40	N/A	85	75	63.8	N/A	50	63	N/A
THD	0.53%	N/A	1%	1%	1%	1.1%	1%	1%	1%
Input range (mV_{pp})	full range		12.4	7.3	5.7	5	2.4	0.16	3.1
Power cons. (μW)	1.26	8.4	80	7.56	7.92	114.8	8.4	12.5	1.92
NEF	2.16	5.55	4	2.67	3.35	19.4	4.9	2.48	2.16

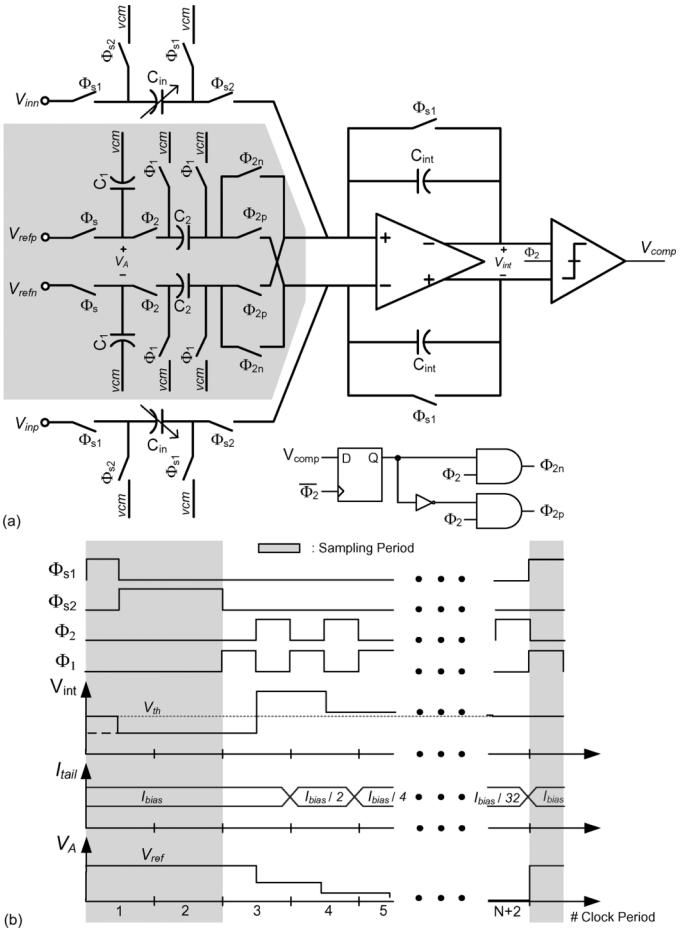


Fig. 10. SC-based ADC. (a) Schematic. (b) Waveform.

charge from capacitor C_{in} to C_{int}. Afterwards, the conversion phase starts. It is simply realized by successively comparing the integrated voltage with $V_{ref}/2^n$, where V_{ref} is the full-scale reference voltage of the converter, and index $n = 1, \ldots, N$, indicates the conversion step (N represents the converter resolution). The weighted voltages $V_{ref}/2^n$ are generated by a passive SC arrangement [shaded area in Fig. 10(a)]. If the integrated voltage is larger (alternatively, smaller) than V_{th} the comparator

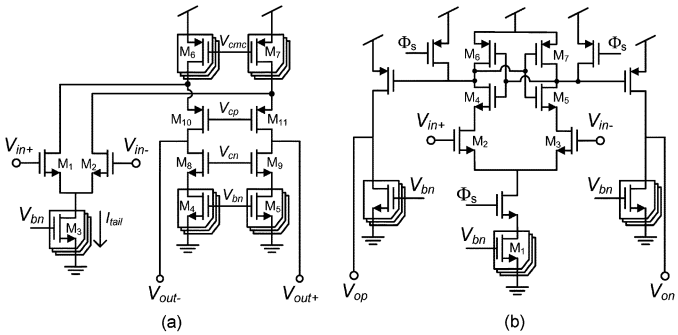


Fig. 11. Transistor-level schematic. (a) OTA. (b) Dynamic-latch.

sets to '1' (alternatively, '0') the n-th conversion, and the integrator is updated by subtracting (alt. adding) $V_{ref}/2^n$. As illustrated in the timing diagram of Fig. 10(b), the conversion takes $N + 2$ clock cycles, 2 for sampling and N for carrying out the binary search algorithm.

During spike detection, the voltage divider and the comparator are disabled and the block operates as a PGA, clocked at 100 kHz. The gain of the PGA can be adjusted from 0 to 18 dB at discrete steps of 3 dB (this gives a total gain for the channel front-end of 47.5–65.5 dB, including the LNA contribution) by controlling a 3-bit programmable input capacitance. When the ADC functionality is enabled (during the rest of the operation modes), the sampling frequency can be programmed between 22.5 kS/s and 90 kS/s.

Fig. 11(a) shows the schematic of the fully differential OTA in the PGA + ADC. It is a folded-cascode topology with a SC-based common-mode feedback circuit (not shown). The OTA uses a dynamic biasing scheme in which supply currents are adjusted according to the slew-rate demand. This is accomplished by controlling the widths of transistors M3-M7. As an illustration, 10(b) shows how the tail current provided by transistor M3 decreases along the conversion process. It is worth mentioning this OTA reconfiguration, applied during the hold phases (Φ_1), has negligible impact on the voltage stored in the integration capacitor, i.e., no contamination by kick-back effects is observed during ADC operation.

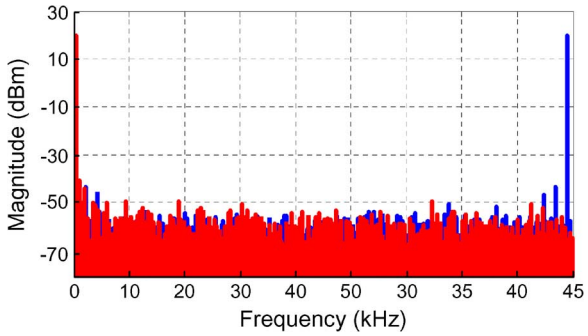


Fig. 12. FFT-spectrum of the ADC response for low and Nyquist input frequencies sampled at 90 kS/s.

Fig. 11(b) shows the schematic of the comparator, a current-controlled dynamic-latch buffered with class-A amplifiers.

The dynamic latch is formed by a differential pair loaded by a positive feedback network based on cross-coupled inverters. When the strobe signal $\Phi_s$turns on, the differential pair transforms the input voltage into a current unbalance which is regenerated and latched by the feedback network to obtain a binary differential output voltage. This voltage is boosted to the rails by means a two class-A amplifiers. The outputs of these amplifiers drive a conventional RS latch (not shown) to store the results of the comparison. As in the OTA, the bias currents of the differential pair and the class-A amplifiers are adapted according to the selected sampling frequency.

Experimental results show that the Equivalent Number of Bits (ENOB) of the ADC is 7.62-bit for a sampling frequency of 90 kS/s, and 7.65-bit for 22.5 kS/s. The total power consumption of the PGA+ADC is 1.8 μW average when the ADC runs at 90 kS/s. It decreases to 500 nW when the sampling frequency is 22.5 kS/s, and to just 360 nW when the ADC function is disabled and the S&H samples the input signal at 100 kHz. Fig. 12 shows the spectrum of the ADC output at 90 kS/s sampling rate (spike processing) for a low input frequency and at Nyquist rate, respectively. The measured linearity is represented in Fig. 13 by means of the INL and DNL.

Defining the Figure of Merit (FoM) for the analog-to-digital conversion as

$$FoM = \frac{P_{ADC}}{f_s \cdot 2^{ENOB}} \tag{8}$$

we obtain 102 fJ/conv for the PGA and ADC sampling at 90 kS/s. In order to make a fair comparison with the state-of-the-art on ADCs, we have calculated the FoM value when only the power of the blocks contributing to the conversion is accounted for; i.e., by excluding the power required to build the PGA functionality. It results into 250 nW, which gives a FoM of 14.12 fJ/conv.

Table II summarizes the performance of the PGA + ADC under its different modes of operation.

V. SC Window Comparator

The window comparator detects a neural spike when the differential output of the S&H PGA goes (in absolute value) above a certain threshold voltage configured by means of the 7-bit digital word V_{th}. Fig. 14 shows the schematic of the window

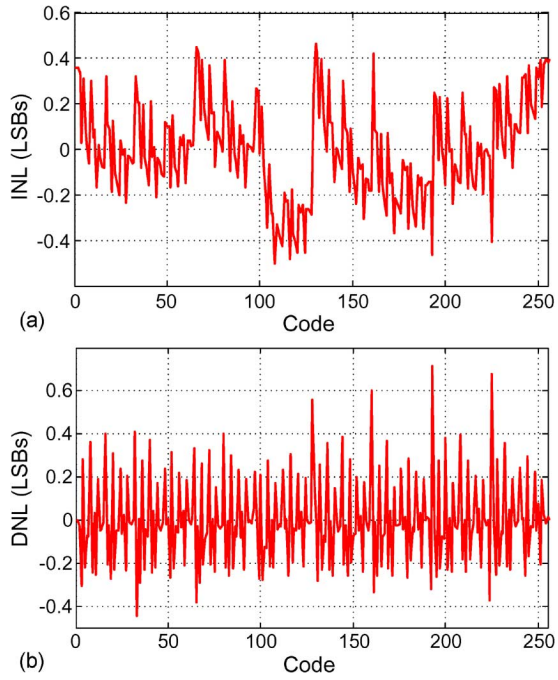


Fig. 13. Linearity response of the ADC. (a) INL. (b) DNL.

TABLE II
PGA + ADC Performance

	PGA + ADC		PGA S&H
Sampling frequency	90kS/s	22.5kS/s	100kS/s
Voltage Supply	1.2-V		
SNDR	47.63dB	47.81dB	49.8dB
SFDR	62.62dB	62.53dB	65.3dB
ENOB	7.62-bits	7.65-bits	7.98-bits
INL	-0.5 - 0.45 LSBs		N/A
DNL	-0.42 - 0.71 LSBs		N/A
Power Consumption	1.8μW	0.5μW	0.36μW
FoM	101.67fJ/conv	101.63fJ/conv	N/A

comparator. It is a switched-capacitor implementation which requires two comparators; one detects the sign of the sampled signal and the other detects the occurrence of the spike. The first one reuses the comparator of the ADC (which is disabled during the spike detection phase), while the second one is implemented using the same dynamic-latch architecture presented in Fig. 11(b). The comparison phase starts by storing the analog threshold voltage in the input capacitors with opposite signs. In the next phase, the differential output of the S&H PGA is connected to the input capacitors depending of the detected sign. Thus the compared voltage is $|V_{ip} - V_{in}| - 2 \cdot V_{th}$, in order to detect both the positive and negative spikes. Note that, as the threshold voltage is multiplied by two, the input digital signal has to be divided by two and, consequently, the system only needs a 6-bits DAC.

The employed DAC follows an architecture similar to that presented in [38], a 6-bits R-2R resistive current divider structure with pMOS transistors. This architecture achieves the required resolution with very low area occupation and a minimum power consumption. Simulation results show that the output

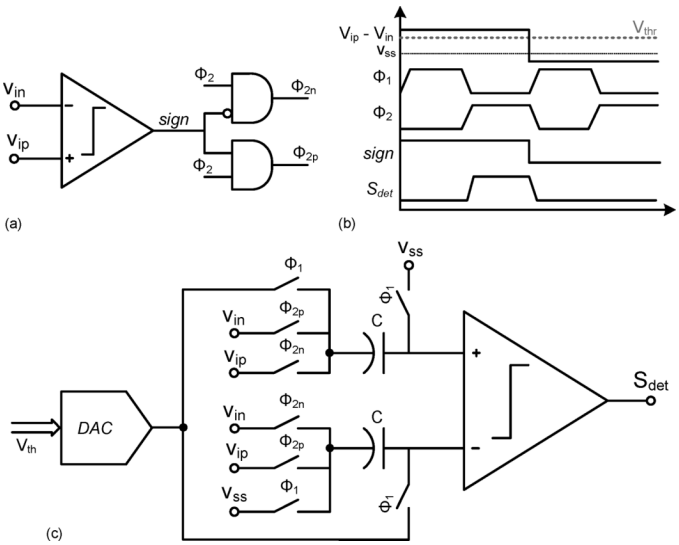


Fig. 14. Schematic of the window comparator. (a) Sign spike detector. (b) Signal waveform. (c) Window comparator.

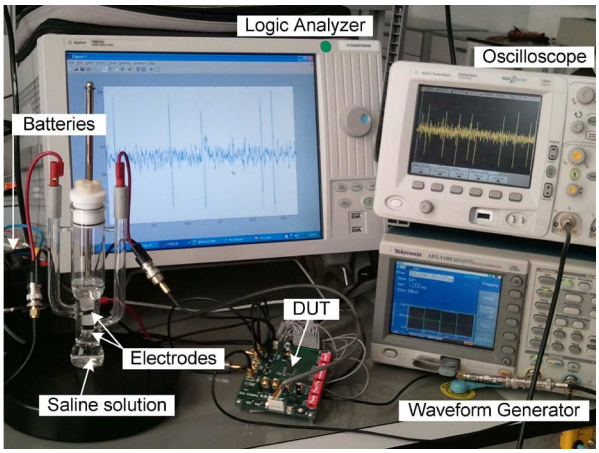


Fig. 15. Experimental set-up for measurements with saline solution.

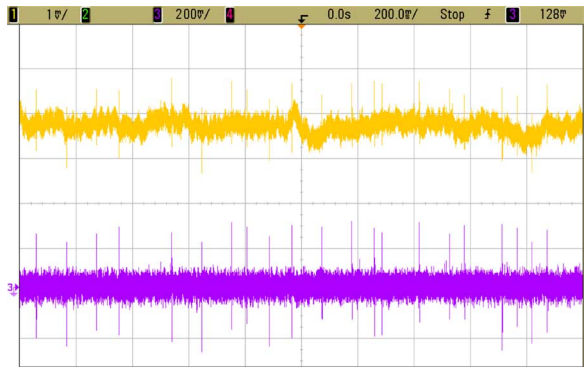
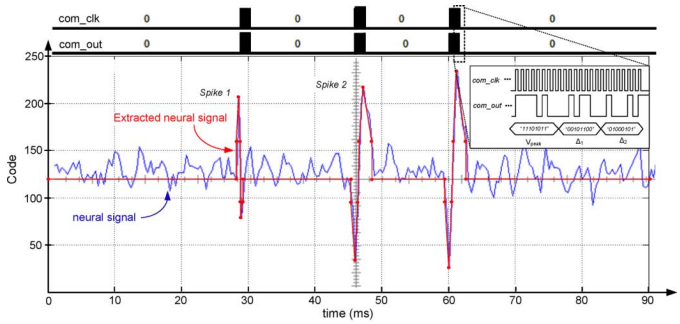


Fig. 16. Oscilloscope capture for the saline solution experiment: input neural signal with low-frequency LFP disturbance (up) and output of the BP-LNA (down).



	Spike 1			
	V_{peak}	Δ_1	Δ_2	Δ_3
Possitive peak	"11010001" (209)	"00010101" (210 us)	"00101011" (430 us)	"00001111" (150 us)
Negative peak	"01001110" (78)	"00010110" (220 us)	"00101100" (440 us)	
	Spike 2			
	V_{peak}	Δ_1	Δ_2	Δ_3
Possitive peak	"11011001" (217)	"00101010" (420 us)	"01010101" (850 us)	"00001011" (110 us)
Negative peak	"00100001" (33)	"00011111" (310 us)	"01000000" (640 us)	

Fig. 17. Capture of the logic analyzer screen under the feature extraction mode.

noise voltage of the resistive DAC is around 450 μV_{rms}, similar to the 475 μV_{rms} output power noise of the LNA, which makes this design suitable for the application.

The power consumption of the window comparator and the DAC is 200 nW.

VI. Experimental Results

The performance of the neural channel sensor has been first validate with an experiment that emulates the neuron-electrode interface in a real neural recording system by means of a controlled saline solution. Fig. 15 shows the set-up of the experiment. The input signal is synthetically generated with an arbitrary waveform generator and introduced in the saline solution through an electrode. This signal is captured by another electrode 2 cm away from the first and connected to the input of the neural channel. In order to emulate the conductivity of the brain tissue, the selected 0.01-molar saline solution has a conductivity of 0.15 S/m [39]. The system is powered by means of two external batteries to reduce as much as possible the 50 Hz interference of the power line.

Fig. 16 illustrates the output of the BP-LNA for a neural input signal containing spikes and a subjacent low-frequency *local field potential* (LFP) waveform. This signal, on the top of Fig. 16, has been taken from a public database of *intra-cortical* recordings [40]. It features 3.0 mVpp amplitude and an output rate of 30 kS/s. A dc offset of 50 mV has been intentionally superposed to this signal. The output of the BP-LNA, represented on the bottom, shows that both the LFP signal and the dc offset are successfully attenuated by the filter. The spikes are clearly visible and detectable.

Fig. 17 shows the response of the system when it works under the feature extraction mode. Signal *com_out* represents the serial output of the spike feature registers, while *com_clk* is the clock signal employed to read this data. The input signal is a synthetic neural signal with 0.8 mVpp amplitude and the dc gain of the channel amounts 59.5 dB after calibration. Both the input signal and the obtained feature extracted PWL representation have been overlaid to appreciate the operation of the extractor.

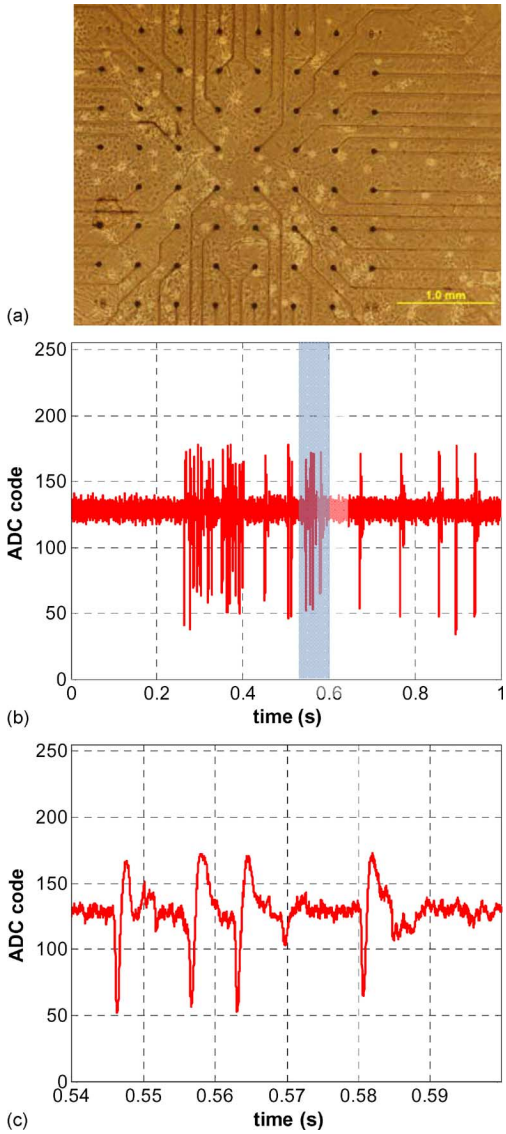


Fig. 18. *In vitro* experiment. (a) Microphotograph of the hippocampus cell culture inside the *in-vitro* MEA. (b) Segment of the extracellular recording with a burst of spikes and (c) zoom over four consecutive spikes.

The collected information for the extracted spikes is shown at the bottom of the figure.

Extracellular recordings were made from a culture of human hippocampus cells to verify the functionality of the acquisition system in a real recording environment. We used a standard *in-vitro* MEA with a pattern of 8 × 8 electrodes, 400 μm pitch. Fig. 18(a) shows a microphotograph of the biological tissue inside the MEA. The channel input signal was taken from one of the microelectrodes with higher neural activity. The dc gain of the channel took its maximum value (65.5 dB) after calibration because the amplitude of the extracellular action potential was less than 350 $\mu\mathrm{m}\mathrm{V}_{pp}$. The BP-LNA was set after calibration to its nominal bandwidth, 167 Hz–6.9 kHz. Fig. 18(b) shows a segment of the recorded waveform at a sampling rate of 22.5 kS/s and Fig. 18(c) shows a zoom of the shaded area in Fig. 18(b), in which four spikes can be easily distinguished. Again, the spikes were clearly visible and detectable along the whole recording session.

TABLE III
MEASURED PERFORMANCE OF THE NEURAL CHANNEL

Operation Mode	Signal Tracking	Spike Feature Extraction Processing	Spike Feature Extraction Detection
Neural Recording Channel			
Process	Standard CMOS 0.13μm		
Supply Voltage	1.2 V		
Overall Gain	47.5 - 65.5dB (3dB step adjustable)		
Power Consumption	2.8μW	3.1μW	
Die Area	0.16mm^2 (400μm x 400μm)		
Band-Pass Low-Noise Amplifier			
Input-referred noise *200Hz - 7kHz* *1Hz - 100kHz*	 2.84μV_{rms} 3.8μV_{rms}		
Low-freq. pole	11.5 - 167Hz (2-bits adjustable)		
High-freq. pole	4.8 - 9.8kHz (2-bits adjustable)		
Power Consumption	1.92μW		
PGA and Analog-to-Digital Converter			
Enabled Blocks	PGA+ADC	PGA+ADC	PGA
Sampling Rate	22.5kS/s	90kS/s	100kS/s
ENOB	7.62-bits	7.65-bits	7.98-bits
Power Consumption	500nW	1.8μW	360nW
DAC + Window Comparator			
DAC resolution	8-bits		
Comparator time response	5μs		
Power Consumption	OFF	OFF	200nW
Digital ASIC			
Reference clock frequency	800kHz		
Serial output buffer	8-bits	24-bit	
Serial output data rate (30 spikes/second)	180kbps	1.44kbps	
Power Consumption	50nW	200nW	

The measured performance of the presented neural recording channel is shown in Table III. The total power consumption of the system (including the 280 nW due to biasing circuitry) is 2.8 μW at the signal tracking mode. When the feature extraction mode is selected, we have to distinguish between the power consumed during the detection operation (2.96 μW), on the one hand, and during the spike processing analysis (4.2 μW), on the other hand. Assuming that, on average, the firing rate of neural signals is of 30 spikes/second and the spike mean duration is about 3 ms, the system will only process the spike during 9% of the time, while the rest will work under the spike detection mode. Consequently, when the system is configured on the feature extraction mode, the average power consumption is 3.1μW. A low-leakage technology option has been employed resulting into a total leakage power of 50 nW for the digital circuitry.

It is also important to remark the achieved reduction of the output data bitrate when the feature extraction mode is selected. It goes from 180 kbps when no signal analysis is done (signal tracking mode) down to 1.44 kbps when just the main spike features are sent, which means a reduction of more than 99%.

VII. CONCLUSIONS

The channel reported in this paper is conceived to include all the circuitry needed to sense, detect, extract features and digi-

TABLE IV
NEURAL CHANNEL SENSORS WITH FEATURE EXTRACTION CAPABILITIES STATE-OF-THE-ART COMPARISON

	[7]	[8]	[9]	[11]	[12]	[13]	This work
Supply Voltage	3.3-V	3.3-V	1.5-V	1.8-V	3.3-V	3-V	1.2-V
CMOS Process	0.35μm	0.5μm	0.5μm	0.18μm	0.35μm	0.5μm	0.13μm
LNA - BPF	*on-channel*	*on-channel*	MUX 1:16	*on-channel*	*on-channel*	*on-channel*	*on-channel*
Low-freq. corner	0.1 - 200Hz	300 - 800Hz	0.1 - 100Hz	100Hz	200Hz	0.1 - 1000Hz	11.5 - 167Hz
High-freq. corner	2 - 20kHz	5kHz	9.1kHz	9.2kHz	10kHz	8kHz	4.8 - 9.8kHz
Input ref. noise	4.9μV_{rms} (0.1Hz - 20kHz)	5.1μV_{rms}	8μV_{rms} (10Hz - 10kHz)	5.8μV_{rms}	3μV_{rms}	4.32μV_{rms} (1Hz - 10kHz)	3.8μV_{rms} (1Hz - 100kHz)
Midband Gain	57 - 60dB	60dB	59.5dB	70dB	74dB	67.8 - 78dB	47.5 - 65.5dB
ADC	MUX 1:16	MUX 1:100	MUX 1:4	*on-channel*	*on-channel*	N/A	*on-channel*
Sampling Rate	40kS/s	15kS/s	62.5kS/s	30kS/s	40kS/s	N/A	90kS/s
Resolution	9-bits	10-bits	8-bits	7-bits	10-bits	N/A	8-bits
Max. DNL/INL	N/A	0.6/0.6 LSBs	N/A	0.5/0.5 LSBs	0.8/1.8 LSBs	N/A	0.71/0.5 LSBs
Feature Extraction	Digital Derivative approx.	Analog Spike det.	Digital Duration	Digital Waveform	N/A	Analog PWM	Digital PWL on-channel
Bits per spike	54-bits	1-bit	24-bits	512-bits	N/A	36-bits	24/56-bits
Power/channel	24.22μW	142μW	24.6μW	42.5μW	330μW	75μW	3.1μW
FOM (pJ/conv)	1.18	9.24	1.54	11.07	8.05	N/A	0.18

tize spikes within an area of $400\ \mu\text{m} \times 400\ \mu\text{m}$, using a standard 130 nm CMOS process, thus fitting to the pitch of commercially available microelectrodes and making it feasible for multi-channel recording. Key point of the reported design are reconfiguration, on the one hand, and data compression on the other. Regarding the latter, Table IV compares the specs of previously reported neural channels with embedded feature extraction to those of the chip presented in this paper. As it can be seen our chip includes all functions (signal adaptation, digitization, spike detection and feature extraction) on-channel, and achieves the lowest power consumption per channel. The FoM value displayed in the table is defined as in (8) but taking into account the power consumption of the channel. Regarding reconfiguration, our chip includes foreground self-calibration (filter bandwidth and PGA), is able to operate at different modes and reconfigure the building blocks dynamically depending selected operation mode. All-in-all, all these reconfiguration features are crucial to achieve the low power operation figures.

Experimental results show that the circuit requires 2.8 μW, from a 1.2 V supply, when tracking the input signal, and 3.1μW if the feature extraction mode is selected. The input referred noise is 3.8 μV_{rms} when integrated in a 1 Hz–100 kHz band, resulting into a NEF value of 2.16. The measured ENOB is 7.64-bits with a power consumption of 1.8 μW at 90 kS/s. Experiments with conductivity-controlled saline solution and *in-vitro* extracellular recordings were done to verify the proper operation of the channel.

Comparison with other published neural sensor interfaces shows that the chip reported in this paper shows the lowest power consumption and is the only one that integrates all the functionality within an electrode pitch area.

APPENDIX

To evaluate the performance of the spike detection and feature extraction, 60-seconds spike-controlled neural signals were used as channel input. These signals were built from an extense neural spike database of *intra-cortical* recordings [40] and randomly distributed following a Poisson distribution with controlled firing rates and background noise levels. The background neural noise noise was generated from 25 aggregated synthetic neural signals with different firing rates to simulate the interference caused by close neurons. The amplitude of this interference was adjusted in the different tests to achieve different signal-to-noise ratios (SNRs). The SNR is defined as [16]

$$SNR = 20 \cdot log_{10}\left(\frac{\sigma_x}{\sigma_n}\right) \tag{9}$$

where σ_x and σ_n are the signal and noise standard deviations, respectively. As both the position and type of the spikes are known *a priori*, it is possible to evaluate the performance of the detection analysis. The neural threshold voltage has been externally calculated in time-domain using the absolute value algorithm [14], and introduced to the system through the digital input V_{th}. In future integrations of the neural channel, this adaptive voltage threshold logic will be embedded in the channel.

The quality of the detection is illustrated by means of the probability of detection and false alarms figures [14]. The first one is given by

$$P_D = 1 - \frac{\text{number of missed spikes}}{\text{number of spikes}} \tag{10}$$

while the probability of false alarm is defined as

$$P_{FA} = \frac{\text{number of false alarms}}{\text{number of detected spikes}}. \tag{11}$$

Fig. 19 illustrates the performance of the spike detection results for different input SNRs compared to that reported by [14] and [16]. The probability of detection is higher than 80% for SNR above 2.5 dB, while, for the same range, the probability of false alarm keeps below 15%. It is worth observing the achieved performance is similar to the other approaches for SNRs above 0 dB. Further, it must be noted that the presented approach has

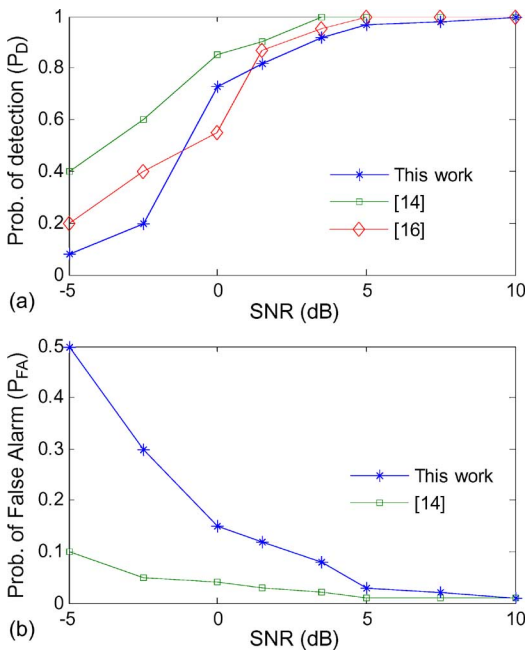


Fig. 19. Performance of the spike detection. (a) Probability of detection versus SNR. (b) Probability of false alarm versus SNR.

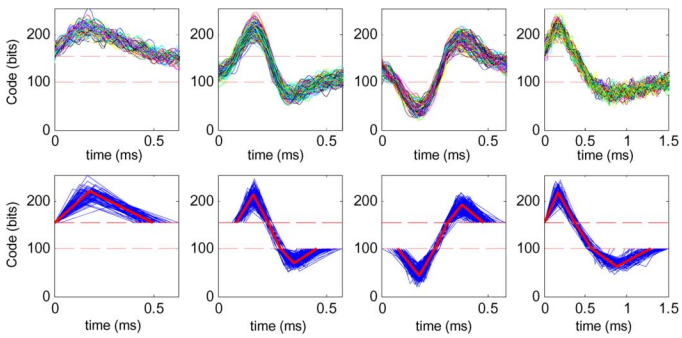


Fig. 20. Spike sorting performance of the proposed feature extraction method: original spikes (first row); detected and sorted spikes (second row).

very limited impact on silicon area thanks to the extensive use of digital-assisted analog design and building block reuse.

The performance of the proposed feature extraction method is evaluated by the accuracy with which spikes can be sorted. In order to do that, a 60-seconds synthetic neural signal with a total of 250 APs from 4 different sources was used as input. The detected spikes were classified depending on their Euclidean distances [15]; if the spike distance to a cluster falls below a certain threshold, such a spike also belongs to that cluster. The result of this classification is shown in Fig. 20. The first row plots ensembles of spikes belonging to the four different clusters, while the second row shows the shapes of their extracted features, as well as their mean. The accuracy of the presented sorting method is depicted in Fig. 21. For this analysis, only the detected spikes have been taken into account. As can be seen, for SNRs above 6 dB, the sorting error is below 10%.

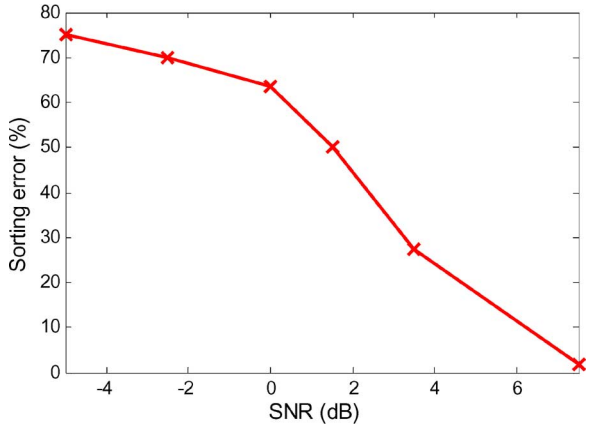


Fig. 21. Classification error of the spike sorting method from the proposed spike feature extraction.

ACKNOWLEDGMENT

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REFERENCES

[1] A. Schwartz, X. Cui, D. Weber, and D. Moran, "Brain-controlled interfaces: Movement restoration with neural prosthetics," *Neuron*, vol. 52, pp. 205–220, Oct. 2006.

[2] L. Hochberg, M. Serruya, G. Friehs, J. Mukand, M. Saleh, A. Caplan, A. Branner, D. Chen, R. Penn, and J. Donoghue, "Neuronal ensemble control of prosthetic devices by a human with tetraplegia," *Nature*, vol. 442, no. 13, pp. 164–171, Jul. 2006.

[3] M. Lebedev and A. Nicolelis, "Brain-machine interfaces: Past, present and future," *Trends Neurosci.*, vol. 29, no. 9, pp. 536–546, 2006.

[4] A. Hoogerwerf and K. Wise, "A three-dimensional microelectrode array for chronic neural recording," *IEEE Trans. Biomed. Eng.*, vol. 41, no. 12, pp. 1136–1146, Dec. 1994.

[5] C. Nordhausen, E. Maynard, and R. Normann, "Single unit recording capabilities of a 100 microlectrode array," *Brain Res.*, vol. 726, no. 1, pp. 129–140, Jul. 1996.

[6] L. Wen-Sin, Z. Xiaodan, Y. Libin, and L. Yong, "A 1-v 60-uw 16-channel interface chip for implantable neural recording," in *Proc. IEEE Custom Integrated Circuits Conf.*, 2009, pp. 507–510.

[7] C. Moo Sung, Y. Zhi, M. R. Yuce, H. Linh, and W. Liu, "A 128-channel 6 mw wireless neural recording ic with spike feature extraction and uwb transmitter," *IEEE Trans. Neural Syst. Rehabil. Eng.*, vol. 17, no. 4, pp. 312–321, 2009.

[8] R. R. Harrison, P. T. Watkins, R. J. Kier, R. O. Lovejoy, D. J. Black, B. Greger, and F. Solzbacher, "A low-power integrated circuit for a wireless 100-electrode neural recording system," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 123–133, 2007.

[9] A. M. Sodagar, G. E. Perlin, Y. Ying, K. Najafi, and K. D. Wise, "An implantable 64-channel wireless microsystem for single-unit neural recording," *IEEE J. Solid-State Circuits*, vol. 44, no. 9, pp. 2591–2604, 2009.

[10] F. Shahrokhi, K. Abdelhalim, D. Serletis, P. L. Carlen, and R. Genov, "The 128-channel fully differential digital integrated neural recording and stimulation interface," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 3, pp. 149–161, 2010.

[11] B. Gosselin, A. E. Ayoub, J. F. Roy, M. Sawan, F. Lepore, A. Chaudhuri, and D. Guitton, "A mixed-signal multichip neural recording interface with bandwidth reduction," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 3, pp. 129–141, 2009.

[12] Y. Perelman and R. Ginosar, "An integrated system for multichannel neuronal recording with spike/lfp separation, integrated a/d conversion and threshold detection," *IEEE Trans. Biomed. Eng.*, vol. 54, no. 1, pp. 130–137, 2007.
[13] S. B. Lee, H.-M. Lee, M. Kiani, U.-M. Jow, and M. Ghovanloo, "An inductively powered scalable 32-channel wireless neural recording system-on-a-chip for neuroscience applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 4, no. 6, pp. 360–371, Dec. 2010.
[14] S. Gibson, J. W. Judy, and D. Markovic, "Comparison of spike-sorting algorithms for future hardware implementation," in *Proc. Engineering in Medicine and Biology Society, 30th IEEE Annu. Int. Conf.*, 2008, pp. 5015–5020.
[15] C.-C. Peng, P. Sabharwal, and R. Bashirullah, "Neural cache: A low-power online digital spike-sorting architecture," in *Proc. Engineering in Medicine and Biology Society, 30th IEEE Annu. Int. Conf.*, Aug. 2008, pp. 2004–2007.
[16] A. Kamboh and A. Mason, "On-chip feature extraction for spike sorting in high density implantable neural recording systems," in *Proc. IEEE Biomedical Circuits and Systems Conf.*, Nov. 2010, pp. 13–16.
[17] A. Rodríguez-Pérez, J. Ruiz-Amaya, O. Guerra, and M. Delgado-Restituto, "A reconfigurable neural spike recording channel with feature extraction capabilities," in *Proc. IEEE Biomedical Circuits and Systems Conf.*, Nov. 2010, pp. 118–121.
[18] A. Rodríguez-Pérez, J. Ruiz-Amaya, J. A. Rodríguez-Rodríguez, M. Delgado-Restituto, and A. Rodríguez-Vázquez, "A power efficient neural spike recording channel with data bandwidth reduction," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 2011, pp. 1704–1707.
[19] A. Rodriguez-Perez, J. Ruiz-Amaya, M. Delgado-Restituto, M. Sawan, and A. Rodriguez-Vazquez, "A self-calibration circuit for a neural spike recording channel," in *Proc. IEEE Biomedical Circuits and Systems Conf.*, Nov. 2011, pp. 464–467.
[20] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, 2003.
[21] W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 2, pp. 136–147, 2007.
[22] Z. Xiaodan, X. Xiaoyuan, Y. Libin, and L. Yong, "A 1-v 450-nw fully integrated programmable biomedical sensor interface chip," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1067–1077, 2009, 0018-9200.
[23] V. Majidzadeh, A. Schmid, and Y. Leblebici, "Energy efficient low-noise neural recording amplifier with enhanced noise efficiency factor," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 3, pp. 262–271, Jun. 2011.
[24] C. Qian, J. Parramon, and E. Sanchez-Sinencio, "A micropower low-noise neural recording front-end circuit for epileptic seizure detection," *IEEE J. Solid-State Circuits*, vol. 46, no. 6, pp. 1392–1405, Jun. 2011.
[25] P. Mohseni and K. Najafi, "A fully integrated neural recording amplifier with dc input stabilization," *IEEE Trans. Biomed. Eng.*, vol. 51, no. 5, pp. 832–837, 2004.
[26] B. Gosselin, M. Sawan, and C. A. Chapman, "A low-power integrated bioamplifier with active low-frequency suppression," *IEEE Trans. Biomed. Circuits Syst.*, vol. 1, no. 3, pp. 184–192, 2007.
[27] Z. Wei, L. Hongge, and Z. Youguang, "A low-noise integrated bioamplifier with active dc offset suppression," in *Proc. IEEE Biomedical Circuits and Systems Conf.*, 2009, pp. 5–8.
[28] J. Ruiz-Amaya, A. Rodriguez-Perez, and M. Delgado-Restituto, "A review of low-noise amplifiers for neural applications," in *Proc. 2nd Circuits and Systems for Medical and Environmental Applications Workshop*, 2010, pp. 1–4.
[29] S. Rai, J. Holleman, J. N. Pandey, F. Zhang, and B. Otis, "A 500 uw neural tag with 2 uvrms afe and frequency-multiplying mics/ism fsk transmitter," in *Proc. IEEE Int. Solid-State Circuits Conference—Dig. Tech. Papers*, 2009, pp. 212–213, 213a.
[30] J. Ruiz-Amaya, M. Delgado-Restituto, and A. Rodriguez-Vazquez, "Accurate settling-time modeling and design procedures for two-stage miller-compensated amplifiers for switched-capacitor circuits," *IEEE Trans. Circuits and Systems I, Reg. Papers*, vol. 56, no. 6, pp. 1077–1087, Jun. 2009.
[31] J. Ruiz-Amaya, M. Delgado-Restituto, and A. Rodríguez-Vázquez, "Transistor-level synthesis of pipeline analog-to-digital converters using a design-space reduction algorithm," *IEEE Trans. Circuits and Systems I, Reg. Papers*, vol. 58, no. 12, pp. 2816–2828, Dec. 2011.
[32] M. S. J. Steyaert and W. M. C. Sansen, "A micropower low-noise monolithic instrumentation amplifier for medical purposes," *IEEE J. Solid-State Circuits*, vol. 22, no. 6, pp. 1163–1168, 1987.
[33] M. D. Scott, B. E. Boser, and K. S. J. Pister, "An ultralow-energy adc for smart dust," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1123–1129, 2003.
[34] A. Agnes, E. Bonizzoni, P. Malcovati, and F. Maloberti, "A 9.4-enob 1 v 3.8 uw 100 ks/s sar adc with time-domain comparator," in *Proc. IEEE Int. Solid-State Circuits Conf., Dig. Tech. Papers*, 2008, pp. 246–610.
[35] N. Verma and A. P. Chandrakasan, "An ultra low energy 12-bit rate-resolution scalable sar adc for wireless sensor nodes," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1196–1205, 2007.
[36] S. Gambini and J. Rabaey, "Low-power successive approximation converter with 0.5 v supply in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2348–2356, 2007.
[37] A. Rodriguez-Perez, M. Delgado-Restituto, F. Medeiro, and A. Rodriguez-Vazquez, "A low-power reconfigurable adc for biomedical sensor interfaces," in *Proc. IEEE Biomedical Circuits and Systems Conf.*, Nov. 2009, pp. 253–256.
[38] R. Kier, R. Harrison, and R. Beer, "An mdac synapse for analog neural networks," in *Proc. Int. Symp. Circuits and Systems*, May 2004, vol. 5, pp. V-752–V-755.
[39] C. Gabriel, S. Gabriel, and E. Corthout, "The dielectric properties of biological tissues," *Phys. Med. Biol.*, vol. 41, no. 11, pp. 2231–2293, 1996.
[40] R. Quiroga, Z. Nadasdy, and Y. Ben-Shaul, "Unsupervised spike detection and sorting wavelets and superparamagnetic clustering," *Neural Comput.*, vol. 16, pp. 1661–1687, 2004.

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