Design of a Compact and Low-Power TDC for an Array of SiPM's in 110nm CIS Technology

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***Abstract*—Silicon photomultipliers (SiPMs) are meant to substitute photomultiplier tubes in high-energy physics detectors and nuclear medicine. This is because of their —to name a few interesting properties— compactness, lower bias voltage, tolerance to magnetic fields and finer spatial resolution. SiPMs can also be built in CMOS technology. This allows the incorporation of active quenching and recharge schemes at cell level and processing circuitry at pixel level. One of the elements that can lead to finer temporal resolutions is the time-to-digital converter (TDC). In this paper we describe the architecture of a compact TDC to be included at each pixel of an array of SiPMs. It is compact and consumes low power. It is based on a voltage controlled oscillator that generates multiple internal phases that are interpolated to provide time resolution below the time delay of a single gate. Simulation results of a 11b TDC based on a 4-stage VCRO in 110nm CIS technology yield a time resolution of 80.0ps, a DNL of ±0.28 LSB, a INL ±0.52 LSB, and a power consumption of 850μW.**

I. Introduction

Several imaging techniques in high-energy physics and nuclear medicine rely on two measurements: the accurate timestamp of the arrival of high-energy photons in a piece of scintillating material and the level of energy involved [1]. A silicon photomultiplier (SiPM) [2] can be employed to this end. By using a time-to-digital converter (TDC), it is possible to determine the time of the impact. By measuring the magnitude of the SiPM current, one can trace the amount of visible photons generated at the scintillator as a proxy of the energy carried by the original high-energy photon. Alternatively, in the case of a digital SiPM [3], instead of measuring the output current, voltage pulses at the SiPM output can be directly counted. In any case, if the magnitude of the impact exceeds a certain threshold, time measurement is triggered.

In order to accurately timestamp the detection of the high-energy photon impact a time-to-digital converter (TDC) is needed [4]. The challenges to built a TDC are in the time resolution which, in principle, is determined by technology. The minimum detectable delay is that of an inverter. If finer resolutions are required, techniques like pulse stretching [5], Vernier delay lines [6], time amplification [7] or multi-path Gated Ring Oscillator (GRO) [8] can be employed. However, the principal drawback of these architectures are the large area and power consumption. There are cases in which specifications demand the incorporation of in-pixel TDCs. For instance, if a high frame rate is required, events need to be timestamped in parallel. For that a TDC with a high resolution but also low area occupation and power consumption is needed. TDCs based on a voltage controlled ring oscillator (VCRO) offer a good trade off between time resolution, area and power. They can be found in a large range of applications, like all-digital phase locked loops (ADPLL) for communications [9]; time-of-flight (ToF) estimation in telemetry [10], [11] and particle identification; and bio-medicine, including fluorescence-lifetime imaging microscopy (FLIM) [12] and positron emission tomography (PET) [13].

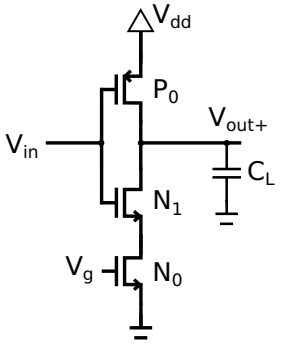

Fig. 1. Current-starved inverter. C_L is the capacitive load.

In this paper we are presenting the design of a TDC in which the building block of the VCRO has been tailored to render a good compromise between time resolution, area and power consumption. Every design decision is oriented towards the maximization of the oscillation frequency, reducing resistive and capacitive parasitics on the signal path. The paper is organized as follows. In Section II the architecture is discussed. An analysis of different stages is presented in Section III. Simulation results are provided and analyzed in Section IV. Finally, conclusions are summarized in Section V.

II. TDC architecture

For a given technology, the selection of the architecture determines the compromise between time resolution, area and power consumption. We have designed a TDC based on a VCRO because of several reasons. First of all, as the oscillation frequency is a function of the delay of individual stages of the oscillator, the time resolution can be controlled by controlling the stage delay (T_d). That can be done through a current-starved inverter like that shown in Fig. 1. The main advantage of current starving is the possibility to adjust the stage delay to a reference value through a control loop, which

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will reduce the effects of PVT variations [14]. Secondly, the small area footprint of this architecture makes it possible to integrate the TDC within a pitch size as small as 50μm$\times 50\mu$m [15]. In the third place, as the current employed at the stages of the oscillator is regulated by a voltage, power consumption can be reduced if a decrease on the oscillation frequency is not critical. Additionally, if great linearity is required, a linearly extended architecture like the proposed in [4] could be used.

Fig. 2 displays a simplified block diagram of the TDC. The controller block generates the internal signals that drive the rest of the circuit, for instance starting and stopping oscillation, resetting, enabling the sample phase, etc. Once the VCRO is stopped, the ripple counter retains the number of oscillations realized by the VCRO, constituting the coarse conversion (8b) of the time period measured. Simultaneously, the internal phases of the VCRO are sampled at the regenerative latches. These phases are encoded into additional 3b, that provide the fine conversion. Notice that unlike a single-ended ring oscillator where there must be an odd number of stages, in differential and pseudo-differential ring oscillators the number of stages can be even. In order to fulfill Barkhausen criteria, however, a wire inversion has to be placed [16].

III. Ring Oscillator and Delay Stage Topology

A pseudo-differential approach has been chosen over single-ended and differential approaches because of the following reasons. The output swing of the pseudo-differential stage, and also of a single-ended stage built with a CMOS inverter, is the full range supply from V_{DD} to V_{SS}. In the case of a true differential stage, this voltage excursion is smaller. Rail-to-rail voltage excursions improve jitter [16], therefore the pseudo-differential delay stage is better for our purpose. Additionally, differential stages, either true- or pseudo-differential, have better rejection to interference coupling from supply/substrate than single-ended architectures [16]. Finally, the power consumption of a pseudo-differential, and of a single-ended, ring oscillator is relatively low as there is only one stage transitioning in each moment, while in a differential ring oscillator each stage consumes the bias current.

The next step in the design of the oscillator is the selection of the topology of the elementary stage. Different topologies have been proposed in the literature [15], [16]. An analytical study is required to select the most suitable topology for the target application, that is, low timing resolution, area and power consumption. In order to do that, the transfer function has been obtained for the different stages. Current starving has been excluded from the analysis for simplification. An additional difficulty for this approach is that while the small signal analysis requires an operating point, the circuit during oscillation is being polarized across the whole supply range. Fig. 3 shows a pseudo-differential stage with cross-coupled inverters. Delay inverters (I_d) have to be stronger than regenerative inverters (I_c) not to create a latch. Fig. 4 shows a pseudo-differential stage with cross-coupled PMOS.

Table I summarizes the small signal transfer function and the gain-bandwidth product (GBW) for the two pseudo-differential stages. These analytical expressions show that the unity-gain bandwidth is higher in the pseudo-differential stage with cross-coupled inverters, because of the contribution of PMOS transistors in the GBW product. Hence, the maximum frequency that can be sustained by this stage is higher. However, the principal advantage of the pseudo-differential stage with cross-coupled PMOS is lower area and layout complexity, mainly because of the lower number of current-starved transistor per stage.

TABLE I
Comparison of the transfer function of pseudo-differential stages

	PD Cross PMOS	PD Cross Inverter
$r_o[\Omega]$	$r_N//r_P$	$(r_N//r_P)_d//(r_N//r_P)_c$
$A(s)[-]$	$\frac{\frac{gm_N\cdot r_o}{1-gm_P\cdot r_o}}{1+\frac{s\cdot r_o\cdot C_L}{1-gm_P\cdot r_o}}$	$\frac{\frac{(gm_N+gm_P)_d\cdot r_o}{1-(gm_N+gm_P)_c\cdot r_o}}{1+\frac{s\cdot r_o\cdot C_L}{1-(gm_N+gm_P)_c\cdot r_o}}$
$GBW[Hz]$	$\frac{gm_N}{2\cdot\pi\cdot C_L}$	$\frac{(gm_N+gm_P)_d}{2\cdot\pi\cdot C_L}$

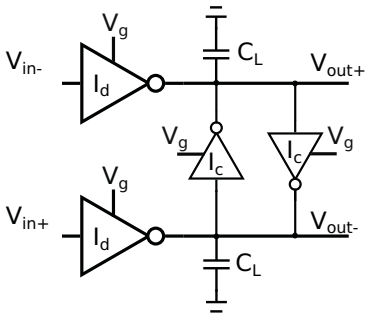

Fig. 3. Pseudo-differential stage with cross-coupled inverters. Note that all inverters are current-starved inverters, V_g is used to control the delay. C_L is the capacitive load of the next stage.

In this work, as the lowest timing resolution is required, pseudo-differential stage with cross-coupled inverters has been chosen over the pseudo-differential stage with cross-coupled PMOS, this decision will be support by simulation results in section IV. The increment in the number of transistors is justified by the timing resolution improvement.

IV. Pre-layout Simulation Results

The TDC simulated is implemented with a 4-stage VCRO, each stage is pseudo-differential with cross-coupled inverters. The dimensions of delay inverters (I_d) of pseudo-differential stage with cross-coupled inverters are $(W/L)_p = 3.6/0.11\mu$m and $(W/L)_n = 1.1/0.11\mu$m (16 times stronger than cross-coupled inverters (I_c)). The dimensions of pseudo-differential stage with cross-coupled PMOS are $(W/L)_p = 3.2/0.11\mu$m and $(W/L)_n = 4.0/0.11\mu$m. The pre-layout verification of the circuit functionality begins with the characterization of timing resolution and power consumption. Fig. 5 represents the timing resolution (T_d) of the TDC as a function of control voltage (V_g). The timing resolution of the VCRO with cross-

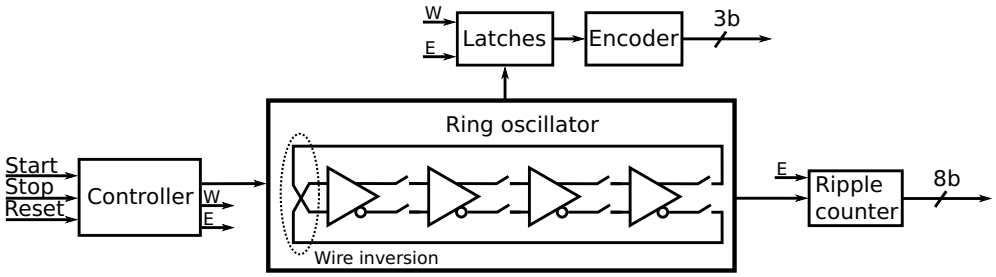

Fig. 2. Simplified block diagram of the TDC.

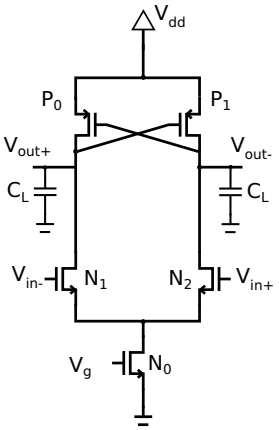

Fig. 4. Pseudo-differential stage with cross-coupled PMOS transistors. C_L is the capacitive load of the next stage.

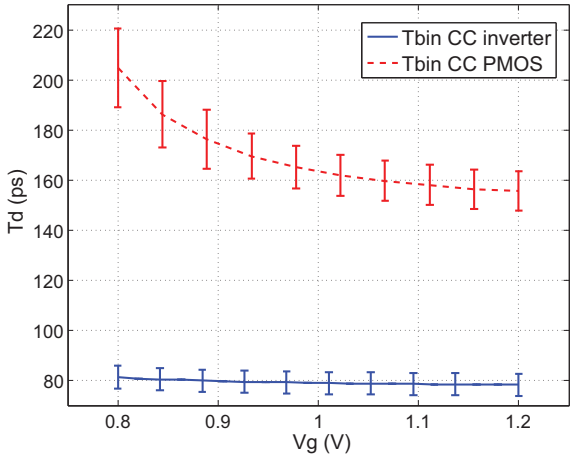

Fig. 5. Timing resolution as a function of control voltage (V_g) for 4-stage VCRO with pseudo-differential with cross-coupled inverters (solid line) and pseudo-differential with cross-coupled PMOS (dashed line). Monte Carlo simulations were carried on to get error bars.

coupled inverters is around 80.0ps with a standard deviation of $\pm$4.3ps, while the VCRO with cross-coupled PMOS has a timing resolution of 170.0ps with a standard deviation of $\pm$10.0ps. The lack of linearity could be a problem in some applications (like ADPLL), but in this target application is not critical. Better timing resolutions (50.0ps) are achieved with 130nm technology in [15]. This result is explained by the fact that only high voltage threshold devices were used here, because no more devices are available in this technology. This means that the overdrive voltage ($V_{dd} - V_{Th}$) during the stage transition is reduced, and hence, the current ($I_d \propto (V_{dd} - V_{Th})$) available to charge and discharge the capacitive load (C_L) is lower.

Fig. 6 depicts the power consumption of the TDC, while the ring is oscillating, as a function of control voltage (V_g). As expected the power consumption is linearly related to the timing resolution. This result is slightly higher than the reported in [13], where the power consumption is 790μA.

In Fig. 7 it is shown the transfer function of the TDC from 0s to 20ns (i.e., when the time difference between the start and the stop signal is sweep from 0s to 20ns), black data represent the encoder output, blue data show the ripple counter output and red data represent the TDC output.

Finally, Fig. 8 illustrates the DNL and INL of the TDC from 0s to 20ns, as can be seen the DNL is in the range of

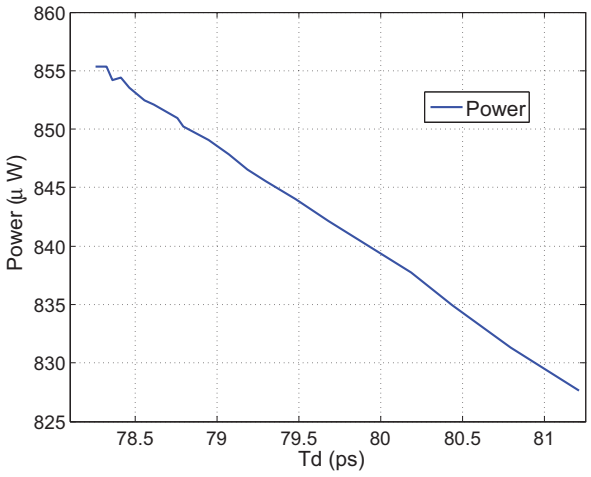

Fig. 6. Power consumption, while the ring is oscillating, as a function of timing resolution.

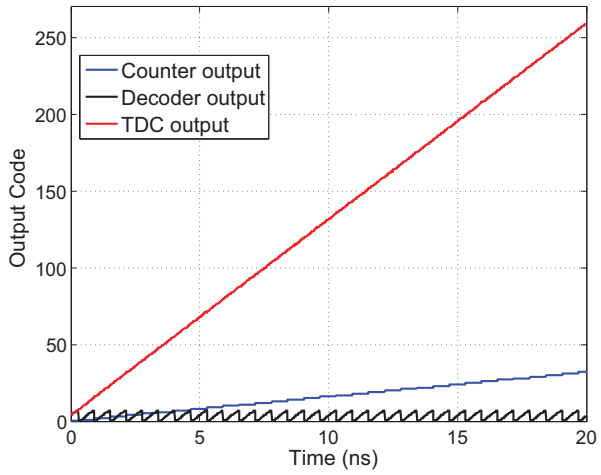

Fig. 7. TDC transfer function. The black data represents the encoder output (3b), blue data represents the ripple counter output (8b), and red data shows the TDC output (11b) as a combination of the encoder and the ripple counter output.

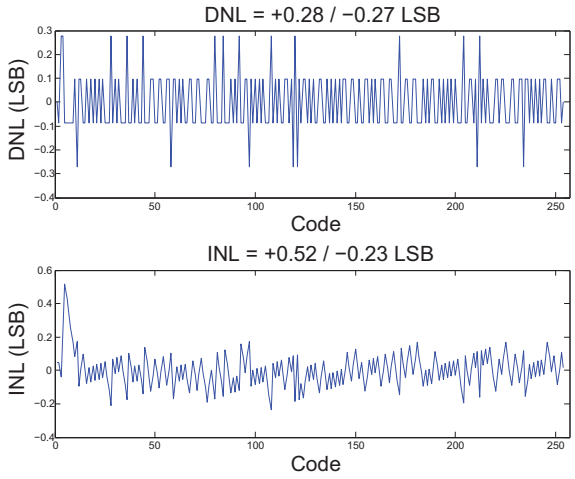

Fig. 8. (top) DNL and (bottom) INL of the TDC from 0s to 20ns.

±0.28 LSB, since the maximum DNL is lower than 1 LSB, there is no missing code. Moreover, INL is in the range ±0.52 LSB. These results are better than those reported by [15], where DNL was ±0.4 LSB and INL was ±1.4 LSB. However, it has to be noted that these results are based on pre-layout simulation, post-layout results are expected to be worse.

V. Conclusion

In this paper the description of a compact TDC to be integrated at each pixel of an array of SiPMs has been done. The voltage controlled ring oscillator architecture was chosen because it fulfills the trade off between timing resolution, area and power consumption. Pseudo-differential stage was selected as delay stage due to its good rejection to interference coupling from supply/substrate and its rail-to-rail voltage excursions. The GBW product was chosen as an analytic metric to compare different stages. Doing so, it is possible to select the stage that provide the highest oscillation frequency (the lower timing resolution). The simulation results has shown a timing resolution that can be tunned from 81.0ps to 78.0ps with accuracy of ±0.28 LSB DNL and ±0.52 LSB INL. The power is consumption around 850μW.

Acknowledgment

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