5x5 SPAD Matrices for the Study of the Trade-offs between Fill Factor, Dark Count Rate and Crosstalk in the Design of CMOS Image Sensors

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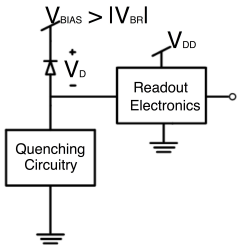
***Abstract*—CMOS Single Photon Avalanche Diodes (SPADs) are a dedicated type of photodetectors that are attracting increasing interest. Crosstalk and fill factor are magnitudes that become important when dealing with arrays of SPADs. There are trade-offs that involve these two magnitudes and dark count rate (DCR) which are of great interest for the implementation of image sensors. A set of 5x5 matrices of SPADs with different sizes and shapes is designed to study the relationships between FF, crosstalk and DCR, and conceive an accurate behavioural model of SPAD arrays. The testchip is fully operative and preliminary experimental results are presented.**

I. Introduction

Single Photon Avalanche Diodes (SPADs) are p-n junctions reverse biased at a voltage larger than its breakdown voltage (V_{BR}) [1]. The resulting high electric field in the depletion region causes the amount of photogenerated carriers in this zone to increase exponentially in time and a macroscopic current can be measured in practice from a single incoming photon. To use these devices as photodetectors it is necessary to extinguish the avalanche and reset the original bias conditions to enable the detection of new incoming photons [2]. The additional circuitry used with such purpose is the quenching circuit [3].

Although the trend in the design of CMOS SPADs is to go to smaller technological nodes [4] –which a priori favors the fill factor (FF)–, the increasing performance requirements imply that additional electronics must be integrated, reducing the FF. Due to their simplicity, a way to reduce the area occupied by the integrated electronics is the use of passive quenching circuits (PQC) instead of active (AQC) or mixed (MQC) ones [3]. However, SPADs with active recharge (MQC) return abruptly to their initial biasing conditions while the recharge is slower in PQCs (see Fig. 1). As a result, any incident photon –or carriers that are thermally generated or released by internal traps– could retrigger the device before the recharge phase ends. Some adverse effects of this retriggering phenomenon are the variation of the dead time (t_{dt}, time in which the SPAD is not sensitive to the arrival of new photons) or the reduction of the photon detection efficiency (PDE) [5].

Another way to improve the FF is to increase the area of the SPAD regarding the electronics within the array cell, but this results in an unwanted increase of DCR (frequency of the avalanche events caused by non photogenerated carriers) [6].



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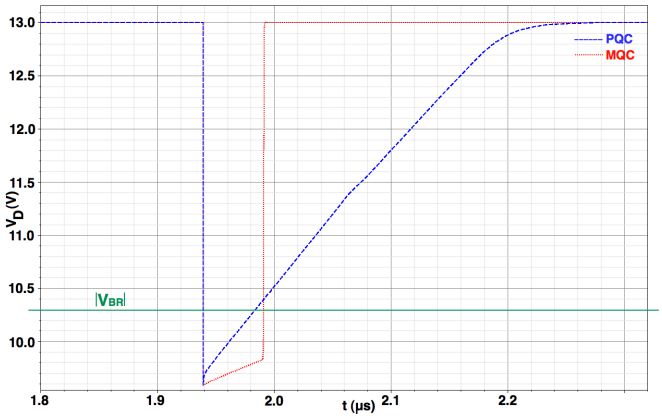

(b)

Fig. 1. (a) Conceptual diagram of the SPAD and its accompanying circuitry. (b) Transient response of the SPAD voltage during both the quenching and the recharge phases for passive and mixed quenching circuits.

Additionally, when implementing CMOS SPAD arrays, the reduction of the pixel pitch and the growth of the SPAD area would be negative in terms of crosstalk, that represents the probability of having a spurious avalanche in a pixel caused by a photon detection or dark count in a neighboring cell [6].

In this work we present a testchip for studying the existing trade-offs between FF, DCR and crosstalk, which are key when designing CMOS SPAD-based image sensors. To this end, a precise extrapolated model of the behaviour of SPAD arrays in terms of these magnitudes will be developed.

II. Testchip Description

A standard CMOS 180nm process has been chosen for the design of the SPADs and their quenching circuits, together

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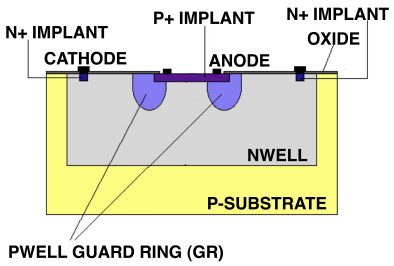

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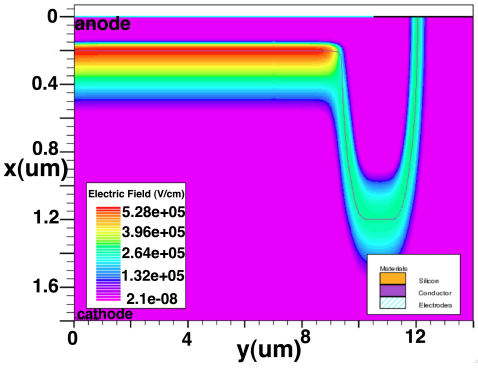

(b)

Fig. 2. (a) Cross section of the SPAD, with the p-well guard ring to avoid PEB. (b) Simulation in ATLAS of the SPAD structure.

with the accompanying test circuitry.

A. SPADs Physical Structure

A variety of SPAD structures has been published [6] to avoid premature edge breakdown (PEB) –a spurious avalanche that preferably takes place at the edges of the p-n interface of the device and reduces its sensitivity [7]. Among the possibilities, due to the limited layer availability and the design rules of the selected standard CMOS process, a SPAD structure has been chosen that includes a guard ring using a lower doped p-well around the p^+ region (see Fig. 2a).

The physical structure of the SPADs has been designed and validated through 2D simulations in ATLAS [8]. For this purpose, the dimensions of the implanted areas have been extracted from the technology files and the diode model parameters of the process, whereas the doping concentrations have been estimated from previous experimental results in the same technological process [9], [10]. Fig. 2b shows the efficiency of the guard ring for lowering the electric field at the edges of the active region.

B. SPADs Geometry

Fig. 3 shows the top view of the three different SPAD shapes that have been included in the testchip to obtain information about their relative performance in terms of DCR; namely, circular, cigar-shaped and ellipsoidal. In [11], a cigar-shaped structure is proposed as an interesting alternative to implement large-area SPADs without having restrictive increases of the DCR, due to the larger gettering efficiency of the geometry

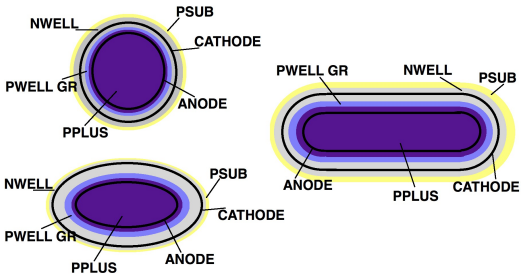

Fig. 3. Top view of the three SPAD geometries included in the testchip.

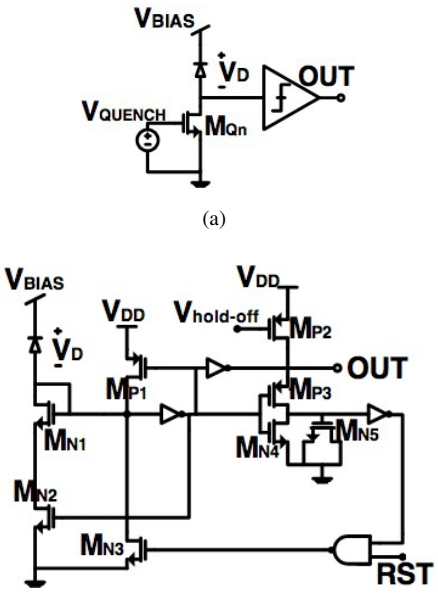

Fig. 4. (a) Passive quenching circuit. (b) Mixed quenching circuit.

to decrease the defect density in the active region [12]. As an extension of this concept, we propose the ellipse due to its resemblance to the cigar-shape and its smoother profile.

C. Crosstalk Characterization

Besides dark counts, crosstalk is another source of noise to be considered when working with arrays of SPADs. It can be caused by two different mechanisms:

- Optical crosstalk: During an avalanche process some secondary photons can be emitted from the SPAD due to electroluminiscence [13]. These photons can propagate through the chip and be detected by neighboring pixels in the array, resulting in a non-desired avalanche pulse.
- Electrical crosstalk: It is due to photons absorbed beyond the active area of the device. These photons generate free carriers that can diffuse laterally to different depletion regions where they could cause an avalanche [7].

The first one depends on the distance between SPADs and also on their size, since the parasitic capacitance influences the number of carriers flowing during the avalanche [7]. Its effect can thus be reduced by decreasing the SPAD size or

increasing their separation in the array, but at the cost of a loss of FF.

The 5x5 matrices of SPADs included in the testchip allow us to characterize the dependence of crosstalk on distance and on SPAD size for modeling purposes. Due to constraints imposed by the experimental setup, a 60-μm pixel pitch has been chosen to enable the individual illumination of each cell.

D. Quenching Circuitry

The aim of quenching circuits is to extinguish the SPADs avalanche current and return them to their bias conditions, allowing the detection of new incident photons. Two different alternatives have been included in the testchip (see Fig. 4):

- PQC with an nMOS transistor operating in the triode region and a comparator with programmable threshold for readout purposes.
- MQC with passive quenching and active recharge, in which t_{dt} can be widely adjusted by varying $V_{hold-off}$.

The electrical design of both quenching circuits in Fig. 4 has been performed using the behavioural model of SPADs proposed in [14] and extended in [10], which includes the DCR as a Poisson distributed phenomenon. Behavioural model parameters have been fine tuned, taking advantage of previous experimental results in the same process [10].

E. Testchip Composition

The testchip has been designed in a 1.8-V 180-nm standard CMOS process, occupies an area of 1.5×1.5mm^2 and comprises:

- nine 5×5 SPAD arrays for the characterization of crosstalk for different sensor shapes, sizes and quenchings.
- four individual SPAD structures for studying their transient operation and measuring their IV-characteristic.
- a 1×8 array to examine alternative test configurations.

Table I summarizes the different test structures included in the testchip. Note that not only the shape and size of the SPADs vary, but also the minor to major axis ratio of cigar and ellipse shapes to check the role of this parameter. Fig. 5 shows the layout of the whole chip and highlights its main parts.

TABLE I
SUMMARY OF THE INCLUDED TEST STRUCTURES.

	Test structure	Shape	Active area (μm^2)	Minor to major axis ratio	Quenching circuit
5×5 Arrays	#1	Circle	155	1	PQC
	#2	Circle	350	1	PQC
	#3	Ellipse	350	0.62	PQC
	#4	Circle	350	1	MQC
	#5	Ellipse	155	0.62	PQC
	#6	Ellipse	350	0.28	MQC
	#7	Cigar	350	0.5	MQC
	#8	Cigar	155	0.39	MQC
	#9	Ellipse	350	0.62	MQC
1×8 Array	#10	Circle	350	1	MQC
	#11	Cigar	113	0.39	PQC
	#12	Circle	40	1	MQC
	#13	Ellipse	40	0.37	MQC
	#14	Cigar	40	0.41	MQC
	#15	Ellipse	155	0.34	PQC
	#16	Cigar	155	0.39	PQC
	#17	Cigar	40	0.22	PQC
Individual Structures	#18	Circle	155	1	–
	#19	Cigar	155	0.42	–
	#20	Ellipse	155	0.52	–
	#21	Ellipse	155	0.6	–

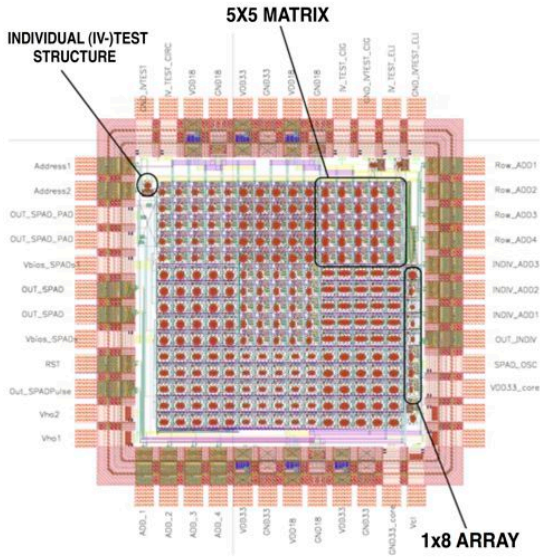

Fig. 5. Layout of the testchip.

III. EXPERIMENTAL RESULTS

The testing of the chip is in progress at the time of writing this paper. Some results of the measurements performed up to this moment are presented in this section for single devices.

In order to get the breakdown voltage and the IV-characteristic, the HP4155A semiconductor parameter analyzer has been utilized. Fig. 6 (left) illustrates the variation of the current through the SPAD versus the bias voltage for two devices with different shape (circular and ellipsoidal) and size (14 and 7μm, respectively). It can be seen that for currents around 200μA (*latching* current), the avalanche is no more self-sustained and the current drops sharply to zero.

On the right side of Fig. 6, the variation of the breakdown voltage with temperature is represented. Theory [14] tells us that the breakdown voltage of SPADs vary with temperature:

$$V_{BR} = V_{B0} \cdot [1 + \beta \cdot (T - T_0)] \quad (1)$$

where V_{B0} is the breakdown voltage at room temperature, and β is the temperature coefficient. In this case, the values of this coefficient are β_{CIR}=6.82×10^{-4}K^{-1} and β_{ELL}=6.79×10^{-4}K^{-1}.

Fig. 7 shows the dependence of the SPAD resistance with temperature. This magnitude is comprised of the space-charge resistance, the resistance of the neutral regions, and the ohmic resistance from the contact to the neutral region of the junction [5]. The SPAD resistance will be studied in detail because it is very important to know the current flowing through the device

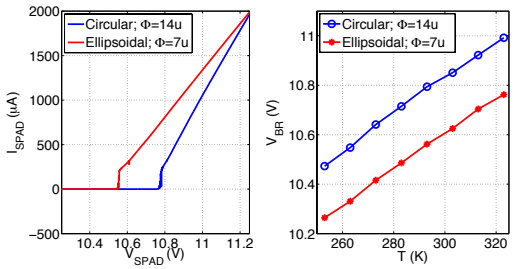

Fig. 6. IV-characteristic (left) and breakdown voltage variation with temperature (right) of the circular (Φ=14μm) and ellipsoidal (Φ=7μm) SPADs.

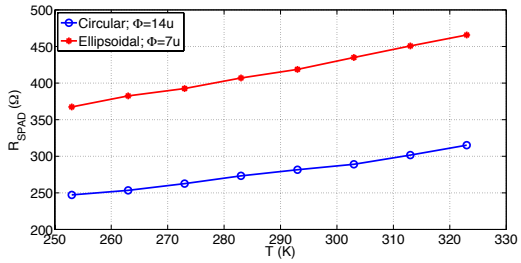

Fig. 7. SPAD resistance dependence for the circular (Φ=14μm) and ellipsoidal (Φ=7μm) devices.

when it comes to design. These results show a similar behavior for both SPADs and also that the smaller the area, the larger resistance of the SPAD, as expected [5].

Dark count rate versus the excess bias voltage is represented in Fig. 8 for the test structures with PQC included in the 1x8 array. In the range of excess bias voltages swept, the behavior in all the cases is quite linear. Moreover, the cigar and ellipsoidal SPADs with the same size (Φ=14μm) present the same levels of dark counts. It is still under experimental validation if for larger active area sizes and comparing with the circular one, these two shapes represent an improvement in terms of the device noise.

Finally, the measurement of the PDE has been performed in the single-photon regime (incident optical power in the nW/mm^2 range). As an orientation, its maximum value for the circular SPAD (Φ=14μm) is 4.2% for V_{exc}=1V at 540nm.

IV. Conclusions

Dark count rate, crosstalk and fill factor are key magnitudes when designing CMOS SPAD arrays. A set of distinct test structures is presented for the study of the existing trade-offs between them. This comparative study will provide important information about the design considerations to be taken into account by CMOS image sensors designers and towards the realization of a complete model for SPAD simulation. Moreover, the investigation of different shapes for the SPADs that could allow an increase in their sizes without prohibitively large increases in the DCR is of great importance since this would mean larger FF and photon sensitivity. The fabricated testchip is fully operative and its complete experimental characterization will be available at the time of the conference.

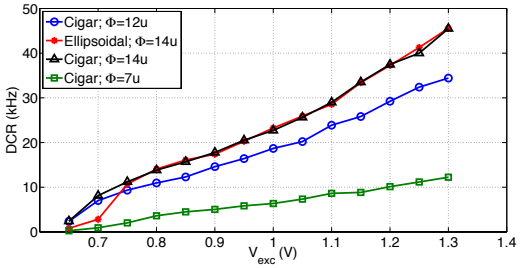

Fig. 8. Dark count rate variation with the excess bias voltage at room temperature. The test structures are those with PQC into the 1x8 array.

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References

[1] F. Zappa *et al.*, "Principles and Features of Single Photon Avalanche Diode Arrays," *Sensors and Actuators A: Physical*, vol. 140, pp. 103–112, Oct. 2007.

[2] A. Dalla Mora *et al.*, "Single-Photon Avalanche Diode Model for Circuit Simulations," *IEEE Photonics Technology Letters*, vol. 19, pp. 1922–1924, Dec. 2007.

[3] A. Gallivanoni, I. Rech, and M. Ghioni, "Progress in Quenching Circuits for Single Photon Avalanche Diodes," *IEEE Trans. on Nuclear Science*, vol. 57, pp. 3815–3826, Dec. 2010.

[4] M. A. Karami, *Deep-submicron CMOS Single Photon Detectors and Quantum Effects*. PhD thesis, Technische Universiteit Delft, 2011.

[5] H. Finkelstein, *Shallow-Trench Isolation Bounded Single-Photon Avalanche Diodes in Commercial Deep Submicron CMOS Technologies*. PhD thesis, University of California, San Diego, 2007.

[6] G. F. Dalla Betta *et al.*, *Avalanche Photodiodes in Submicron CMOS Technologies for High-Sensitivity Imaging*, ch. 11 in Advances in Photodiodes, pp. 225–248. InTech, 2011.

[7] P. Seitz and A. J. P. Theuwissen, *Single-Photon Imaging*. Springer Series in Optical Sciences, 2011.

[8] http://www.silvaco.com/.

[9] B. Blanco-Filgueira, P. López, and J. B. Roldán, "Experimental characterization of peripheral photocurrent in cmos photodiodes down to 65nm technology," *Semiconductor Science and Technology*, vol. 28, Apr. 2013.

[10] M. Moreno *et al.*, "CMOS SPADs Selection, Modeling, and Characterization Towards Image Sensors Implementation," in *Proc. of the 19th Intl. Conf. on Electronics, Circuits and Systems (ICECS)*, pp. 332–335, Dec. 2012.

[11] B. Nouri, M. Dandin, and P. Abshire, "Large-area low-noise single-photon avalanche diodes in standard cmos," in *IEEE Sensors*, Oct. 2012.

[12] A. Zanchi *et al.*, "On-chip probes for silicon defectivity ranking and mapping," in *Proc. of the 38th IEEE International Reliability Physics Symposium*, pp. 370–376, 2000.

[13] R. Newman, "Visible light from a silicon p-n junction," *Physical Review*, vol. 100, no. 2, pp. 700–703, 1955.

[14] G. Giustolisi, R. Mita, and G. Palumbo, "Behavioral Modeling of Statistical Phenomena of Single-Photon Avalanche Diodes," *International J. of Circuit Theory and Applications*, vol. 40, pp. 661–679, July 2012.