An Experimentally-Validated Verilog-A SPAD Model Extracted from TCAD Simulation

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***Abstract*— Single-photon avalanche diodes (SPAD) are photodetectors with exceptional characteristics. This paper proposes a new approach to model them in Verilog-A HDL with the help of a powerful tool: TCAD simulation. Besides, to the best of our knowledge, this is first model to incorporate a trap-assisted tunneling mechanism, a cross-section temperature dependence of the traps, and the self-heating effect. Comparison with experimental data establishes the validity of the model.**

Keywords—CMOS; Verilog-A; TCAD simulation; single-photon avalanche diode (SPAD); device simulation.

I. Introduction

Silicon-based single-photon avalanche diodes (SPADs) are semiconductor devices with the ability of detecting the arrival of isolated photons. They have been initially developed as a cheaper, magnetic-field-compatible replacement for photomultiplier tubes. They can be employed either to sense low-intensity luminous signals, by photon counting, or to timestamp the arrival these photons, enabling the estimation of their time-of-flight (ToF). Nowadays they can be built in CMOS technology, what allows incorporating functionality and opens the door to many more applications. Apart from depth and proximity sensors, SPADs are finding suitable application scenarios in fluorescence life-time microscopy (FLIM) and positron emission tomography (PET).

Basically, a SPAD is a p-n junction biased above its breakdown voltage. In these conditions, anything can trigger a self-sustained avalanche like, for instance, a photon absorbed in the space-charge region. Over the last years there has been an interest to develop an accurate model of this device. However, its electrical characteristics and noise behavior have proven to be difficult to emulate. The first model of the SPAD using Verilog-A [1], solved convergence problems from previous SPICE models [2], and introduced the voltage dependence of the junction capacitance. This model, however, lacked some important statistical phenomenon, like dark count noise (DCR) and after-pulsing probability (AP). Later on, DCR and AP were included by [3][4]. However, band-to-band tunneling (BTBT), and the fact that AP has a strong dependence on the time since the previous avalanche event, was not considered in [3]. Another relevant contribution to DCR, trap-assisted tunneling (TAT), was not included in any of them.

Our approach to SPAD modeling is based in exhaustive simulation with TCAD tools. In a first step, the fabrication process of the SPAD is simulated and a static characterization is carried out over the TCAD description of the device. This permit the inclusion of effects associated to complex structures, namely the guard ring, the second junction between the deep n-well and the substrate, etc. In a second step, these simulation results are employed to build the model in Verilog-A[1]. Additional components in the device description are incorporated as improvements over previous models, such as a different BTBT description than that in [4], using Kao's correction [5] to Hurkx's BTBT model [6] and the inclusion of Webster's dark count spectroscopy results [7]. Also, this is the first SPAD model that considers the trap-assisted tunneling mechanism and quantifies the contribution of the self-heating effect and the temperature dependence of the cross-section of the traps and deep-level traps.

II. TCAD Simulation

A. Simulated device

TCAD simulations have been conducted using Silvaco TCAD tools. The basic device structure consists in a 12 µm diameter active area device with a guard ring of low-doped p-well material, or T-Well, around the central p+/deep-n-well breakdown region, to avoid edge-junction breakdown.

The device fabrication process flow has been simulated with Athena, SSuprem4 and Elite tools, belonging to the Silvaco TCAD suite. This consists in simulated layer implantations with ion beams and ion diffusion processes through a silicon lattice, so that the final device structure can be a realistic approach to a real SPAD with doping profiles that match that of a standard CMOS 0.18µm technology.

B. Simulated tests

Process simulation have been carried out with Atlas as part of Silvaco TCAD suite. This simulation include carrier mobility models (ANALYTIC, FLD.MOB), recombination models (CONSRH, AUGER), carrier statistics models (FERMI, BGN) and impact ionization models (SELB), all necessary to describe the physical phenomena present in the operation of a SPAD [8]. The first simulations were intended to characterize quantum

[1]The Verilog-A model can be found at http://www2.imse-cnm.csic.es/icaveats/SPAD_12um.va

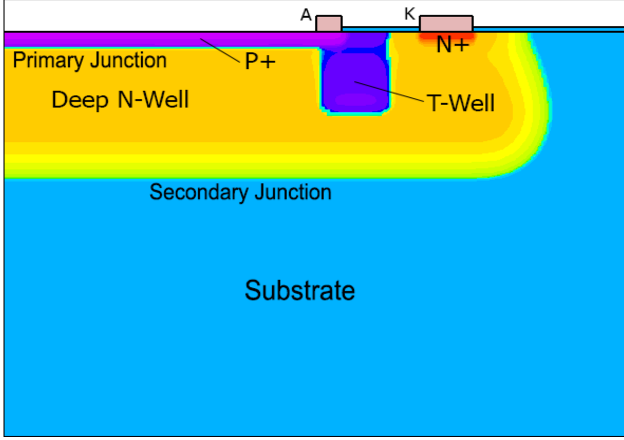

Fig. 1. SPAD structure simulated with TCAD tools. The left border acts as an axis of revolution.

efficiency for different wavelengths, for a window of illumination that matched the active area. After that, a dc simulation was conducted to find out the I-V characteristics of the four SPADs at a given temperature. Key parameters are extracted along with their temperature dependence, namely: breakdown voltage, built-in voltage and maximum electric field for the primary and secondary junctions and the guard ring.

III. Current-Voltage Modeling

The analytical model is similar to that in [3] and is shown in Fig. 2. Unlike previous works, both primary and secondary junctions have been considered in order to describe the dc current-to-voltage relation. A fully differentiable pseudo-max function is used to avoid convergence problems when the reverse bias voltage is near the breakdown voltage [3]:

$$I_{SPAD} = \begin{cases} I_{S1} & \text{no avalanche} \\ I_{S1} + \frac{V_n}{R_{brk}} \cdot \ln\left(1 - e^{\frac{V_E}{V_n}}\right) & \text{avalanche} \end{cases} \quad (1)$$

being I_{SPAD} the SPAD reverse current, I_{S1} the saturation current through the primary junction. The three other parameters are: the breakdown series resistance (R_{brk}), the excess bias voltage ($V_E = V_{KA} - V_B$) and a normalization voltage (V_n).

The dynamic (ac) behavior of the SPAD can be determined by three contributions: the charges being stored in both depletion regions (Q_{j_1} and Q_{j_2}) and the anode-to-substrate (Q_{AS}) stray

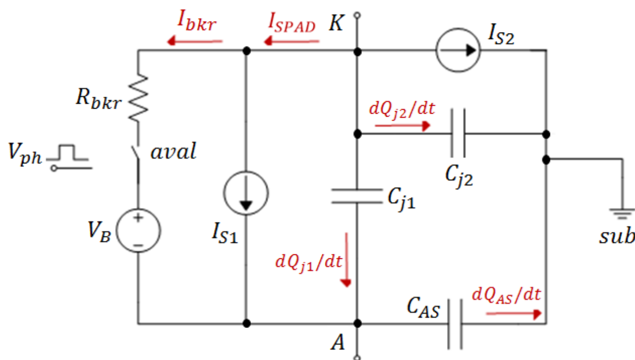

Fig. 2. SPAD analytical model.

capacitor. In other works, a cathode-to-substrate stray capacitor is used instead of the stored charge in a second depletion region [2]-[4].

Therefore, the current at the diode terminals is:

$$I_K = I_{SPAD} + I_{S2} + \frac{dQ_{j_1}}{dt} + \frac{dQ_{j_2}}{dt} \quad (2)$$

$$I_A = -I_{SPAD} - \frac{dQ_{j_1}}{dt} + \frac{dQ_{AS}}{dt} \quad (3)$$

where I_{S2} is the saturation current of the secondary junction.

IV. Modeling of Statistical Phenomena

There are three statistical phenomena that may trigger an avalanche in the SPAD. The first one is the arrival of a photon to the space charge region. Next one is the generation of charge carriers in the depletion region of the active area, that is responsible for the primary dark counts. And finally, the release of carriers from deep-level traps after previous avalanche pulses, that accounts for the secondary dark counts.

A. Photon arrival

The probability of a photon arriving to the space charge region and triggering an avalanche is governed by the photon detection efficiency (PDE):

$$PDE = QE(\lambda) \cdot FF \cdot P_{tr} \quad (4)$$

being $QE(\lambda)$ the quantum efficiency, which can be determined by TCAD simulations, *FF* the fill factor and P_{tr} the avalanche triggering probability, which can be then approximated experimentally with the *PDE* data provided in [7] .

B. Primary dark counts: thermal generation of carriers

Thermal carrier generation is characterized by a carrier generation rate: CGR_{TH}. It can be expressed by the well-known Shockley-Read-Hall theory of recombination through defects:

$$CGR_{TH} = \frac{n_i A W}{\tau_{eff}}\left(1 - e^{\frac{-qV}{2k_bT}}\right) \quad (5)$$

Here, the difficulty lies in determining the effective carrier lifetime, τ_{eff}. The work about dark count spectroscopy, presented at [7], suggests that the major source of DCR in modern SPADs is the phosphorus-vacancy defect or E-center. This known defect has an activation energy of $E_a \approx 0.44$eV below the conduction band and a cross-section of $\sigma_T = 1.1 \cdot 10^{-13}\text{cm}^2$ [10]. If we consider this defect a single-level trap, that this energy is stable, that the semiconductor is non-degenerate and that the trap acts mainly as a recombination center, τ_{eff} can then be approximated [11]:

$$\tau_{eff} \approx \frac{\tau_{n_0}(p_0+p_1+\Delta n)+\tau_{p_0}(n_0+n_1+\Delta n)}{n_0+p_0+\Delta n} \quad (6)$$

being n_o and p_o are electron and hole concentrations at thermal equilibrium, n_1 and p_1 are the SRH densities, and Δn is the injection density level, which can be expressed as a linear

function of I_{SPAD} through TCAD simulations. Finally, τ_{n0} and τ_{p0}, the recombination lifetimes for electrons and holes, are given by:

$$\tau_{0n,p} = \frac{1}{vth_{e,h}\, N_T\, \sigma_T\, (1+\Gamma_{n,p})} \quad (7)$$

where $vth_{e,h}$ is the electron and hole thermal velocity, N_T the density of recombination centers and σ_T the cross-section of this recombination centers, also called traps. Here the classic equations are modified by adding a parameter called the electric-field enhancement factor (Γ) [11]. This parameter represents the trap-assisted tunneling component and can only be solved by numerical methods, however an exponential fit could be determined from the numerical results obtained and thus be added to the model:

$$\Gamma_n \approx G_1(T) \cdot e^{G_2(T)\cdot E} \quad (8)$$

$$\Gamma_p \approx G_3(T) \cdot e^{G_4(T)\cdot E} \quad (9)$$

being E the electric field in the primary junction and G', parameters that show a quadratic dependence with the temperature that fit the numerical results above. It has to be mentioned that these results are consequence of the calculations from the TCAD simulations.

C. Primary dark counts: band-to-band tunneling.

With the scaling down of CMOS technology, the depletion layer is becoming increasingly thinner. This increases the electric field. When it approaches $7 \cdot 10^5$ V/cm, the probability of an avalanche being triggered by a carrier generated by a band-to-band tunneling (BTBT) process becomes significant.

In this paper, we apply the work in [6] about the widely used Kao's model to determine the carrier generation rate due to BTBT (CGR_{BTBT}), as it has been successfully reported [7].

Once the primary sources to dark count have been defined, the dark count rate due to primary sources can be expressed as [4]:

$$DCR_{PRI} = (CGR_{TH} + CGR_{BTBT}) \cdot P_{tr} \quad (10)$$

Each carrier generation process follows a Poissonian distribution whose average value is its own *CGR*. Then, the time interval between two subsequent carrier generation events of each carrier generation process has an exponential distribution, whose expected mean value is respectively:

$$\tau_{TH,BTBT} = \frac{1}{CGR_{TH,BTBT}} \quad (11)$$

D. Secondary dark counts: after-pulsing.

Deep-level traps are defects in the semiconductor lattice causing valid energy levels in the forbidden band-gap. During the triggering of an avalanche, some carriers may be captured by these deep-level traps. After a period of time that is statistically defined as the trap lifetime, the carrier is released. If the SPAD is ready to detect a photon at that time, this released carrier may trigger an additional avalanche. This phenomenon is called after-pulsing. In general, there are several deep level traps, and they can be modeled by different trap-lifetimes.

The probability of after pulsing is a function of time as stated by [12], and is given by [12]:

$$P_a(t) = \sum_{i=1}^{N} \frac{A_i}{\tau_i} e^{\frac{-t}{\tau_i}} \quad (12)$$

being A_i a pre-exponential factor, N the number of deep-level traps, i the i-th deep-level trap and τ_i the trap-lifetime of the i-th trap. The pre-exponential factor represents the probability of a carrier being captured by a unique deep-level i-th trap during an avalanche, and, if to be released, the probability for that carrier to trigger an avalanche [13]:

$$A_i = N_{Ti}\, \sigma_{Ti}\, vth_e\, n_e\, t_a\, P_{tr} \quad (13)$$

$$n_e = \int_{t_0}^{t_f} \frac{I_{spad}}{q} dt \quad (14)$$

where σ_{Ti} represents the cross-section of the i-th deep-level trap, n_e the electrons generated during the last avalanche, N_{Ti} the i-th deep-level trap density and t_a the duration time of the last avalanche which begins at t_0 and ends at t_f.

In our work we used the data provided by [4], who models the after-pulsing with 3 deep-level traps (1 slow trap of 156 ns of trap-lifetime, and 2 fast traps of 23 and 28 ns trap-lifetime at a temperature of 300K). The traps cross-sections were approximated from the data provided by the work in [3].

E. Modeling of temperature effects

This work includes two additional temperature-dependent effects that has not be included in other works to the best of our knowledge:

1) Trap and deep-level trap cross-section temperature dependece (σ_T): The values associated to these parameters, described in this work, are considered to be at room temperature (300K). If we take it as a reference [14]:

$$\sigma_T = \sigma_{300} e^{\frac{E_A}{k_B}\left(\frac{1}{300} - \frac{1}{T}\right)} \quad (15)$$

2) Self-Heating: the generated current by avalanches increases the device temperature significantly. This work just considered the simple model of Joule heating:

$$\Delta T = P_w \cdot R_T = R_E \cdot I_{SPAD}^2 \cdot R_T \quad (16)$$

where P_w is the dissipated power in the SPAD, R_T the thermal resistance and R_E the electric resistance of the volume of the device where the current flows. It is to be noted that the thermal resistance of silicon is also temperature-dependent.

V. Simulation and Experimental Validation

A model has been built in Verilog-A HDL using data from a TCAD simulation of a SPAD. The Verilog-A model simulations have been carried out using Cadence Spectre. The SPAD model is operated under a 100-kΩ passive quenching resistor, and

proved to have fidelity to the real-life one, as matched parameters like the breakdown voltage (10.3V at Fig. 3 (top)).

When making the Verilog-A model, the most difficult parameter to determine was the density of recombination centers, N_T. This is a technology parameter which is not often available. Hence, a process of calibration was needed. In order to do so, we employed the experimental DCR results of obtained by [9] and took the DCR value at 0.65V of excess voltage as a reference. Bottom of Fig. 3, shows how the complete model matches the experimental results quite well, getting a relative error no greater than 7% from 0.55V excess bias voltage onwards. It is also possible to see how a model without the self-heating effect (No SH) or without the trap cross-section dependence on the temperature (No Trap(T)), underestimates the dark count rate significantly as early as 0.8V of excess bias. With these results we can tell that this SPAD is indeed heavily affected by self-heating. Also, not taking the TAT contribution to DCR can lead to an overestimation of dark counts as a result of overestimating N_T by more than two orders of magnitude.

VI. Conclusion

In this paper a new approach to model a single-photon avalanche diode has been proposed through TCAD simulations and Verilog-A modelling. This approach has proven to be accurate to describe the behavior of carrier generation, and to diagnose some problems of the real SPADs like, in this case, self-heating. The model can be also used to improve and design circuits, since Verilog-A is integrated in Spectre and SPAD arrays are usually limited by dark counts, especially in time-of-flight applications. Also it can be used to design a SPAD at a given technology and make it appropriate for a specific purpose. For example, we could engineer the electric field at the junction by means of TCAD simulation and try to negate the band-to-band tunneling component of the primary DCR. The advantage of using TCAD simulations is that the final model can be easily modified to include other complex SPADs structures like virtual guard rings.

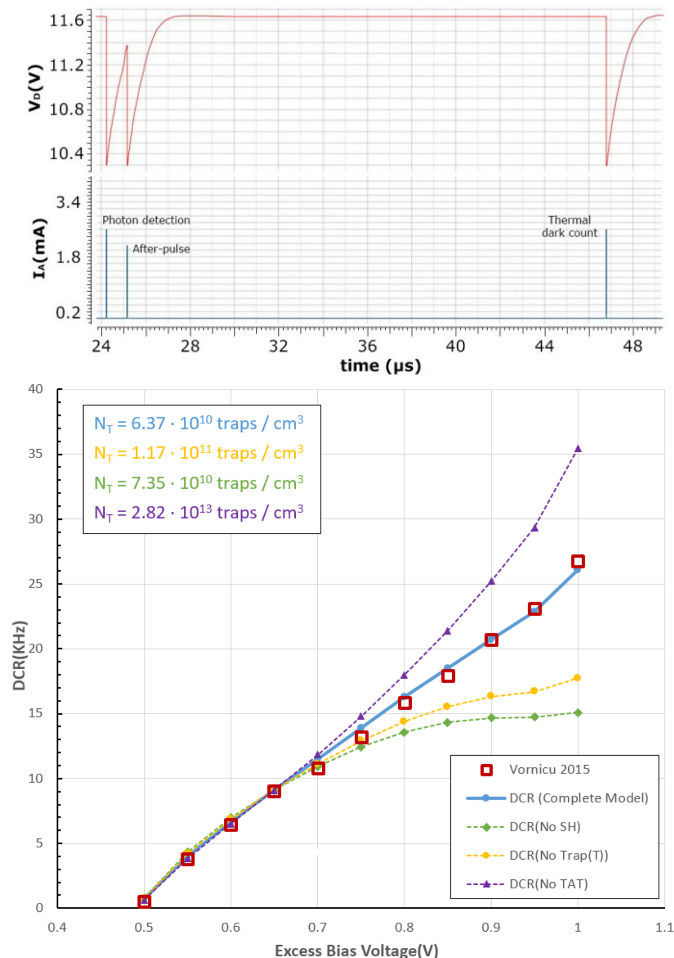

Fig. 3. Example of a simulation run with 1.25 V of excess bias at 40ºC (top), and simulation results of the primary DCR with excess bias voltage for the complete model and some partially complete instances of the model (bottom).

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