A 2.2 μW analog front-end for multichannel neural recording

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***Abstract*—In this paper an analog front-end for the multichannel implantable recording of neural signals is presented. It is comprised by a two-stage AC-coupled low-noise amplifier (LNA) and a one stage AC-coupled variable gain amplifier (VGA). The proposed architecture employs highly power-noise efficient current reuse fully differential OTAs in the LNA stage and a fully differential folded cascode for the VGA stage. Simulation results in AMS $0.18\mu m$ validate the proposed architecture under process corners variations with an estimated power consumption of $2.2\mu W$ and $3.1\mu Vrms$ in-band noise.**

***Index Terms*—analog front-end, neural recording, low-power circuit, low-noise circuit**

I. Introduction

Recent advances in microelectronics and micromachining have brought forward the possibility of high-density in-situ recording of neural signals [1] [2] [3]. The sensing and processing of these signals has varied applications such as prosthetic limb control [4], speech decoding [5] and epileptic seizure prediction [6].

Neural signals at the cortex level can be classified as follows:

- Local Field Potential.
  Generated by the activity of a group of neurons, it has an amplitude of $(10\mu\text{-}1m)V$ in the $(1-500)Hz$ frequency band.
- Action Potential.
  It is product of the dynamics of a single neuron, it has an amplitude of $(10\mu - 1m)V$ in the $(250-7k)Hz$ band.

Fig. 1 shows a general block-based view of an implantable neural recording chip. It can be seen that the analog front-end (AFE) performs the fundamental task of acquiring the neural signals which are then converted to the digital domain for further processing. The design of the AFE is a clear challenge since it has to achieve the following:

- Low-power consumption due to the limited budget as well as the danger of tissue damage.
- The input referred noise of the front-end has to be kept below the background noise of the recording site ($< 5\mu Vrms$).
- Rejection of DC non-idealities produced at the tissue-electrode interface.
- Minimum area occupation.

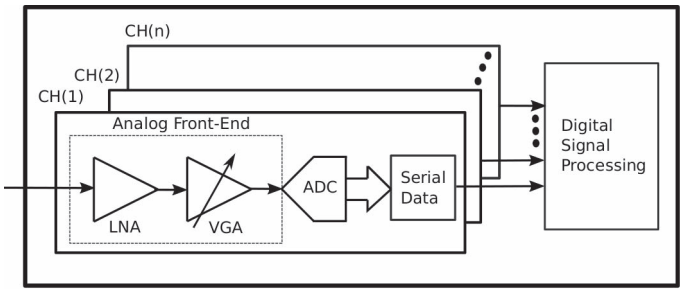

Fig. 1: Multichannel neural recording chip.

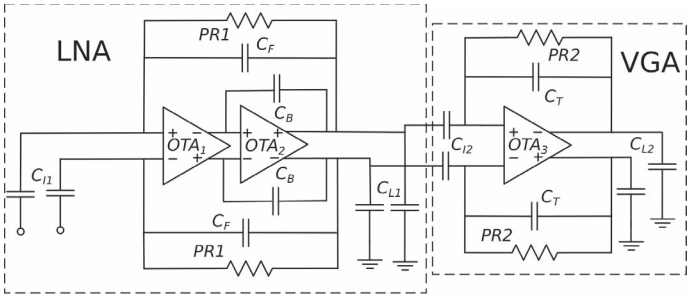

Fig. 2: Proposed analog front-end.

- Large enough gain in order to obtain an adequate signal range to ease the design of the subsequent stages.

In this paper, an AFE for multichannel neural recording is presented. It is inspired by the one introduced by [7]. It features a capacitive-coupled two-stage low-noise amplifier (LNA) as well as a folded-cascode based variable gain amplifier (VGA). The paper presents the details of the AFE design in Section II. Section III contains the simulation results, conclusions are discussed in Section IV.

II. Analog Front-end

The proposed AFE is shown in Fig. 2. It is comprised by three operational transconductance amplifiers (OTA), where the first two belong to the LNA stage and the last one performs the VGA function. Details are given in the following subsections.

A. LNA

Although high-gain is not the goal of the LNA, it is still necessary to set a considerable amount around $(30-40)dB$.

The gain is given by:

$$Gain_{LNA} \simeq \frac{C_{I1}}{C_F}. \quad (1)$$

The LNA has AC-coupled inputs meaning it exhibits a band-pass frequency response. The high-pass corner is set by:

$$HPcorner_{LNA} = \frac{1}{C_F PR_1}, \quad (2)$$

where PR is a pseudo-resistor structure that displays an extremely high resistance which enables the setting of a $< 1Hz$ high-pass corner. This is required in order to reject DC non-idealities generated at the tissue-electrode interface.

Capacitor C_B compensates the amplifier and allows for low-pass tuning in order to alleviate process variations. The low-pass corner is given by:

$$LPcorner_{LNA} \simeq \frac{C_B \beta}{\alpha}. \quad (3)$$

Small-signal analysis shows that $\beta = -C_F gm_1 + C_I gm_2 - C_F gm_2 - C_{p1} gm_2$ and $\alpha = C_I C_F C_B + C_I C_F C_{p2} + C_I C_B C_{p2} + C_I C_B C_L + C_I C_{p2} C_L$. Where C_{p1}, C_{p2} and gm_1, gm_2 are the parasitic input capacitance and transconductance of each OTA, respectively.

The LNA is comprised by a couple of OTA circuits as shown in Fig.3(a), differently sized and biased according to its function as introduced by [8]. In both cases, they are biased in weak inversion in order to obtain maximum transconductance efficiency. The transconductance in weak inversion is:

$$gm = \frac{I_{BIAS}}{nVt}. \quad (4)$$

Sensing a signal while exhibiting low-noise is the main function of the LNA. The main noise contributor in this circuit is the differential pair of OTA_1. Achieving relatively low $1/f$ noise is possible once large areas for the differential pair are used, by neglecting its contribution the noise of OTA_1 can be approximated as follows:

$$\overline{Vni^2_{OTA_1}} \simeq \frac{4kT\gamma nVt}{I_{BIASOTA_1}} \cdot \Delta_f, \quad (5)$$

where $\gamma = 1/2$ in weak inversion and Δ_f is the bandwidth of the amplifier. The noise introduced by the feedback pseudo-resistor can also be neglected since it is inversely proportional to its resistance. Referring this noise to the LNA gives:

$$\overline{Vni^2_{LNA}} = \frac{C_{I1} + C_F + C_{P1}}{C_{I1}} \cdot \overline{Vni^2_{OTA_1}}. \quad (6)$$

It can be seen then that noise reduction can also be achieved if C_{I1} is made as large as possible.

Considering the previous remarks, the design of the LNA focuses first on achieving a noise floor target of $\sim 50nV/\sqrt{Hz}$. Eq. 6 tells us that this is done by increasing the bias current in OTA_1, further noise reduction is obtained if large differential pair areas are considered. This last measure also leads to mismatch offset reduction. OTA_2 is biased in weak inversion

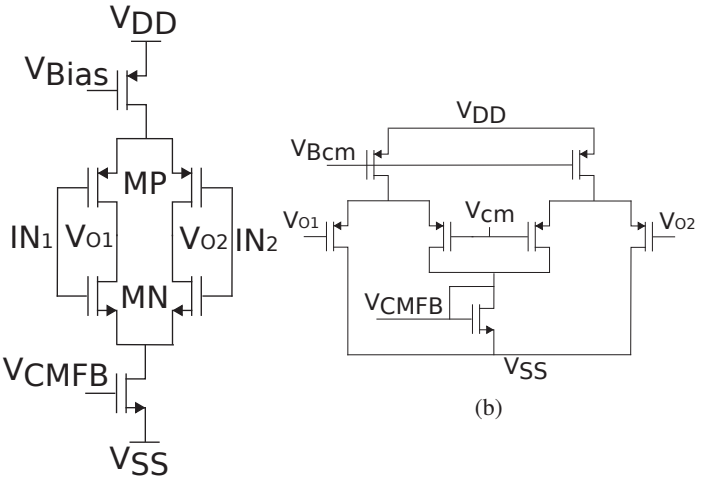

Fig. 3: (a) Current reuse OTA.(b) Common mode feedback.

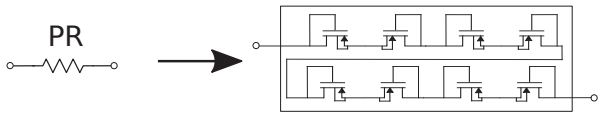

Fig. 4: Feedback Pseudo-resistor.

in such a way that it contributes mainly to increase the gain of the LNA while consuming the least possible current in order to improve its noise efficiency factor (NEF).

The pseudo-resistor is comprised by four-pairs of transistors in deep subthreshold region as shown in Fig. 4. This chain is used since it represents a relative improvement in linearity over the usual one-pair pseudo-resistor.

C_{I1} is sized as large as possible in order to achieve a low noise floor while keeping in mind its area contribution. The gain target of the LNA has to be also considered when sizing C_{I1}, this is also the case for C_F. C_B defines the bandwidth of the LNA and is sized for a target of $\sim 7kHz$. Design values for the capacitors in the LNA end up as follows: $C_{I1} = 30pF$, $C_F = 0.28pF$, and $C_B = 5pF$. The common mode-feedback is shown in Fig. 3(b). Table I shows relevant sizing and biasing data with $V_{DD} = 1V$ and the AMS $0.18\mu m$ process for the AFE.

TABLE I: Operating points for transistors in the differential pairs of OTA1 and OTA2.

Device	W/L (μm)	Ibias (nA)	Inversion Coefficient
MP_{OTA1}	300/4	563	0.021
MN_{OTA1}	200/4	563	0.013
MP_{OTA2}	110/1	25	$3.3e^{-4}$
MN_{OTA2}	90/1	25	$6.3e^{-4}$

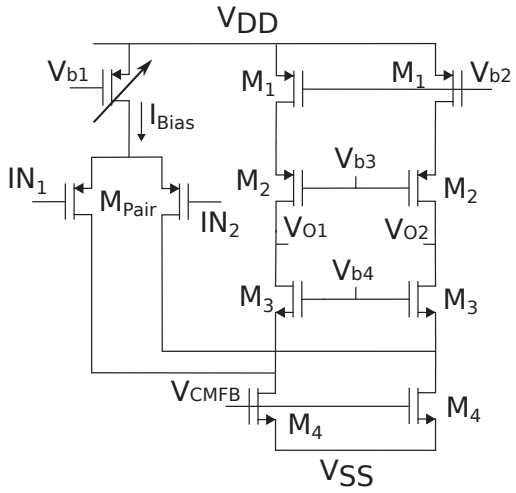

Fig. 5: FC OTA for the VGA stage.

B. VGA

The VGA stage increases the overall gain of the AFE by $(15-20)dB$. A one-stage AC-coupled OTA is used since this structure eases the gain tuning while also keeping the necessary high-pass corner for LFP signals. The gain is given by

$$Gain_{VGA} \simeq \frac{C_{I2}}{C_T}. \tag{7}$$

Gain tuning is realized by capacitor bank C_{I2}. The high-pass corner is given by

$$HPcorner_{VGA} = \frac{1}{C_T P R_2}. \tag{8}$$

The low-pass corner is as follows:

$$LPcorner_{VGA} = \frac{gm_3}{Gain_{VGA} \cdot (C_{L2} + C_{P3})}, \tag{9}$$

where C_{P3} is a parasitic capacitance of OTA_3. The bandwidth defined by these equations should be larger than the LNA bandwidth so that the gain is tuned with minimal impact on the bandwidth. It can be seen that low-pass corner variations can be compensated by changing the bias in OTA_3.

A folded cascode (FC) OTA as shown in Fig. 5 is used to implement the VGA function. Since its noise contribution to the system noise is negligible, the sizing and biasing focuses on achieving both, bandwidth and gain targets with the least possible power consumption. As usual, this is done by biasing the circuit in moderate to weak inversion. This stage uses the same common-mode feedback circuit as the LNA, shown in Fig. 3(b). Table II shows the operation point for the VGA stage.

III. Simulation Results

Electrical simulations of the AFE were performed in Cadence-Spectre. Fig. 6 shows a total minimal gain of $\sim 49dB$ in all 180 process corners for the AFE. A high-pass frequency spread of $(0.3-1.8)Hz$ and a low-pass spread of $(3.6-8.2)kHz$ is also seen. Worst-case bandwidth can be compensated with an increase in the current bias of OTA_3.

TABLE II: Operating points for transistors in OTA3.

Device	W/L (μm)	Ibias (nA)	Inversion Coefficient
M_{PAIR}	11/31	138	11
M_1	1/10	26	0.7
M_2	1/10	26	0.7
M_3	6/60	26	0.7
M_4	23/10	164	0.2

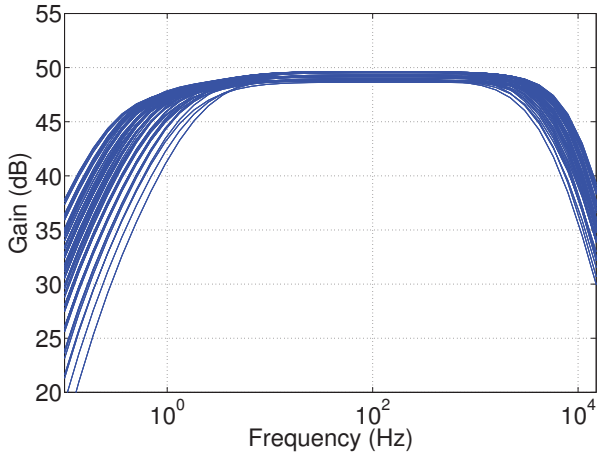

Fig. 6: AFE AC Response under process corners.

Fig. 7 shows the available gains for the AFE. A $49dB$ gain is achieved if C_{I2} is set to $9pF$ while $55dB$ are obtained for $19pF$. Thus, a capacitor bank that covers the $9pF-19pF$ range is able to set the AFE gain in the specified gain interval.

Fig. 8 shows Monte-Carlo simulation results of the output node voltage.

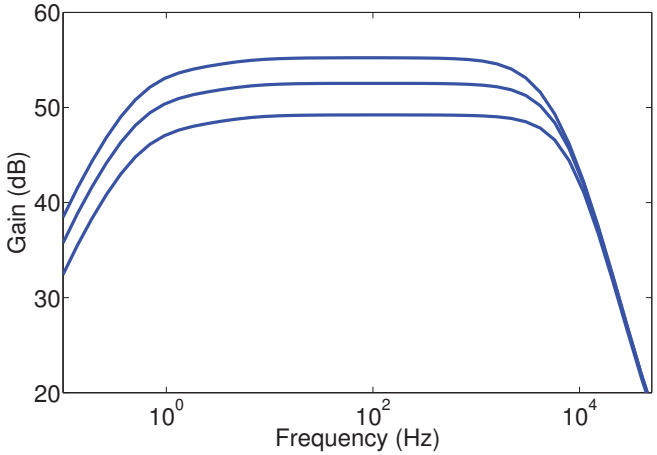

Fig. 7: AFE tunable gain.

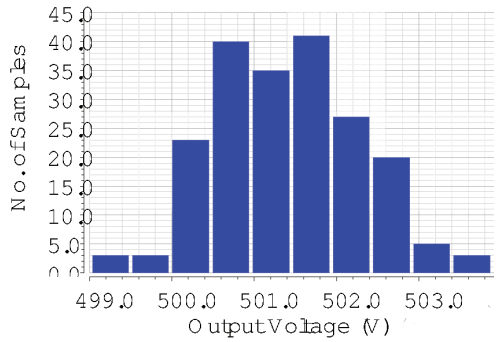

Fig. 8: 200 Monte-Carlo runs for the output voltage.

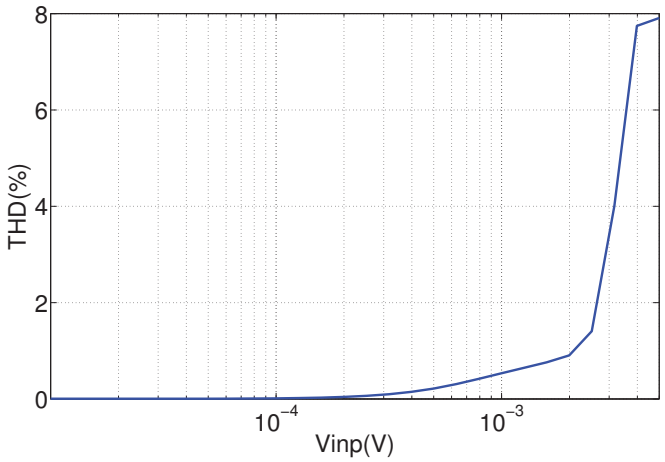

Fig. 9: Total harmonic distortion for the AFE.

Finally, the total harmonic distortion and hence, the input swing capabilities of the AFE are shown in Fig. 9 for a frequency of $1kHz$. Table III shows more details of the performance of the simulated circuit.

IV. Conclusions

This paper presented a novel three-stage OTA analog front-end for the implantable recording of neural signals. The LNA has been successfully tested under process corners and the nominal case satisfies the initial power and noise targets. The simulated results suggests an state of the art performance of the eventually fabricated chip. It is expected that this circuit will be used as the basis for a multichannel neural interface.

TABLE III: Comparison with state of the art.

	This work (simulation)	[3]	[9]	[10]
Gain (dB)	49-55	54-60	49-66	52-55
Power (μW)	2.2	-	4.7	0.73
Bandwidth (Hz)	(0.6-7k)Hz	(0.38-5.1k)Hz	(350/0.1-11k/293)Hz	(0.25-8k)Hz
Integrated Input Noise	3.1	4	5.4-11.2	3.2
THD (%)	1@1mVpin 1kHz	1@0.9Vpout -	- -	0.53@900μVout 1kHz
NEF (AFE)	2	1.9	4.4	1.57

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