Operational Transconductance Amplifier-Based Nonlinear Function Syntheses

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Abstract — **We show that the operational transconductance amplifier (OTA), as the active element in basic building blocks, can be efficiently used for programmable nonlinear continuous-time function synthesis. Two efficient nonlinear function synthesis approaches are presented. The first approach is a rational approximation and the second is a piecewise-linear approach. Test circuits have been fabricated using a 3-μm p-well CMOS process. The flexibility of the designed and tested circuits was confirmed.**

I. Introduction

LATELY, several authors [1]–[5] have been successfully using the operational transconductance amplifier (OTA) as the main active element in continuous-time active filters. The OTA is a programmable device[1] and has only a single high-impedance node, in contrast to conventional op amps. This makes the OTA an excellent device candidate for high-frequency and voltage (or current) programmable analog basic building blocks.

The applicability of OTA's as components in the design of linear networks has been extensively discussed elsewhere [1], [6] and will not be repeated here.

The objective of this paper is to examine the applicability of OTA's as the basic elements in the design of *nonlinear* networks. There is not much reported in the literature on the use of OTA's for designing nonlinear components [7], [8]. Excellent contributions [9]–[11], [16] are reported of nonlinear circuits dealing with particular important nonlinear problems. In this paper, rather than try to tackle a specific problem, we focus our attention on a general approach dealing with nonlinear basic building blocks using OTA's as the main active elements. Nothing special was done to optimize the circuit performance but rather to explore the potential and applicability of the OTA-based nonlinear system approach.

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[1]The output current I_0 of an OTA due to a differential input v_{id} is $I_0 = g_m v_{id}$, and g_m is a voltage (current) controllable parameter [1], [6], [7].

We will present a number of nonlinear OTA circuits and will discuss two nonlinear analog function synthesis techniques based on these OTA basic building block elements. One synthesis approach uses rational approximation functions and the other uses a piecewise-linear approximation. Actual circuit implementations will be presented as well as the experimental results from several 3-μm p-well CMOS test prototypes.

II. Basic Building Blocks

In this section we introduce the OTA-based fundamental nonlinear building blocks involved for the synthesis procedures.

A. Multiplier Block

A two-input four-quadrant multiplier has an output current given by

$$I_0 = K_M V_1 V_2 \tag{1}$$

where the multiplier constant K_M has units of amperes per square volt. If V_1 and V_2 can take any positive or negative sign, the multiplier is called a four-quadrant multiplier. This multiplier is represented in Fig. 1(a). The corresponding OTA-based implementations are shown in Fig. 1(b) and (c). The triangular block labeled a represents a signal attenuator (with an attenuation factor a); its function is to equalize the maximum voltage swing of V_1 and V_2. $-V_{\text{BIAS}}$ is the usual bias control of the OTA. An active attenuator can be implemented in CMOS technology [15]. The signal level in the multiplier is restricted by a few hundred millivolts for V_{I_1} and V_{I_2}. Although not indicated in Fig. 1, assume the power supplies of the OTA's are V_{DD} and $-V_{SS}$. The two options of Fig. 1(b) and (c) allow us to change the sign of K_M. Thus for the circuit of Fig. 1(b) we obtain

$$I_{o_1} = g_{m_1} V_1 = K\left(V_{I_1} + V_{SST}\right) V_1 \tag{2a}$$

and

$$I_{o_2} = -g_{m_2} V_1 = -K\left(V_{I_2} + V_{SST}\right) V_1 \tag{2b}$$

where K is a process- and geometry-dependent constant,

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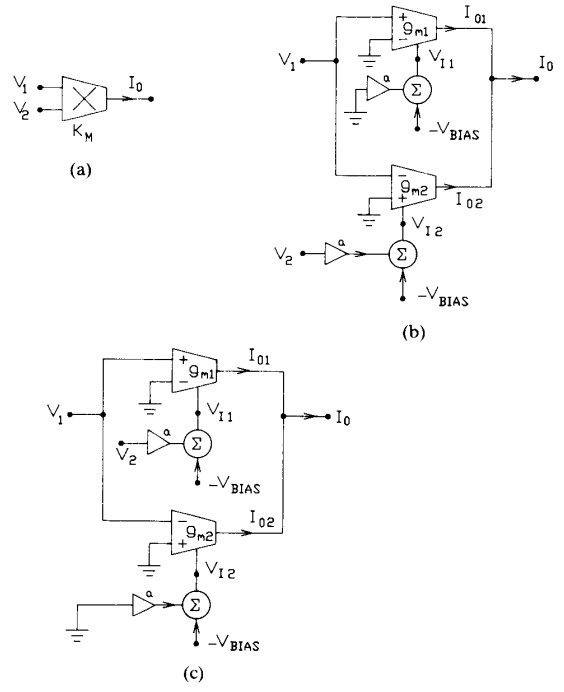


Fig. 1. Multiplier: (a) symbol, (b) OTA implementation 1, and (c) OTA implementation 2, $0 < a < 1$.

$V_{SST} = V_{SS} - V_t$, and V_t is a transistor threshold voltage[2]:

$$V_{I_1} = a0 - V_{\text{BIAS}} \tag{3a}$$

$$V_{I_2} = aV_2 - V_{\text{BIAS}}. \tag{3b}$$

The output current I_0 becomes

$$I_0 = I_{o_1} + I_{o_2} = \left[K(-V_{\text{BIAS}} + V_{SST}) - K(aV_2 - V_{\text{BIAS}} + V_{SST})\right]V_1 \tag{4}$$

$$I_0 = -aKV_1V_2 = K_MV_1V_2, \qquad K_M = -aK. \tag{5}$$

A similar analysis of the circuit of Fig. 1(c) yields

$$I_0 = aKV_1V_2 = K_MV_1V_2, \qquad K_M = aK. \tag{6}$$

Therefore, we can make the sign of K_M positive or negative.

B. Divider Block

A two-input divider has an output which is the ratio of the two inputs, multiplied by a constant K_R with dimensions in volts:

$$V_0 = K_R\frac{V_1}{V_2}. \tag{7}$$

A symbol of the divider is shown in Fig. 2(a), where n and d stand for numerator and denominator, respectively. The corresponding circuit implementation using the multiplier symbol is shown in Fig. 2(b). Analysis yields

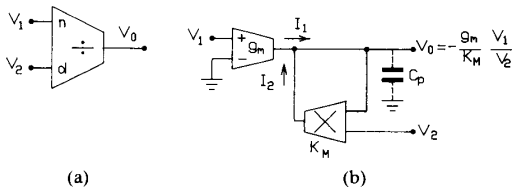


Fig. 2. Divider: (a) symbol and (b) OTA implementation.

$$I_1 = g_mV_1 \tag{8a}$$

$$I_2 = K_MV_0V_2. \tag{8b}$$

By Kirchhoff's current law (KCL) we obtain

$$I_1 + I_2 = g_mV_1 + K_MV_0V_2 = 0. \tag{9a}$$

Thus, the resulting output signal is proportional to the ratio of the input signals

$$V_0 = -\frac{g_m}{K_M}\frac{V_1}{V_2} = K_R\frac{V_1}{V_2}. \tag{9b}$$

Observe that K_R can also be either negative or positive and $V_2 = 0$ is not allowed to avoid output saturation (V_o). A closer look at the circuit of Fig. 2(b) is required to study stability. Assuming the dominant dynamic element is a parasitic capacitance C_p at the output, (9a) is modified as

$$I_1 + I_2 = sC_pV_0 \tag{10a}$$

which yields

$$V_0 = \frac{-g_mV_1}{K_MV_2 - sC_p}. \tag{10b}$$

Thus, V_0 has a pole located at

$$s_p = \frac{K_M}{C_p}V_2. \tag{10c}$$

Hence, in order for the circuit to be stable, its pole must be in the left-hand plane (LHP), which dictates that[3]

$$K_MV_2 < 0. \tag{10d}$$

A summary of the stability conditions are pictorially indicated by the hyperbolas of Fig. 3.

C. Squaring and High-Powers (Exponentiation) Blocks

A one-input squarer has an output proportional to the square of the input:

$$I_0 = K_MV_i^2. \tag{11}$$

[2]We have assumed equal K's and threshold voltages V_t's for the OTA's.

[3]Observe that we are applying linear treatment to a nonlinear circuit. This linear analysis is valid if for a certain instant t_x, $V_1(t_x)$ and $V_2(t_x)$ are considered constant; then V_o will eventually reach its solution independent of the initial conditions.

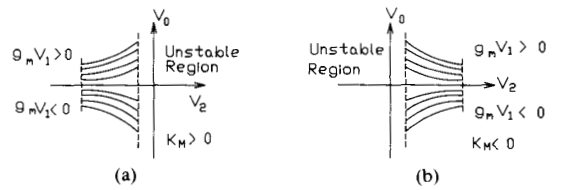


Fig. 3. Stability regions of divider. (a) Stable for $K_M > 0$ and $V_2 < 0$. (b) Stable for $K_M < 0$ and $V_2 > 0$.

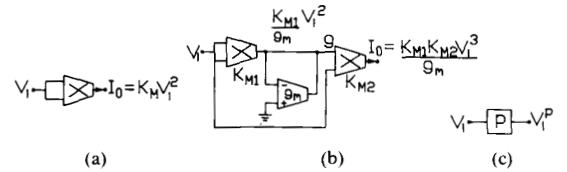


Fig. 4. Exponentiation (raising to a power) operation: (a) squarer, (b) cubic, and (c) pth.

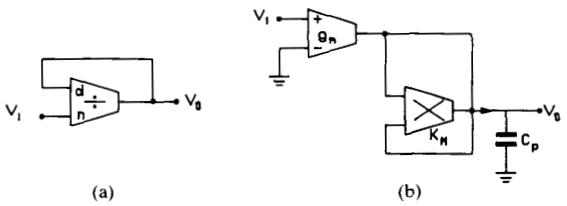


Fig. 5. Square rooter: (a) implementation and (b) OTA implementation.

The implementation of the squarer is obtained by simply using a multiplier with equal inputs, as shown in Fig. 4(a).

To obtain an *exponentiation* (raising to a power) circuit with an input V_i and an output to be proportional to V_i^p, where p is an integer greater than 2, we require $(p+1)/2$ multipliers for p odd and $p/2$ multipliers for p even. Furthermore, since the proposed multipliers are of the transconductance type, the outputs must be converted into voltages for use as the inputs to subsequent multipliers. This can be done by connecting an equivalent resistor at the output. An equivalent resistor using an OTA [5], [6] is implemented by connecting the output to the negative OTA input and grounding the positive OTA input. An example for $p = 3$ is shown in Fig. 4(b). It should be evident that a similar procedure can be followed to obtain an exponentiation of any order p; this is symbolically illustrated in Fig. 4(c).

D. Square-Rooter Block

A one-input square rooter has an output with the negative or positive square root of an input voltage multiplied by a constant of a proper polarity, e.g.

$$V_0 = \pm\left|\sqrt{K_R V_i}\right|, \qquad K_R V_i > 0. \tag{12}$$

Fig. 5(a) shows the implementation of the square rooter, where the output V_0 is given by

$$V_0 = K_R \frac{V_i}{V_0} \tag{13a}$$

which yields

$$V_0 = \pm\left|\sqrt{K_R V_i}\right|. \tag{13b}$$

A more detailed description of the implementation is shown in Fig. 5(b). The circuit will be stable if, after a perturbation, the output evolves towards the desired output value. Assume the input is fixed at $V_i = U_S$. To study the stability and the dynamics of the circuit, a parasitic capacitance C_p at the output is again considered. Using the KCL at the output node results in the following nonlinear differential equation:

$$C_p \frac{dV_0}{dt} = g_m U_S + K_M V_0^2 \tag{14a}$$

which can be rewritten as

$$\frac{1}{K_M} \frac{dV_0}{V_0^2 + \dfrac{g_m U_S}{K_M}} = \frac{dt}{C_p}. \tag{14b}$$

Integrating both sides of (14b) and solving for $V_0(t)$ (when $(g_m/K_M)U_S < 0$) yields

$$V_0(t) = K_i \frac{1 + \dfrac{V_0(0) - K_i}{V_0(0) + K_i} e^{2K_i\left(\frac{K_M}{C_p}\right)t}}{1 - \dfrac{V_0(0) - K_i}{V_0(0) + K_i} e^{2K_i\left(\frac{K_M}{C_p}\right)t}} \tag{15a}$$

where

$$K_i = \left|\sqrt{\frac{-g_m U_S}{K_M}}\right|$$

hence

$$V_0(\infty) = \begin{cases} K_i = \left|\sqrt{\dfrac{-g_m U_S}{K_M}}\right|, & \text{for } K_M < 0 \quad (15b) \\ -K_i = -\left|\sqrt{\dfrac{-g_m U_S}{K_M}}\right|, & \text{for } K_M > 0. \quad (15c) \end{cases}$$

For $(g_m/K_M)U_S > 0$ the solution yields an unbounded output. It is concluded that a stable square-rooter circuit is obtained when $(g_m/K_M)V_i < 0$, i.e., $K_R V_i > 0$. Furthermore, the polarity of V_0 can be determined according to (15b) or (15c). Fig. 6 shows the conditions for stable operation of the square rooter.

E. Piecewise-Linear Function Generators

Diodes interconnected with OTA's can simulate ideal diodes, hence allowing the creation of a piecewise-linear approximation to any desired nonlinear function. The ideal basic building blocks for a piecewise-linear function approximation are shown in Fig. 7. High-frequency improve-

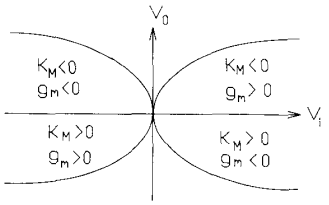


Fig. 6. Stability regions of square rooter.

ments of this basic block are discussed in the Appendix. Note that $I_D = 0$ until the breaking point (voltage reference V_r) is reached. The slopes of the linear segments are proportional to the g_m's. The diodes can be implemented with MOS transistors with their gate and drain tied together. If a step type input–output characteristic is needed to implement discontinuities in the function approximation, the linear OTA of Fig. 7 can be substituted by an OTA comparator which ideally simulates a large g_m and a saturation (output) current of $\pm I_{BIAS}$.

III. Nonlinear Function Syntheses

We present two approaches for nonlinear function syntheses. The first approximation uses a polynomial approach, and the second approximation a piecewise-linear approach.

The first is a *rational approximation* that has the general form of a polynomial function or of a ratio of polynomials, i.e.,

$$y_0 = \frac{\sum_{i=0}^{M} A_i x^i}{\sum_{i=0}^{N} B_i x^i} \tag{16}$$

where i is a positive integer number. In fact, the exponent i can be a fractional exponent of the form p/q, where p and q are negative or positive integers. Assume an element $K_R x^{p/q}$ needs to be implemented. This is obtained as shown in Fig. 8(a). The exponentiation blocks are of the type of Fig 4(c). If a negative $-p/q$ is needed, an additional divider is used as shown in Fig. 8(b).

Next we discuss a *piecewise-linear approximation* synthesis approach. This approach consists of adding (transconductance) gain segments that have null contribution until a reference (threshold) voltage is reached. A simple but illustrative example is shown in Fig. 9 where a convex curve is approximated. The breakpoints occur at V_{r_1}, V_{r_2}, and V_{r_3}. The slopes are given by

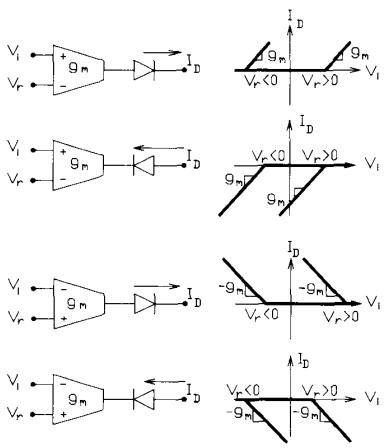


Fig. 7. Piecewise-linear (PL) function generator building blocks.

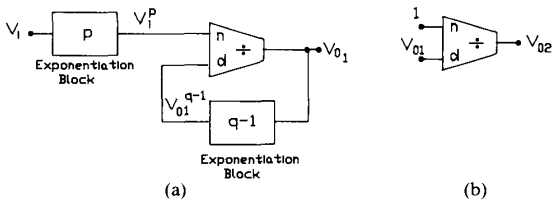


Fig. 8. Fraction power exponentiation: (a) $V_i^{p/q}$ and (b) $V_i^{-p/q}$.

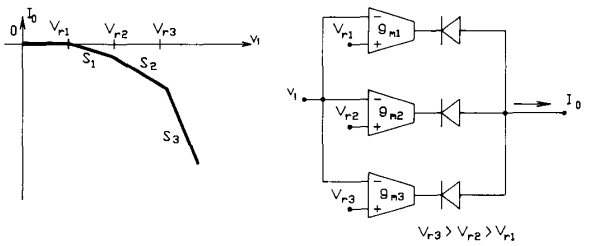


Fig. 9. Convex curve piecewise-linear approximation: (a) I_0 versus V_i characteristics, and (b) circuit implementation.

Note the continuing increase in magnitude of the slope as the input v_i increases, thus forming a convex curve. The approximation will improve as the number of segment lines increases.

Observe that by combining the basic building blocks of Fig. 7, arbitrary functions with variable positive and negative slopes and breakpoints can be approximated. Furthermore, the slopes and breakpoints are *voltage programmable*, which gives an additional flexibility in the function approximation design problem. Note that if a resistive load simulated with an OTA is used, the slopes become ratios of transconductances which provides a very

$$\begin{aligned}
&S_0 = 0, && I_o = 0, && \text{for } V_{r_1} > V_i \\
&S_1 = -g_{m_1}, && I_o = -g_{m_1} V_i, && \text{for } V_{r_2} > V_i > V_{r_1} \\
&S_2 = -(g_{m_1} + g_{m_2}), && I_o = -(g_{m_1} + g_{m_2}) V_i, && \text{for } V_{r_3} > V_i > V_{r_2} \\
&S_3 = -(g_{m_1} + g_{m_2} + g_{m_3}), && I_o = -(g_{m_1} + g_{m_2} + g_{m_3}) V_i, && \text{for } V_i > V_{r_3}.
\end{aligned}$$

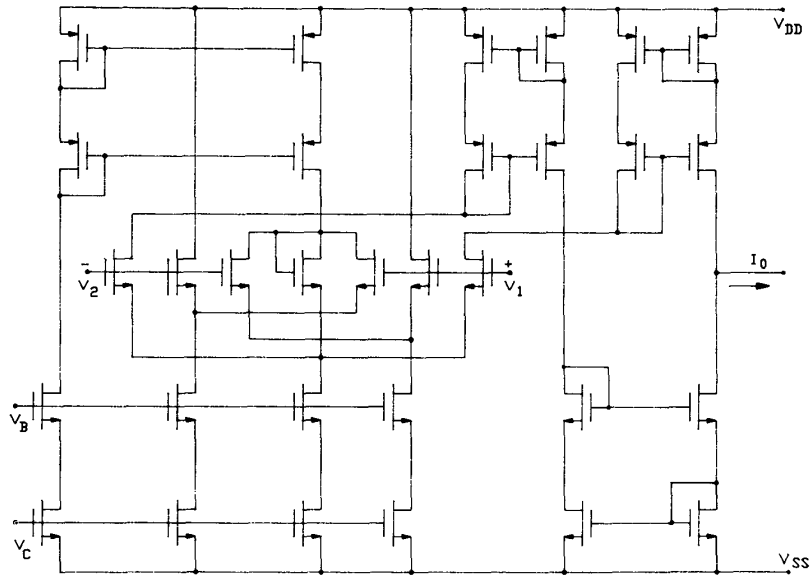


Fig. 10. Circuit diagram of the OTA [3] used.

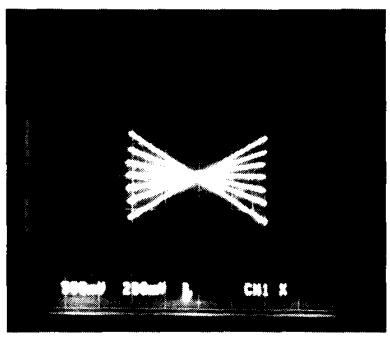


Fig. 11. Large-signal characteristics of multiplier. $V_1 = \pm\{0.75, 0.50, 0.25, 0.0\}$ V.

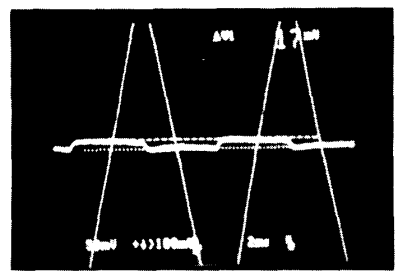


Fig. 12. Nonlinearity multiplier error: fixed $V_1 = 1$ V and variable triangular wave for V_2.

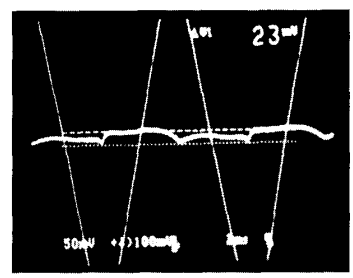


Fig. 13. Nonlinearity multiplier error: fixed $V_2 = 1$ V and variable V_1.

good temperature compensation [18] and accuracy improvement. In stringent applications where minimum temperature dependence is required, the use of a resistive-load OTA is needed. One example of an arbitrary function approximation containing negative and positive slopes is discussed in the next section. Details on the practical considerations of the OTA-based piecewise-linear circuits are given in the Appendix.

IV. Experimental Results

Several test circuits containing OTA's and transistors connected as diodes were fabricated using a 3-μm p-well CMOS process through (and thanks to) MOSIS. The linearized OTA used to synthesize the different nonlinear analog functions is reported elsewhere [3]. Its schematic is shown in Fig. 10. The OTA has an area of 220×700 μm^2 and consumes 10 mW for ± 5-V supply voltages. In all the examples (unless otherwise indicated) the output current was measured across a 100-kΩ load resistor.

A. Transconductance Multiplier

The structure used is as shown in Fig. 1. The measured value of $|K_M|$ is 3.3 $\mu A/V^2$. The output current was measured across a 100-kΩ load resistor. The large-signal characteristics of the multiplier are shown in Fig. 11. V_1 was held constant (at 0.0, ± 0.25, ± 0.50, and ± 0.75 V), while the input V_2 varied between ± 1 V. The nonlinearity error is shown in Fig. 12. For V_2, a triangular 2-V peak-to-peak signal was applied, while keeping V_1 equal to 1 V.

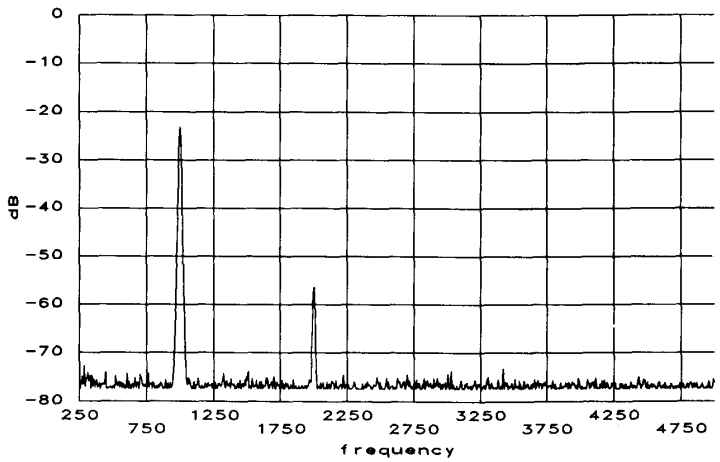


Fig. 14. Spectrum of the multiplier output voltage: $V_1 = 1$ V and $V_2 = 2\sin\pi \times 10^3 t$.

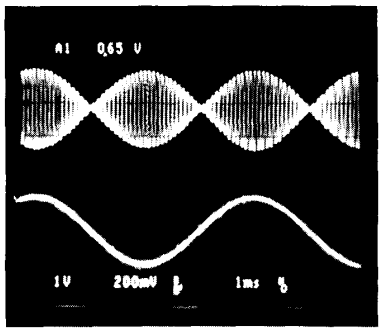


Fig. 15. Modulation for two-input sinusoidal signals.

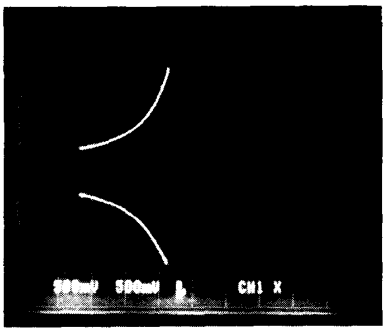


Fig. 16. Divider experimental results: constant V_1 and varying V_2.

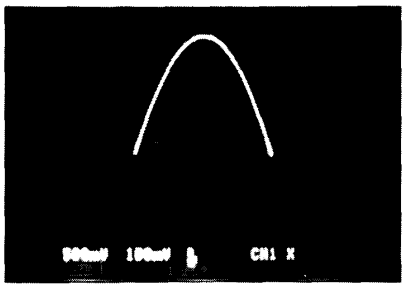


Fig. 17. Squarer experimental results.

The output current produced a triangular voltage signal of 660-mV peak to peak. Subtracting this signal from an ideal triangular wave, the resulting peak-to-peak error signal was 17 mV, which yields a nonlinearity error of nearly 2 percent. (The ideal triangular wave is a scaled version of the input in such a way that the amplitude of the error signal is minimum.) Repeating the measurement but interchanging V_1 and V_2 (V_1 is a triangular signal of 2-V peak to peak), the result obtained is shown in Fig. 13. The peak-to-peak error signal of 23 mV corresponds to a 3.5-percent nonlinearity error. The asymmetry of the multiplier (see inputs in Fig. 1) yields this distortion difference when interchanging the inputs. Making $V_1 = +1$ V and V_2 a 2-V peak-to-peak sinusoidal waveform of 1 kHz, the spectrum for the multiplier output shown in Fig. 14 was measured. Observe that only the second harmonic, 33 dB below the fundamental, is present. Fig. 15 shows the multiplier being used as a modulator where both input signals are sinusoidal.

B. Voltage Divider

The tested circuit has the structure shown in Fig. 2(b) with $|K_M|$ as before in Section IV-A and $K_M > 0$. The experimental result shown in Fig. 16 was obtained by switching V_1 between two symmetrical constant values (± 1 V) while varying V_2 ($V_2 < 0$). This result matches with the theoretical results of Fig. 3(a).

C. Squarer

The squarer is obtained by simply making $V_1 = V_2$ in the multiplier discussed in Section IV-A. In this particular case, K_M is negative resulting in the inverted parabola shown in Fig. 17. The input range was ± 1 V.

D. Square Rooter

The basic architecture used is the one shown in Fig. 5(b). The input signal V_i is given by $V_i = A + A\cos\omega t$ and

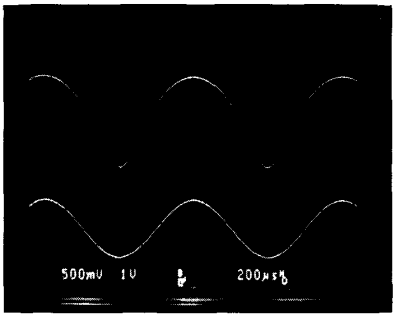


Fig. 18. Square rooter experimental results.

the output, obtained in the first quadrant, has the form

$$\left|\sqrt{-2\frac{Ag_m}{K_M}}\cos\frac{\omega}{2}t\right|$$

where $g_m > 0$, $K_M < 0$, $A = 1$ V, $f \simeq 1$ kHz, $g_m = 3.2$ μmhos, and $K_M = 3.3$ $\mu A/V^2$. The experimental results are shown in Fig. 18 where the lower trace signal is the input and the output is shown in the upper trace.

E. Piecewise-Linear Approximation

The intended transfer characteristic is shown in Fig. 19(a) and consists of three linear segments. The individual slopes due to each OTA are indicated in the lower part of Fig. 19(a), and the composed resulting transfer characteristics are shown in the upper part of Fig. 19(a). The actual OTA circuit implementation is shown in Fig. 19(b), where an optional diode and voltage source have been added at the OTA (2 and 3) to improve the high-frequency performance of the circuit (see the Appendix for more details). Note that the slopes of the transfer characteristics can be easily modified by changing the OTA voltage-dependent transconductances. The experimental results are shown in Fig. 19(c). To show further flexibility, a chip test circuit was reprogrammed to implement a five-segment characteristic to convert a triangular to a sinusoidal waveform. The experimental characteristic is shown in Fig. 30(a), and the input and output waveforms are shown in Fig. 20(b). The measured THD, after optimally adjusting breakpoints and slopes, was 1.5 percent. The chip photomicrograph for these experimental results is shown in Fig. 21.

V. Conclusions

The suitability of OTA's as the main active element to obtain basic building blocks for the design of nonlinear networks was established. Methods to implement practical nonlinear circuits in a systematic design approach were developed. Two practical synthesis approaches were introduced. Observe that for both approaches, every time the output current is converted into a voltage by an OTA resistor load, temperature variations are minimized. The programmability and flexibility of the OTA provide the potential to design time-varying nonlinear circuits. The experimental results verified theoretical predictions. Implementations of other nonlinear synthesis approaches [20] are feasible using the basic blocks here introduced. There are many important areas of application of nonlinear functions [22]. One of them is in neural networks [19], [21] as shown by Mead [17, ch. 6]. The proposed OTA-based building blocks can be incorporated in a CAD software [12] to fully exploit their functionality and versatility.

Appendix
Practical Considerations of the OTA-Based Piecewise-Linear Circuits

In this Appendix some practical considerations of the OTA-based piecewise-linear circuits are discussed taking into account some nonidealities of the OTA and of the MOS transistor used as a diode. A simple modification of the circuits of Fig. 7 that leads to a drastic improvement in their high-frequency performance is also presented.

Nonideal Circuit Elements

Simple equivalent circuits for an MOS OTA and for a diode-connected MOS transistor are shown in Fig. 22. The OTA is characterized by its output impedance (output capacitance C_o and output resistance R_o) and input capacitance (C_i). The diode-connected MOS transistor, as shown in Fig. 22(b), is modeled by a resistance[4] R_D in series with a voltage source V_t (threshold voltage of the MOS transistor) and an ideal diode, where $\hat{I}_D$ is the peak current in the MOS diode. Fig. 22(c) shows the equivalent circuit of the OTA when used as a two-terminal resistive element to simulate a grounded load resistance [6]. The simplified analysis that follows assumes that the transconductance g_m of the OTA is frequency independent and neglects the parasitic capacitance of the MOS transistor.[5] Also, effects due to OTA and diode resistance nonlinearities are not considered.

Low-Frequency Considerations

The low-frequency equivalent circuit of the OTA precision rectifier of Fig. 23(a) is shown in Fig. 23(b). g_{m_2} and R_{o_2} are the transconductance and the output resistance of an OTA used as a load. Parasitic capacitances have been neglected for this low-frequency analysis. Standard circuit

[4]In fact, taking into account the mobility degradation [14], R_D can be more accurately evaluated, i.e., $R_D \cong (2\theta/\mu_0 C_{ox})(L/W)$.

[5]In most practical cases the time constant $R_D C_D$ associated with the MOS transistor is negligible compared with other time constants in the circuit.

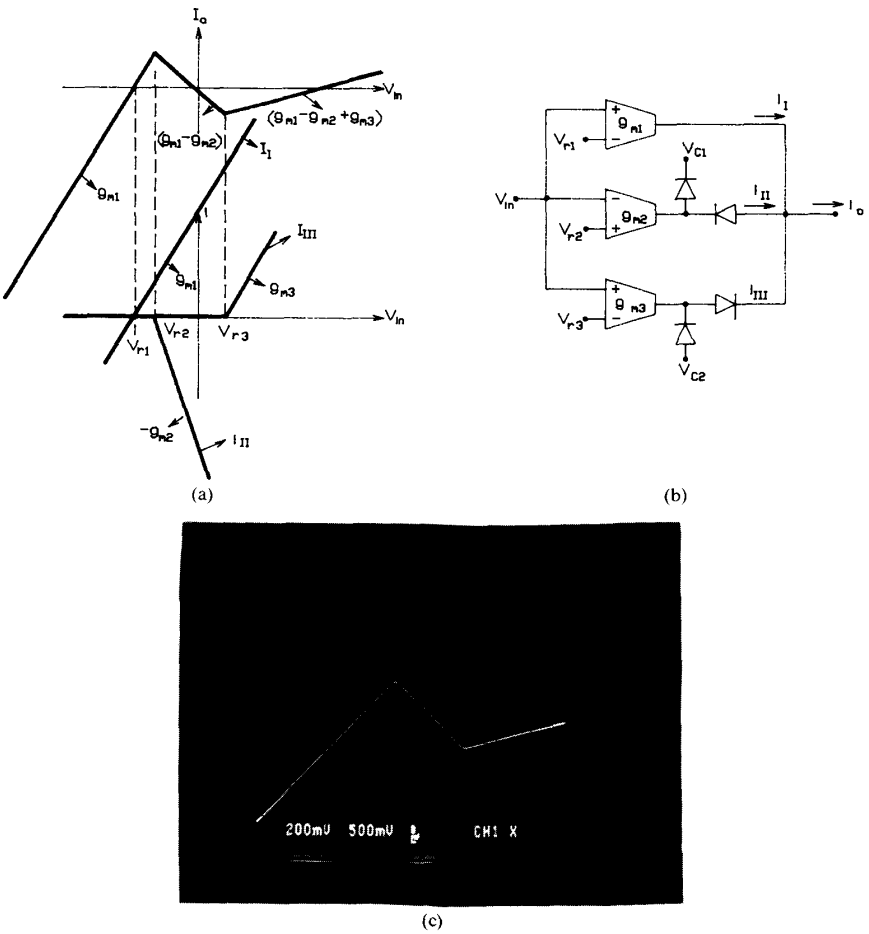


Fig. 19. Piecewise-linear approximation function: (a) transfer characteristic, (b) circuit implementation, and (c) experimental results.

analysis shows that for $v_i > 0$:

$$v_0 = \left(g_{m_1} R_{o_1} v_i - V_t\right) \cdot \frac{R_{o_2} \| \frac{1}{g_{m_2}}}{R_D + R_{o_1} + R_{o_2} \| \frac{1}{g_{m_2}}}. \quad (17)$$

Equation (17) can be simplified by assuming $1/g_{m_2} \ll R_{o_2}, R_{o_1}$. Then

$$v_0 = \frac{g_{m_1}}{g_{m_2}} \cdot \frac{R_{o_1}}{R_D + R_{o_1}} \cdot v_i - \frac{V_t}{g_{m_2}\left(R_D + R_{o_1}\right)}. \quad (18)$$

The factor $R_{o_1}/(R_D + R_{o_1})$ in the first term of the right side of (18) represents an undesired attenuation. The second term in (18) represents an offset added to the output signal which, added to the offset of the OTA, limits the minimum amplitude of the signal that can be rectified. Assuming $R_D \ll R_{o_1}$ and $R_{o_1} \cong R_{o_2}$, an estimated value for the second term is V_t/A_{V_2} where $A_{V_2} = g_{m_2} R_{o_1}$ is the voltage gain of the OTA 2. Typical values $V_t \simeq 1$ V and $A_V = 200$ result in approximately 5 mV for this second term. This is also a typical value for the offset voltage of an MOS OTA.

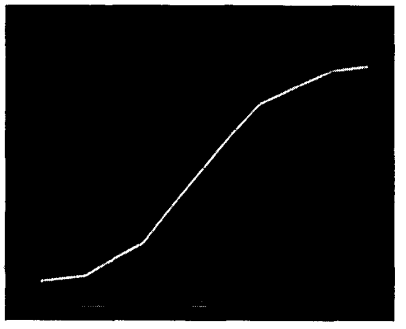
To reduce (18) to the ideal case, i.e.,

$$v_0 = \frac{g_{m_1}}{g_{m_2}} v_i, \quad \text{for } v_i > 0 \quad (19)$$

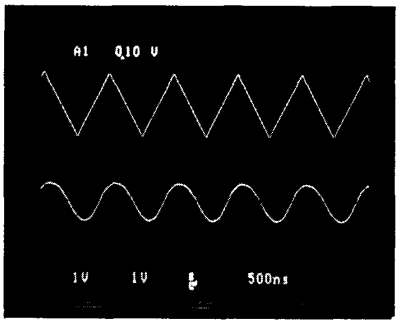
consider the following practical design considerations for low-frequency applications.

1) Use OTA's with high-voltage gain in order to minimize the offset term in (18) and design the OTA yielding the lowest possible offset voltage. Then limit the minimum input signal amplitude according to (18).

2) Select the W/L ratio of the diode-connected MOS transistor such that $R_D \ll R_o$ is satisfied. This will make $R_{o_1}/(R_{o_1} + R_D) \simeq 1$. Since the output impedance R_o of an OTA is typically very large, this condition in general does not require an excessively large value for the W/L ratio of the MOS transistor.



(a)



(b)

Fig. 20. (a) Five-segment transfer characteristic. (b) Triangular and sinusoidal waveforms at 1 MHz.

High-Frequency Analysis Considerations

The most important practical factor limiting the high-frequency operation of the circuit of Fig. 23 (see also Fig. 7) is the delay time t_D required to discharge the output capacitance C_{o_1} from the negative peak voltage $-V_S^-$ (which is charged during negative half-cycles) to the value V_t required for the diode to start conducting. Assuming, for simplicity, that the current during the negative half-cycle is entirely supplied to C_{o_1} (with the current in R_o considered negligible), the following relationship of the input signal $V_i = \hat{V}_i \sin \omega t$ involving its frequency f and the delay time t_D can be derived from $C_{o_1}(dV_{C_{o_1}}/dt) = g_m \hat{V}_i \sin \omega t$ as[6]:

$$f = \frac{I^{\text{MAX}}}{2\pi C_{o_1}(V_t + |V_S^-|)}[1 - \cos(2\pi f t_D)] \qquad (20)$$

where $I^{\text{MAX}} = g_m \hat{V}_i$ is the peak output current. Fig. 24 illustrates the typical waveform that is observed in the precision rectifier circuit of Fig. 23 for high-frequency operation when t_D becomes comparable to the period of the signal, and for the particular case $g_{m_1} = g_{m_2}$.

[6]An additional delay, not considered in the simplified analysis presented here but that can be observed in Fig. 24, is the time taken for the output signal to reach the input signal once the diode is conducting.

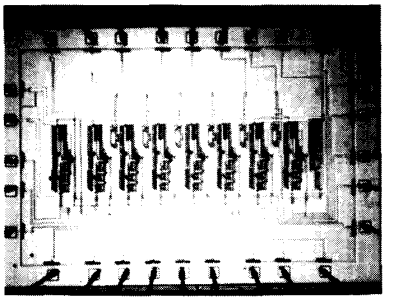


Fig. 21. Microphotograph of chip for piecewise-linear approximation.

If the maximum frequency of operation $f^{\text{MAX}} = 1/T$ is defined arbitrarily as the frequency at which $t_D = T/10$, then from (20) we obtain[7]

$$f^{\text{MAX}} = \frac{0.19 I^{\text{MAX}}}{2\pi C_{o_1}(V_t + |V_S^-|)}. \qquad (21)$$

Typical values of $g_m = 30\ \mu\text{A/V}$, $10\ \text{mV} \leqslant \hat{V}_i \leqslant 1\ \text{V}$, $A_v = g_m R_o = 100$, $C_{o_1} = 0.5$ pF, $V_t = 1$ V, and $1\ \text{V} \geqslant |V_S^-| \leqslant 5$ V result in a range of $9.07\ \text{kHz} \leqslant f^{\text{MAX}} \leqslant 302$ kHz. From (21) one can see that to increase f^{MAX} one must increase I^{MAX} (and hence the power dissipation which is typical for high-frequency circuit performance) and/or design a "better OTA" with smaller C_{o_1}.

Modification of the Basic Precision Rectifier Circuit to Improve High-Frequency Operation

Fig. 25 shows high-frequency improved versions of the OTA-rectifier circuits including a second diode[8] D_2 and a source $V_B = (V_{t_1} + V_{t_2})$ where V_{t_1} and V_{t_2} are the threshold voltages of D_1 and D_2, respectively. In this circuit the OTA1 output voltage does not go into saturation, but is limited to a minimum (maximum) value V_{t_1} $(-V_{t_1})$ during negative (positive) half-cycles. At the beginning of the positive (negative) half-cycles, the diode D_1 will be ready for conduction so that no delay due to charging or discharging of the output capacitance C_{o_1} takes place, hence $t_D = 0$.

The addition of the diode D_2 and the bias V_B allows a drastic improvement in the high-frequency performance of the circuit without excessively increasing the power consumption. Additional power dissipated still needs to be supplied by the battery V_B which absorbs the output current of the OTA through D_2 during the negative half-cycles, but this does not increase quiescent power dissipation.

The remaining high-frequency limitation of the improved circuits is related to the low-pass behavior of the rectifier. The circuit of Fig. 26 shows a high-frequency equivalent circuit of the OTA rectifier (assumed linear for

[7]Where $|V_S^-| = A_v \hat{V}_i$ for $|V_S^-| < V_{SS}$, otherwise $|V_S^-| \cong |V_{SS}|$ and V_{SS} is the negative power supply voltage.

[8]D_2 works similar to the catch diode of the op-amp version [13] of the same circuit.

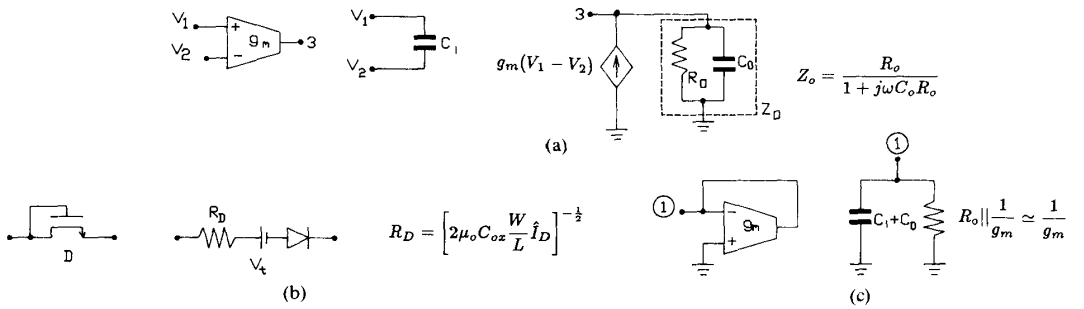


Fig. 22. (a) Equivalent circuit of nonideal OTA. (b) Equivalent circuit of diode-connected MOS transistor. (c) Equivalent circuit of OTA used as two-terminal resistive elements.

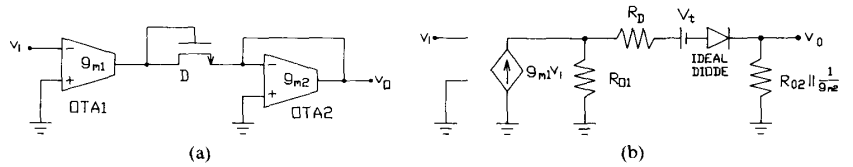


Fig. 23. (a) Basic OTA-precision rectifier. (b) Low-frequency equivalent circuit of (a).

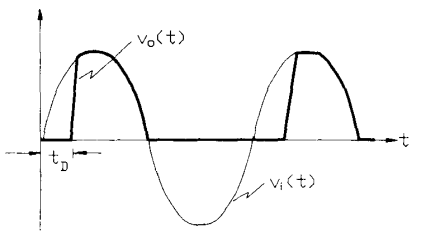


Fig. 24. Nonlinear distortion for high frequency of OTA-precision rectifier of Fig. 23(a).

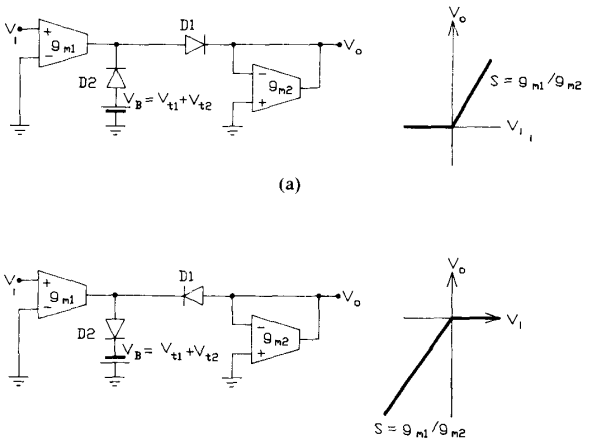


Fig. 25. Improved versions of OTA-precision rectifiers for high-frequency operation.

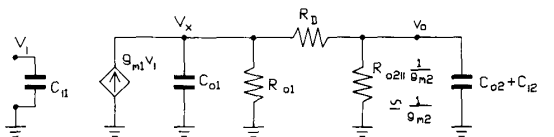


Fig. 26. Small-signal equivalent circuit of improved OTA rectifier of Fig. 25.

tractability since the nonlinear transient has been eliminated) for $v_i > 0$. The transfer function of the circuit, characterized by two poles ω_{p_1} and ω_{p_2}, is given by

$$\frac{v_o}{v_i} = \frac{g_{m_1}/g_{m_2}}{\left(1+\frac{s}{\omega_{p_1}}\right)\left(1+\frac{s}{\omega_{p_2}}\right)} \tag{22}$$

taking ω_{p_1} and ω_{p_2} into account[9] and assuming the inequalities, R_D, $(1/g_{m_2}) \ll R_{o_1}$, are satisfied. The 3-dB frequency, $\omega_{3\,\mathrm{dB}}$, can be approximated [13] by

$$\omega_{3\,\mathrm{dB}} = \frac{g_{m_2}}{C_{o_1}\left(1+g_{m_2}R_D\right)+C_{o_2}+C_{i_2}}. \tag{23}$$

If the conditions given above are satisfied, and $1/g_{m2} \gg R_D$, then we can approximate

$$\omega_{3\,\mathrm{dB}} \simeq \frac{g_{m_2}}{C_{o_2}+C_{o_1}+C_{i_2}}. \tag{24}$$

For typical values ($C_{o_2} = C_{o_1} = 0.5$ pF, $C_{i2} = 0.1$ pF, $g_m = 30$ μA/V), (24) predicts $f_{3\,\mathrm{dB}} \simeq 4.32$ MHz, which is a factor between 476 and 14 times higher than the maximum frequency attainable from the basic OTA rectifier. This corresponds to the limit set by the parameters of the OTA used. *The conclusion is, then, that the maximum frequency at which OTA precision rectifiers operate can be made as high as the OTA itself allows.*

From (23) the following design considerations can be derived to extend $\omega_{3\,\mathrm{dB}}$, which is now effectively the maxi-

[9] Where $\omega_{p_1} = \dfrac{1}{C_{o_1}\left[R_{o_1}\|\left(R_D+1/g_{m_2}\right)\right]}$ and $\omega_{p_2} = \dfrac{1}{\left(C_{o_2}+C_{i_2}\right)\left[1/g_{m_2}\|\left(R_D+R_{o_1}\right)\right]}$.

mum frequency of operation of the improved OTA rectifier circuit.

1) Design the OTA with reduced excess phase and parasitic capacitances C_{o_1}, C_{o_2}, C_{i_2}, which is, in general, an obvious requirement to improve high-frequency operation.

2) Increase g_{m_2} (and also g_{m_1} if a fixed value g_{m_1}/g_{m_2} is desired). Keep $R_D \ll 1/g_{m_2}$, that is, assign a sufficiently large W/L ratio for the MOS transistor used as diode so that its resistance is much lower than the load resistance, and the multiplying factor of C_{o_1} (in (23)) is minimized.

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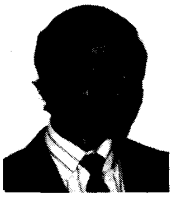

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