A 4-Mode Reconfigurable Low Noise Amplifier for Implantable Neural Recording Channels

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***Abstract*—In this paper a reconfigurable implantable low noise amplifier for the recording of neural signals is presented. It is comprised by low-power and noise efficient current reuse OTAs in its direct path. The proposed architecture allows for an active feedback to set the high-pass corner in place of the commonly used pseudoresistor. Bandwidth selectivity is achieved by cicuit reconfigurability which changes the pole frequencies of the system without impacting the total power consumption. Simulation results in AMS $0.18\mu m$ technology validate the proposed architecture in both nominal and corner process conditions with an estimated total power consumption of $454nW$.**

***Index Terms*—low noise amplifier, neural recording, low power circuit, reconfigurable amplifier**

I. Introduction

It is possible to sense two types of signals within the surface of the cerebral cortex: local field potential (LFP) and action potential (AP). The LFP has an amplitude of $(10\mu$-$1m)V$ in the $(1-500)Hz$ band while the AP has an amplitude of $(10\mu-1m)V$ in the $(250-7k)Hz$ band. Furthermore, the hippocampus of an epileptic brain exhibits an oscillation known as fast ripple (FR) in the $(250-600)Hz$ band with an amplitude of $(30\mu-1.5m)V$. Neuroscience research has proven and suggested that these signals are useful in several applications such as epileptic seizure predictors [1], general epilepsy studies [2] as well as prosthetic limb control [3] and speech decoding [4].

The acquisition of these neural signals by a reconfigurable analog front-end (AFE) is a problem that has recently generated great interest [5],[6],[7],[8]. A channel of this kind features bandwidth selectivity capabilities in order to observe the neural signals separately or simultaneously. In general, the AFE has to be able to achieve the following:

- Operate at low power due to very limited budget and to avoid the possibility of tissue damage caused by excessive heating [9].
- The input referred noise of the amplifier has to be kept below the background noise ($< 5\mu Vrms$) of the recording site.
- The tissue-electrode interface produces DC nonidealities such as offsets and drifts that must be filtered out in order to avoid amplifier saturation.

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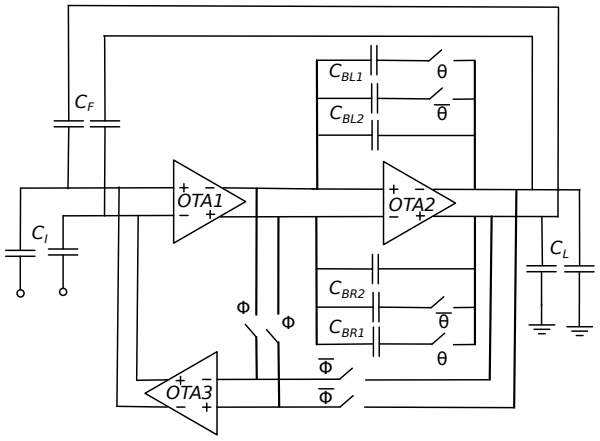

Fig. 1. Reconfigurable Low Noise Amplifier

The low noise amplifier (LNA) is the most fundamental block in a reconfigurable AFE since it determines the thermal noise floor as well as most of the power consumption in the system. Additionally, it has to be able to perform adequately for all operational bandwidths. Therefore, the challenge posed by the design of the LNA is evident.

With few exceptions, most LNAs are based on the circuit introduced in [10]. These amplifiers set a high-pass pole with a pseudoresistor and a feedback capacitor. Although this solution is successful in proof-of-concept scenarios, the nominal value of pseudoresistors shows high variability, which complicates bandwidth tuning [11]. On the other hand, most LNAs either focus only on a specific neural signal type or require subsequent specialized filters stages in order to achieve bandwidth selectivity.

In this paper, the concept of a reconfigurable LNA is presented. It features an active feedback to set the high-pass pole in place of the pseudoresistor as well as circuit reconfigurability which enables to select different neural signal bandwidths. The paper is organized as follows. Section II presents the mathematical models of the circuit for all modes of operation. Section III shows the low-power design considerations and procedure. Section IV depicts the simulation results, conclusions are given in Section V.

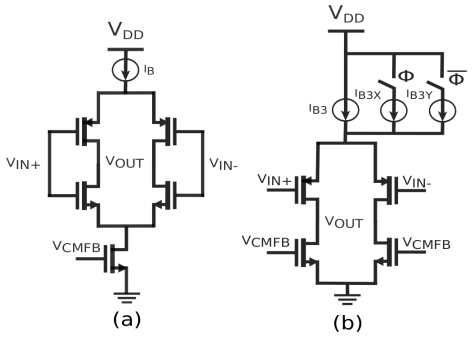

Fig. 2. a) Current reuse OTA b) Simple programmable OTA

TABLE I
MODES OF OPERATION FOR THE RECONFIGURABLE AMPLIFIER

ϕ	θ	Mode of operation
0	0	Fast Ripple
0	1	Action Potential
1	0	Local Field Potential
1	1	Full Bandwidth

II. RECONFIGURABLE AMPLIFIER

Fig. 1 shows the reconfigurable neural amplifier architecture. Its topological structure and the value of the capacitor bank C_B change according to control signals ϕ and θ. The amplifier features capacitive coupled inputs and is comprised of two cascaded current reuse OTAs as shown in Fig. 2(a). These OTAs generate the transconductance of a complementary input pair from half the current as they are biased by the same source. OTA3 performs a reconfigurable active feedback from the output of either OTA1 or OTA2. A simple differential programmable OTA as depicted in Fig. 2(b) is used since this structure is able to produce extremely low transconductance. Regardless of the mode of operation, the mid-band gain of the amplifier is given by the input and feedback capacitors as follows:

$$Gain_{Midband} \simeq \frac{C_I}{C_F}. \tag{1}$$

Small signal analysis shows that the transfer function for all modes of operation contains factors $\beta = -C_F gm_1 + C_I gm_2 - C_F gm_2 - C_{p1} gm_2$ and $\alpha = C_I C_F C_B + C_I C_F C_{p2} + C_I C_B C_{p2} - C_I C_B C_{p3} - C_I C_{p2} C_{p3} + C_I C_B C_L + C_I C_{p2} C_L$. Where C_{p1}, C_{p2}, C_{p3} and gm_1, gm_2, gm_3 are the parasitic input capacitance and transconductance of each OTA, respectively.

Four modes of operation are accomplished by changing the frequency of the three dominant poles in the system, which in turn is done by a combination of reconfigurable feedback and picoampere bias of OTA3 as well as programmability in the capacitor bank. This scheme is unlike most front-end amplifiers hitherto reported since generally, bandwidth tuning is achieved by changing the main bias current which translates as a non-constant power consumption: an undesirable feature in an implanted device. The modes of operation for the proposed reconfigurable neural amplifier are defined in Table I and are carefully examined in the following subsections.

A. Full Bandwidth Mode

When $\phi = 1$ and $\theta = 1$ the circuit enters the full bandwidth (FB) mode, which covers both the local field and action potential frequency bands. Fig. 3(a) shows a simplified diagram of this mode. Assuming $5 \cdot C_{B1} < C_L$, the first pole is

$$HPpole_{(1)FB} \simeq \frac{gm_3}{C_F A_2}, \tag{2}$$

where $A_2 = gm_2/gds_2$. A pair of complex conjugate poles sets the low-pass $-40dB/decade$ roll-off as follows:

$$LPpole_{(2,3)FB} \simeq \frac{-C_{B1}\beta \pm \sqrt{\Delta_{FB}}}{2\alpha}. \tag{3}$$

Where $\Delta_{FB} = C_{B1}^2 \beta^2 - 4\alpha C_F gm_1 gm_2$.

B. Local Field Potential Mode

The LFP mode of operation is accessed when $\phi = 1$ and $\theta = 0$ and is as depicted in Fig. 3(b). The high-pass pole is the same as the FB mode. The low-pass pole is given by one pole only and its frequency is reduced since $C_{B2} > 10 \cdot C_{B1}$ and $C_{B2} > C_L$. Therefore, the second and third poles split and are defined as

$$LPpole_{LFP} = Pole_{(2)LFP} \simeq \frac{C_F gm_1 gm_2}{C_{B2}\beta}, \tag{4}$$

$$Pole_{(3)LFP} \simeq \frac{C_{B2}\beta}{\alpha}. \tag{5}$$

As a consequence, the frequency response of the LFP mode exhibits a $-20dB/decade$ roll-off.

C. Action Potential Mode

Fig. 3(c) shows the AP mode. A topological change is completed when $\phi = 0$ and $\theta = 1$ meaning that OTA3 now feedbacks from the output of OTA2. This has the following effect on the high-pass pole,

$$HPpole_{(1)AP} \simeq \frac{gm_3}{C_F}. \tag{6}$$

Eq. (6) shows that by removing A_2 the high-pass pole moves to a higher frequency. An even higher frequency is achieved if $I_{B3Y} > I_{B3X}$ is considered. The second and third poles are described by Equation 3 as well since C_{B1} is set as the feedback capacitor.

D. Fast Ripple Mode

The amplifier enters FR mode as depicted in Fig. 3(d) when $\phi = 0$ and $\theta = 0$. The bandwidth is set by a combination of the AP high-pass pole and LFP low-pass pole. The high-pass pole is thus described by Equation 6 (considering $I_{B3Y} > I_{B3X}$ as well) while Equations 4 and 5 describe the second and third poles of the FR mode transfer function.

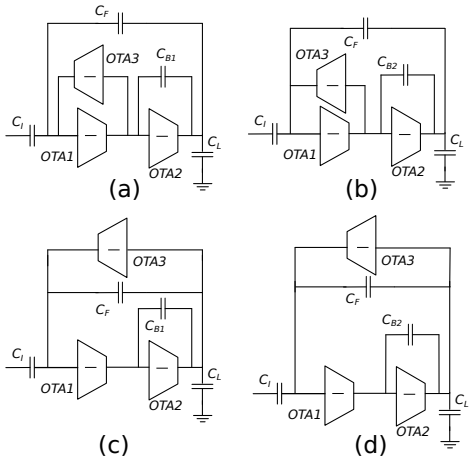

Fig. 3. Reconfigurable Modes. a) Full bandwidth mode b) Local field potential mode c) Action potential mode d) Fast ripple mode

III. Circuit Design

In order to obtain maximum transconductance efficiency, the differential pairs of amplifiers in low-power circuits are normally biased in the weak inversion region. The trancon-ductance of OTA1 and OTA2 in weak inversion is

$$gm_{(1,2)} = \frac{I_{B(1,2)}}{nVt} \tag{7}$$

where n is the sub-threshold slope and Vt is the thermal voltage. In the case of OTA3, the transconductance is given by

$$gm_3 = \frac{I_{B3}}{2nVt}. \tag{8}$$

Noise is a critical concern in the design of low-power circuits. In this amplifier, the main noise generator is the differential pair of OTA1. Achieving minimal contribution of $1/f$ noise is possible once large transistor areas are used, however, thermal noise is unavoidable. The input referred noise of the amplifier can be approximated as follows

$$\overline{Vni^2_{rms}} \simeq \frac{4kT\gamma nVt}{I_{B1}}\Delta_f, \tag{9}$$

where $\gamma = 1/2$ in weak inversion and Δ_f is the bandwidth of the amplifier, which is approximated to the value of the low-pass corner. In the proposed amplifier, C_B is the dominant term in the bandwidth for every operation mode. This feature allows to set up Δ_f and $\overline{Vni^2_{rms}}$ relatively independently. This has to be done with caution so as not to lead to instability.

Taking into account the previous remarks, the design starts by biasing OTA1 in weak inversion with a thermal noise floor of $\sim 50nV/\sqrt{Hz}$ in the FB mode while ensuring large differential pair area to combat $1/f$ noise. Adequate noise performance is obtained for the rest of the modes of operation by setting up the noise in this mode. Total power consumption is kept low by biasing OTA2 in weak inversion with the minimal possible current while maintaining stability and high enough gain. OTA3 is biased with an extremely small

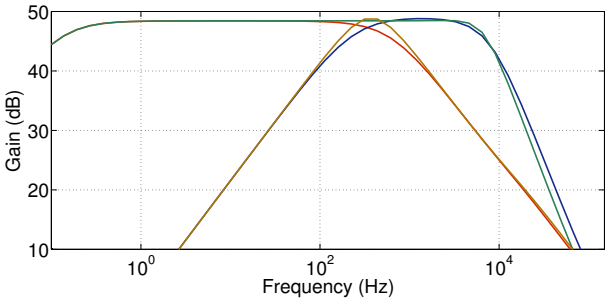

Fig. 4. Frequency Response for Reconfigurable Modes. FB in green, LFP in red, FR in Yellow, AP in Blue.

picoampere current so as to keep a $< 1Hz$ high-pass pole in the FB and LFP modes. This current is barely increased for the AP and FR modes to the point that its impact on the total power consumption is still negligible. Capacitor bank C_B is sized according to the bandwidth targets for each mode.

IV. Simulation Results

The circuit was simulated in Cadence-Spectre considering a behavioral common-mode feedback block and the AMS $0.18\mu m$ process. Bias voltage was set to $1V$, $C_I/C_F = 40pF/155fF$ and $C_L = 4.6pF$. Fig. 4 shows the frequency response for each of the reconfigurable modes. The predicted behavior from the mathematical models in the previous section is hereby verified. However, a slight difference in the estimated low-pass corner between the AP and FB modes is seen. This difference is probably due to the input parasitic capacitance of OTA3 which is added to the output node in the AP mode. Fig. 5 shows the total harmonic distortion for the four modes. It can be seen that at $1mV$ the circuit in all modes shows a $< 1\%$ distortion, which validates the input swing capabilities of the proposed circuit.

Process variations simulation show a low-pass corner frequency spread of $\Delta f_{LP} = \pm 2.5kHz$ for FB and AP modes and $\Delta f_{LP} = \pm 200Hz$ for the LFP and FR modes. Fig. 6(a) shows how a 3-bit $C_B \in [247fF, 1.23pF]$ is able to compensate the low-pass corner variations for the FB and AP modes. The low-pass corner variations for the LFP and FR modes can be compensated by a 3-bit $C_B \in [7.1pF, 15.1pF]$ as shown in Fig. 6(b). In a similar fashion, the high-pass corner can be tuned by changing I_{B3} as seen in Fig. 7. Table II further dissects the performance of the simulated circuit. All modes maintain an adequate noise performance while keeping the same power consumption. No comparison with the state of the art is made since we believe simulation results shouldn't be compared with experimentally verified work.

V. Conclusions

A new reconfigurable LNA for neural recording was introduced and verified through simulations. The LNA is capable of switching between four modes of operation that cover the most relevant neural signal bandwidths without impacting the total power consumption. The circuit characteristics are ideal

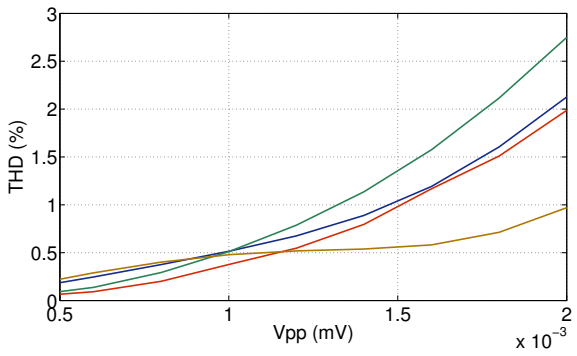

Fig. 5. Total Harmonic Distortion for Reconfigurable Modes. FB in green, LFP in red, FR in Yellow, AP in Blue.

TABLE II
SIMULATION RESULTS FOR RECONFIGURABLE MODES

	FB	LFP	AP	FR
Gain (dB)	48	48	48	48
Power (nW)	454	454	454	454
High Pass (Hz)	0.129	0.129	224	224
Low Pass (Hz)	7k	590	6.8K	590
Integrated Input Noise ($\mu Vrms$)	5.76 (1-7k)Hz	4.2 (1-590)Hz	4.1 (224-6.8k)Hz	1.24 (224-590)Hz
THD (%)	0.5@1mVpp 1kHz	0.37@1mVpp 100Hz	0.5@1mVpp 1kHz	0.47@1mVpp 400Hz
C_B (pF)	0.68	9.1	0.68	9.1
NEF	1.79	4.5	1.31	1.68

for the first stage in a neural recording channel. The simulated power consumption suggests that the eventually fabricated chip will be the lowest power consuming circuit of its kind. A design in a smaller channel length process might be able to further reduce the power consumption of the circuit since the threshold voltage of the transistors is smaller.

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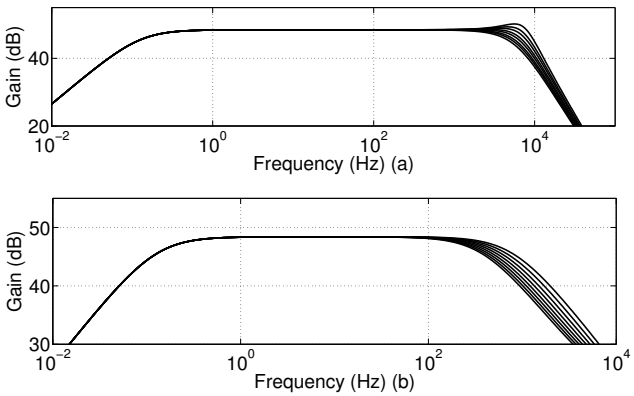

Fig. 6. Low-pass corner tuning a) FB mode, valid also for AP b) LFP mode, valid also for FR.

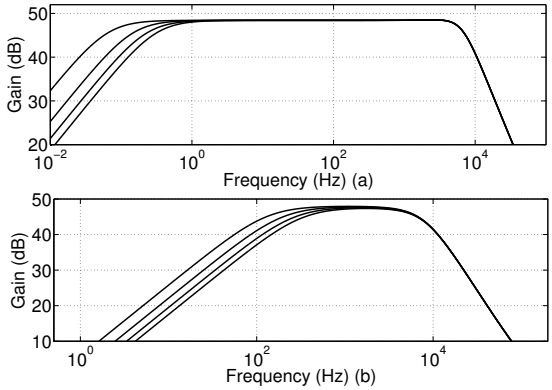

Fig. 7. High-pass corner tuning a) FB mode, valid also for LFP b) AP mode, valid also for FR.

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