A 76nW, 4kS/s 10-bit SAR ADC with offset cancellation for biomedical applications

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***Abstract*—This paper presents a 10-bit fully-differential rail-to-rail successive approximation (SAR) ADC designed for biomedical applications. The ADC, fabricated in a 180nm HV CMOS technology, features low switching energy consumption and employs a time-domain comparator which includes an offset cancellation mechanism. The power dissipated by the ADC is 76.2nW at 4kS/s and achieves 9.5 ENOB.**

I. Introduction

Implantable biomedical devices are continuously increasing their degree of complexity. Most recent proposals often include sophisticated signal processing sections, together with the tissue interface and means for data transmission. This allows (i) to increase the autonomy of the devices, as they can operate in an essentially unsupervised manner, (ii) to relax the specifications of the communication link, as raw data are internally processed and only relevant features have to be transmitted, and (iii) to make it possible new applications such as the implementation of closed-loop neurodevices for the treatment of epilepsy [1] or movement disorders [2].

Power consumption saving is a major objective in the implementation of these systems on chip. This is favored by the mild digital processing specifications, which usually has to handle medium resolution (around 10-b) and low sampling frequency signals (typically below 100kS/s). However, besides energy efficiency, care must be taken on preserving the integrity of the captured signals so that the embedded processing also proves accurate. In particular, dc offsets may have deleterious effects on typical biomedical processing blocks. Some examples are those implementing threshold-related detection algorithms, commonly used in the analysis of neural action potentials [3] or heart rates [4], or those focused on the energy extraction of signals in relevant frequency bands, often employed in the analysis of neural local field potentials or EEG signals [5]. In the former, events might be erroneously skipped whereas, in the latter, signal-dependent terms contaminate energy calculation. Hence, offsets have to be suitably canceled before any signal processing task takes place.

In this paper, a low-power offset-canceling SAR ADC is presented. The offset cancellation technique takes advantage of a programmable time-domain comparator with little area and power consumption overhead, and makes unnecessary any additional dc suppression block in digital domain. The paper is organized as follows. Sec. II presents the ADC architecture and describes the conversion procedure. Then, Sec. III shows the time-domain comparator of the ADC and describes the foreground mechanism for the offset cancellation of the converter. Afterward, Sec. IV gives experimental results measured on the fabricated ADC and, finally, Sec. V briefly concludes the paper.

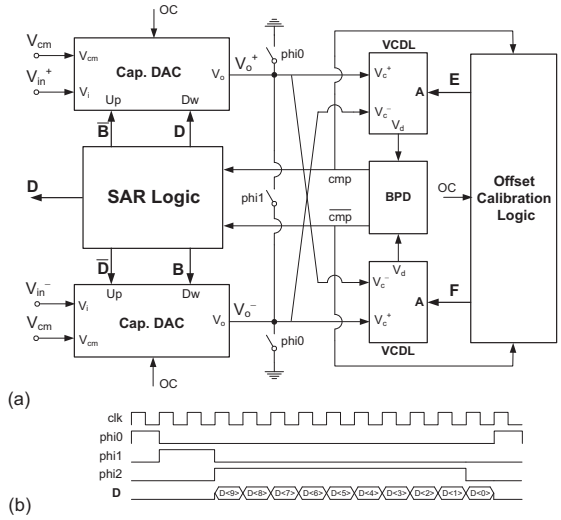

Figure 1. ADC architecture and clock phases.

II. ADC architecture and conversion procedure

Fig. 1(a) shows the architecture of the proposed 10-b rail-to-rail fully-differential ADC. It consists of two capacitive DACs, a time-domain comparator, a SAR logic block and an offset calibration circuit. The comparator includes two digitally programmable Voltage-Controlled Delay Lines (VCDL) which are driven by the output voltages of the capacitive DACs, and a Binary Phase Detector (BPD) which obtains the result of the comparison based on the phase difference between the output signals of the VCDLs. A control module, not shown in Fig. 1(a), defines the clock phases and the operation mode of the converter. Two operation modes are available: (i) *calibration* (control signal *OC* = '1'), in which the VCDLs are adjusted to cancel out the dc offset of the whole converter, and (ii) *conversion* (control signal *OC* = '0'), in which the input voltage V_{in} is normally digitized.

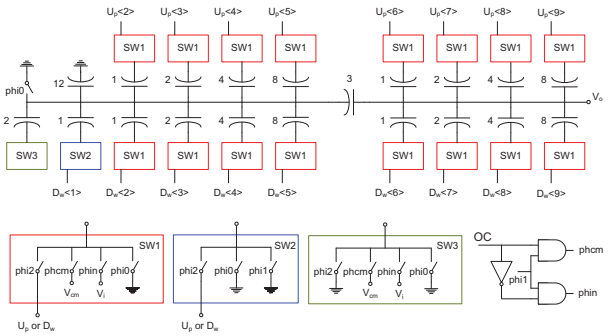

Figure 2. Capacitive DACs and switch arrangements.

The converter operates with three clock phases, derived from a master clock signal, clk. They are illustrated in Fig. 1(b). During the reset phase, $phi0$, both DACs are fully discharged and the different logic blocks are initialized for a new conversion. Phase $phi1$ defines the sample phase of the capacitive DACs which are charged either with the input voltages V_{in}^{+} and V_{in}^{-} (conversion mode) or by the input common mode voltage V_{cm} (calibration mode). During this phase, which lasts two master clock cycles to relax the driving strength of the converter previous stage, the DAC outputs are connected together. During phase $phi2$, the capacitor arrays are disconnected and the sampled signal is converted.

The ADC uses three different supply voltages. The capacitor arrays are supplied from $V_{DDA} = 1\text{V}$; the SAR logic block uses $V_{DDH} = 0.5\text{V}$; and the remaining blocks employ $V_{DDD} = 1\text{V}$. Level shifters at the outputs of the SAR logic block are used for driving the switches of the capacitive DACs.

Fig. 2 shows the structure of the capacitive DACs. Each DAC uses a bridged capacitor array controlled by two programming words, denoted as Up and Dw. Capacitors are built by parallel connecting multiple instances of a unit MiM capacitor, as indicated by the numbers in Fig. 2. Three different switch arrangements, identified as $SW1$, $SW2$ and $SW3$, are employed in the DACs. Boosted switches, controlled by signals $phin$ and $phcm$, are used for sampling, whereas conventional transmission gates are employed for loading the programming words. Simple nmos transistors are used for connecting to ground the top and bottom plates of the capacitors during reset. Signals $phin$ and $phcm$, aligned to phase $phi1$, are selected according to the operation mode. Note that 12 unit capacitors in the DAC have their bottom plates permanently connected to ground and that $SW2$ and $SW3$ have different roles during sampling or conversion as compared to $SW1$. This is done to guarantee mid-thread uniform quantization with 2^{10} voltage intervals in the ADC and, additionally, to make the DAC outputs converge towards mid-rail along the conversion process.

The conversion process is illustrated in Fig. 3. It uses two programming words **B**<9:1> and **D**<9:0> (see Fig. 1) which are updated according to the comparator output. Once the sampling phase is over, **B** and **D** are initially set to **0** and the comparator makes a first comparison. If $V_o^{+} > V_o^{-}$, the comparator gives *cmp* = '1' and the most significant bit of **D** changes to D<9> = '1', while vector **B** remains unaltered.

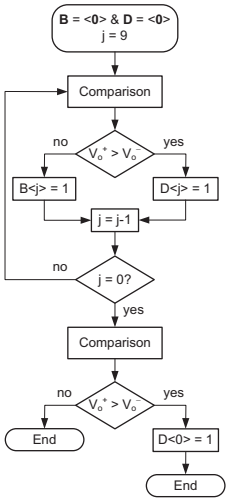

Figure 3. Flow diagram of the conversion process.

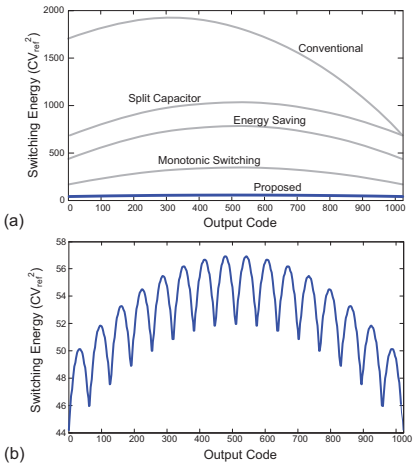

Figure 4. Switching energy vs output code.

Otherwise, the output of the comparator is *cmp* = '0' and the most significant bit of **B** changes to B<9> = '1', while vector **D** is not modified. Afterward, a new comparison is made and the following bits in **B** and **D** are similarly solved. Once the bits D<1> and B<1> are set, a last comparison is carried out and the *cmp* value is stored in D<0>. Vector **D** constitutes the conversion output.

Note that, for each bit cycle, only one capacitor per DAC is switched at a time during conversion. This, together with the reduced number of unit capacitors per DAC (only 78), considerably benefits the energy efficiency of the converter. This is illustrated in Fig. 4(a) which shows the normalized switching energy versus output code for different SAR ADC architectures. The energy performance of the proposed ADC is further detailed in Fig. 4(b). As it can be seen, the proposed technique consumes less energy than the other approaches [6]–[9] at the price of some extra circuits in the SAR logic block for handling the auxiliary vector **B**. This is partially compensated by reducing the power supply of the SAR logic to $V_{DDH} = 0.5\text{V}$.

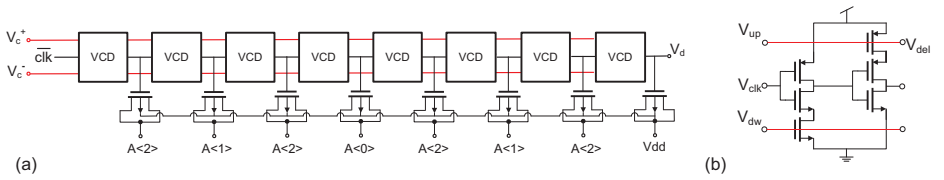

Figure 5. (a) Delay line. (b) Voltage controlled delay element.

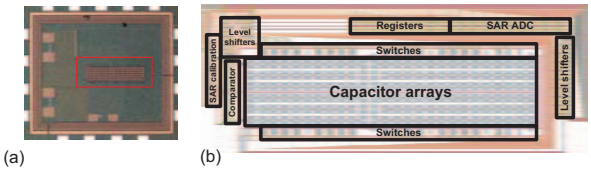

Figure 6. Photograph (a) and layout (b) of the SAR ADC prototype.

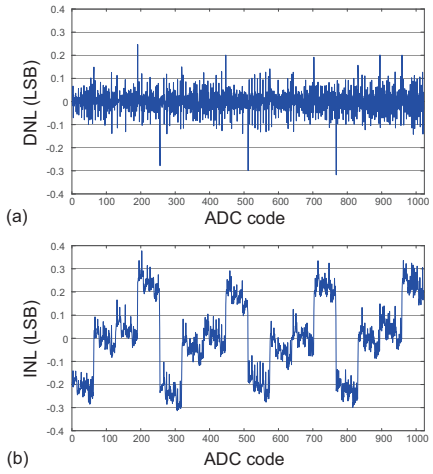

Figure 7. INL and DNL.

III. Programmable Comparator and Offset Cancellation Process

The proposed offset cancellation technique relies on the programmability of the VCDLs. Fig. 5(a) shows the block diagram of the proposed VCDL which consists of 8 Voltage Controlled Delay (VCD) stages. As shown in Fig. 5(b), each delay stage comprises a cascade of two current-starved inverters [10] which are respectively controlled by the outputs of the capacitive DACs (see Fig. 1). Inversion-mode pmos varactors are gate-connected to the outputs of the VCD elements [11]. A 3-b programming word sets the source node voltages of the first 7 varactors, whereas the source of the last varactor is permanently connected to V_{DDD}. Taking advantage of the bias-dependent capacitive load offered by the varactors, the propagation delay of the VCDLs can be digitally controlled. In this design, the tuning range allowed by the total of varactors amounts about $\pm 4\%$ of the total delay of the VCDL.

By exploiting this tuning capability, a foreground mechanism for the offset cancellation of the converter has been implemented. This mechanism requires, at most, four conversion cycles and uses a binary search algorithm for solving the VCDL programming words, **E** and **F** (see Fig. 1). An auxiliary SAR logic block supervises the calibration process and stores the resulting vectors **E** and **F** for use during normal conversion. Once the calibration is completed, the auxiliary SAR is disabled.

The offset cancellation process is as follows. Upon setting OC = '1', all varactors are connected to V_{DDD} and, hence, vectors **E** and **F** are initialized to '**1**'. Afterward, the ADC samples and converts the input common mode voltage V_{cm}. If the result is above or below the mid-range codes '511' or '512', the calibration SAR block runs a conventional three-step binary search algorithm on the programming word of the slower VCDL. Meanwhile, the control vector of the faster VCDL is kept at '**1**'. At each step of the search algorithm a new conversion cycle takes place using V_{cm} as input, and the result is compared to the mid-range codes. If the converted value is equal to '511' or '512', the calibration process finishes. Otherwise, the control bits of the slower VCDL are sequentially solved up to the LSB.

In order to guarantee the calibration procedure always ends at the mid-range codes, no matter the process corner or the impact of mismatch, the possible variations of the propagation delays between the VCDLs have to be solely compensated by the tuning range provided by the varactors in one of the chains. The larger the length of the VCDL and the number of bits of the controlling word, i.e., the higher the number of varactors, the wider the offset range that can be canceled out. However, this also increases the area and power consumptions of the whole time-domain comparator. In the presented design, which has been exhaustively verified with PVT and Monte Carlo simulations, the programmable time-domain comparator is able to minimally cancel up to ± 5 LSB dc offset deviations with only 28.6nW power consumption from 1V supply an a tiny area occupation of $20 \times 70 \mu\text{m}^2$.

IV. Measurement Results

The ADC has been fabricated in a 0.18μm HV CMOS technology. Fig. 6 shows the die photograph together with the converter floorplan. The active area occupation is only 0.071mm^2. The input range is 2V_{pp} differential. With a 100Hz input sampled at 4kS/s, the INL and DNL are -0.31/0.38 and -0.31/0.25, respectively (see Fig. 7). Figs. 8 and 9 illustrates the dynamic performance of the ADC. Along the whole Nyquist band, the converter obtains around 70dB of Spurious-Free Dynamic Range (SFDR), above 60dB of Signal to Noise and Distortion Ratio (SNDR) and an Effective Number of Bits (ENOB) higher than 9.5-b.

Fig. 10 shows a snapshot of the network analyzer (Agilent 16902B) used in the test-bench to illustrate the offset cancellation process. After a reset phase, the ADC enters in calibration mode, and the input common mode voltage is sampled in both capacitive DACs. After a first conversion cycle, the ADC obtains a value of '513' which corresponds to 1-LSB offset. In the following three conversion cycles, the programming words

Table I
COMPARISON WITH STATE-OF-THE-ART SAR ADCS IN SIMILAR TECHNOLOGIES.

	[12]	[13]	[14]	[15]	[16]	[17]	[18]	**This work**
Technology (μm)	0.18	0.18	0.13	0.13	0.18	0.18	0.13	0.18
Power	31nW	1.35μW	3.02mW	1.1μW	98μW	1.3μW	0.92mW	76.2nW
Supply (V)	0.5	0.45	1.2	1.2	1	0.6V	1.2	1/0.5
Sampling rate	4kS/s	200kS/s	45MS/s	31.3kS/s	10MS/s	100kS/s	50MS/s	4kS/s
ENOB	9.55	8.27	10.85	9.72	9.83	8.7	8.48	9.5
Area (mm^2)	0.12	-	0.059	-	0.086	0.125	0.075	0.071
FoM (fJ/c-s)	17	22	36.3	42	11	31	52	26.3

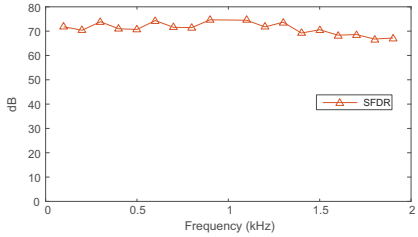

Figure 8. SFDR versus input frequency.

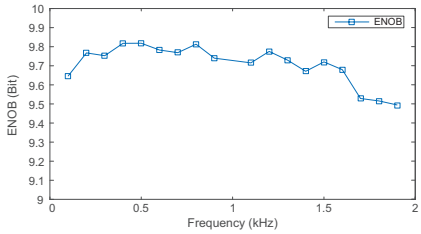

Figure 9. ENOB versus input frequency.

of the VCDLs are adjusted until the output reaches the desired value (in this case, '511'). At this point, the calibration process concludes and the ADC is ready for normal data conversion. For all the 25 tested samples of the ADC, the calibration mechanism successfully canceled the offset.

The ADC consumes 76.2nW at 4kS/s to give a FoM of 26.3fJ/conversion step. A summary of the ADC is listed in Table I together with other state-of-the-art SAR ADCs in the literature, using a similar technology process. Our solution obtains a comparable FoM with small area occupation and features an offset cancellation mechanism not available in the other proposals.

V. CONCLUSIONS

A 10-b fully-differential rail-to-rail SAR ADC with offset cancellation capability has been presented. Such offset correction mechanism relies on a time domain comparator, tunable by means of varactors, and a dedicated SAR block. The DAC architecture of the converter has been carefully designed seeking on the reduction of the switching energy consumption.

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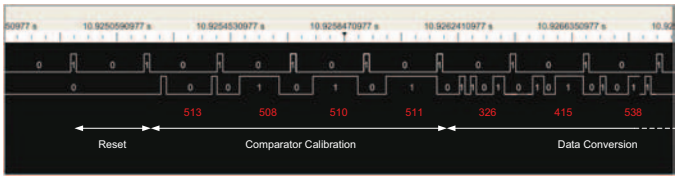

Figure 10. Illustration of the offset cancellation process.

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