A Low-Power Reconfigurable ADC for Biomedical Sensor Interfaces

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Abstract – This paper presents a 12-bit low-voltage low-power reconfigurable Analog-to-Digital Converter (ADC). The design employs Switched Capacitor (SC) techniques and implements a Successive Approximation (SA) algorithm. The ADC can be tuned to handle a large variety of biopotential signals, with digitally selectable resolution and input signal amplitude. It achieves 10.4-bit of effective resolution sampling at 56kS/s, with a power consumption below 3μW from a 1V voltage supply.

I. INTRODUCTION

Fig.1 shows the typical block diagram of a bio-potential acquisition interface. It includes a band-pass low-noise amplifier (which selects and amplifies the signal of interest and rejects the DC offset introduced by the electrodes), followed by a programmable gain amplifier and then by an ADC. Commonly the ADC is realized by using a Successive Approximation (SA) architecture to reduce power consumption [1-3].

Since different bio-potential signals pose different constraints on the block specifications, optimum operation with a single system requires tunable blocks. The circuit in [3] incorporates programmability of both the bandpass frequency and gain of the front-end interface. However, for optimum power consumption the ADC must be tunable as well. This paper reports a reconfigurable SA-ADC which can adapted to different bio-potential acquisition applications and environmental conditions.

SA-ADCs consist of a Sample&Hold (S&H) circuit followed by a feedback loop which implements a binary search algorithm. Such a loop is composed by a comparator, a Successive Approximation Register (SAR) logic block, and a *N*-bit Digital-to-Analog Converter (DAC). Most often, and particularly for low resolution applications (below 10bit), the DAC is realized through passive, charge redistribution capacitor arrays [1-3]. In these architectures the capacitor sizes impact on the ADC resolution such that both the area occupation and the power consumption increase very rapidly with the targeted ADC resolution. This feature is disadvantageous for programmability. Moreover, these structures exhibit very high sensitivity to parasitic capacitances. Parasitics of 3% with respect to the nominal capacitance may induce a 1-bit degradation of the effective resolution. This is an important drawback in modern technologies where MiMs capacitors are being replaced by MoMs structures with larger parasitic capacitances – as high as 20% of the nominal.

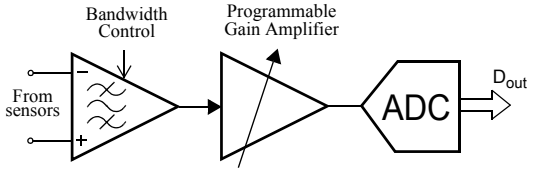

Fig. 1: Typical biosensor interface architecture.

This paper presents a 12-bit charge redistribution SA-ADC which employs active Switched-Capacitor (SC) techniques, instead of passive capacitive DACs, to implement the binary search algorithm. The ADC follows an operation principle similar to that in [4], but only uses a fully-differential opamp and a comparator to reduce as much as possible the power and area consumptions. The ADC requires less than 3μW to obtain 10.4-bit effective resolution (worst case) at 550kHz clock frequency under 1V supply. The gain of the proposed ADC can be programmed through a 3-bit digital control word between x1 and x8, thus allowing either to relax the specifications of the programmable gain amplifier in Fig.1 or even replace its function. The ADC resolution and the ADC conversion rate can be tuned within the 6-bit to 12-bit range and within the 10kS/s to 100kS/s range, respectively. Active blocks are made programmable (using a 2-bit control word) so that their power consumptions scale in accordance with the required resolution and conversion rate. The ADC occupies 0.12mm^2 including the input gain stage.

The paper is structured as follows. Section II describes the architecture of the ADC. The design of the most critical blocks is detailed in section III. Section IV illustrates the performance of the converter. Finally, section V compares the proposed ADC with capacitor-based charge redistribution solutions.

II. ARCHITECTURE OF THE SA ADC

Fig.2 shows the operation principle and timing diagram of the proposed SA-ADC, where Φ_1 and Φ_2 are non-overlapping clocks. It consists of a S&H block, an integrator and a divide-by-two circuit. The input is first sampled by the S&H and then transferred to the integrator. Afterwards, the stored voltage is compared with a threshold to determine the Most Significant Bit (MSB). Depending on the comparison result, voltage

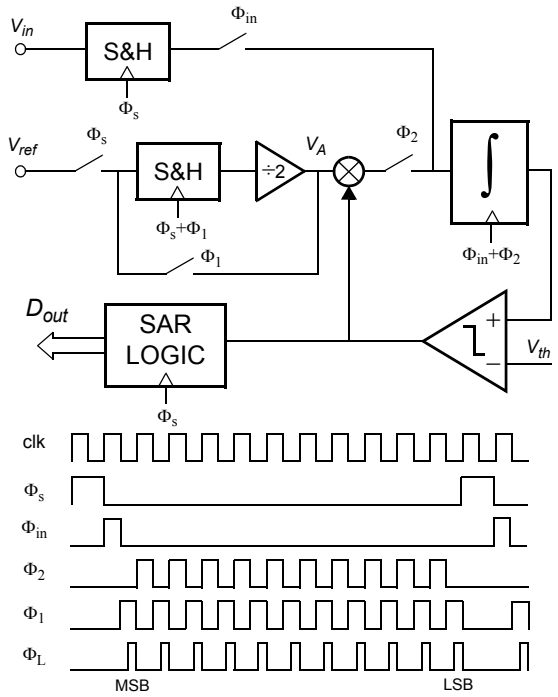

Fig. 2: Block diagram of the proposed SA A/D converter.

V_A, initially set to $V_{ref}/2$, is either added or subtracted from the integrated voltage. The newly accumulated value is compared again with the threshold to set the following bit of the conversion. The procedure repeats until the magnitude of the increments is $V_{ref}/2^{N-1}$, where N is the target resolution.

Fig.3 shows the schematic of the proposed Fully-Differential (FD) SA-ADC based on this algorithm. Reference voltage division and S&H operations are realized by passive SC circuits. Offset and gain errors of the opamp are cancelled to a first order by means of capacitors C_{off} [5]. FD operation reduces charge injection errors, is less susceptible to common-mode noise and provides a larger output voltage swing – an appealing feature for low-voltage applications. Note also that, for given ADC resolution, the capacitor count of this topology is much lower than that of capacitive-based DAC architectures. Hence, FD operation does not report area penalty.

Circuit operation is divided into two cycles denoted, respectively, as signal acquisition cycle and conversion cycle. The former starts with the sampling phase ($\Phi_S = 1$) during which the input data is stored on C_{var}. Additionally, the reference voltage V_{ref} is stored on C_1, the opamp offset is stored on C_{off} and the voltages across capacitors C_{int} and C_2 are cancelled. In the next phase, Φ_S is OFF, Φ_{in} is ON, and the charge stored in C_{var} is transferred to C_{int} so that the differential output voltage of the integrator becomes $(C_{var}/C_{int})V_{in}$. Note that if C_{var} is realized with a digitally-programmable capacitor array, the amplitude of the ADC input signal can be made externally selectable. During the next phase ($\Phi_{in} = 0$ and $\Phi_1 = 1$), the sign of the integrator output voltage is detected by means of the comparator. If $v_{in} > 0$, $v_{comp} = 1$ and the MSB (Most Significant Bit) of the conversion is set to "1", otherwise, the MSB is "0".

Afterwards, the conversion cycle starts by turning Φ_2-controlled switches ON. During this phase (Φ_1 is OFF), assuming that $C_1 = C_2$, half of the charge stored on C_1 is transferred to C_2 and, hence, to the integrator. Assuming that $C_2 = C_{int}$ and depending on the value of the previous comparison, either Φ_{2neg} or Φ_{2pos} is active, producing either a decrement or an increment by $V_{ref}/2$ in the output voltage of the integrator, respectively. During the next phase Φ_1 is ON (Φ_2 is OFF), the sign of the stored voltage determines the next most significant bit and capacitor C_2 is reset. Phases Φ_2 and Φ_1 are alternatively repeated until the required N-bit digital representation is obtained. Note that because of the charge sharing operation between capacitors C_1 and C_2, the magnitude of the increments/decrements are progressively decreasing from $V_{ref}/2$ to $V_{ref}/2^{N-1}$. Therefore, the ADC requires $N+1$ clock periods to complete the conversion. It is worth noting, that the resolution of the proposed architecture can be easily controlled by digitally setting the number of clock periods during the conversion cycle.

In order to minimize mismatch and charge injection errors, the unity capacitor is 1pF.

III. DESIGN OF THE SA-ADC BLOCKS

Critical building blocks to the performance of the SA converter are the comparator and the FD opamp.

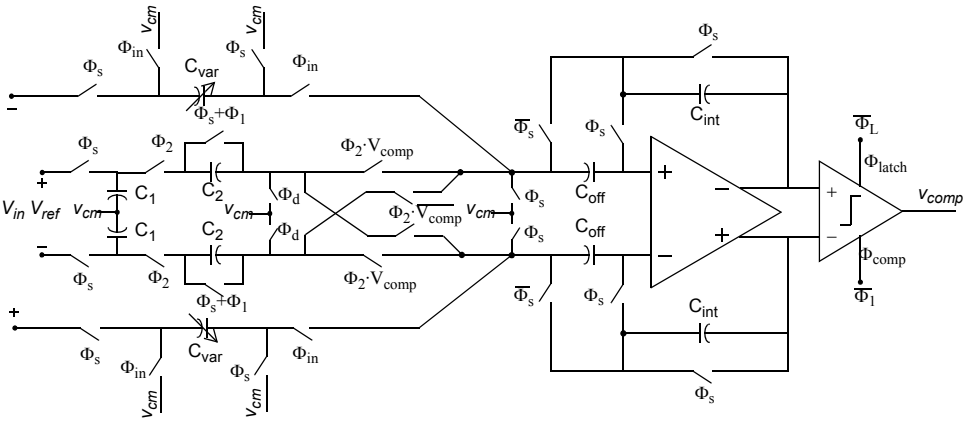

Fig. 3: Simplified schematic of the proposed fully differential SC-based SA-ADC architecture.

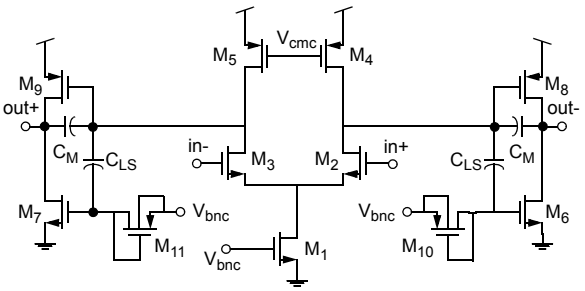

Fig. 4: Class AB fully-differential opamp with dynamic level shifter.

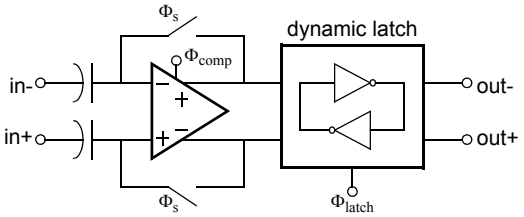

Fig. 5: Two-stage input offset storage comparator schematic.

A. Fully Differential Operational Amplifier

Fig. 4 shows the OTA used in the integrator of the ADC. It is a fully-differential class-AB two-stage Miller-compensated amplifier [3]. Class-AB operation is achieved through a push-pull output scheme (through capacitors C_{LS}), which drives both the nMOS and pMOS transistors of the second stage of the ADC. Capacitors C_M do the Miller compensation. All transistors work in sub-threshold region. Transistors M_{10} and M_{11} operate in deep sub-threshold region and exhibit very high channel resistance. They are used to set the voltage across capacitors C_{LS}. The continuous-time common-mode circuitry, not shown in Fig. 4, uses a conventional two differential pair topology and controls the common-mode through V_{cmc} [8].

In order to include programmability on this block, the multiplicity of transistors M1, M6 and M7 is selectable, controlling the bias current of the opamp and adapting it to the required bandwidth [3]. In order to fit conversion rates ranging from 10kS/s to 100kS/s, the GBW can be programmed from 500kHz to 5MHz, keeping 60dB DC-gain with power consumptions ranging from 400nW to 1.6µW through two bits of control.

B. Comparator

Due to the fact that the ADC has to detect differential voltages below 1mV, an auto-zeroed comparator composed of a preamplifier and a dynamic latch is used to accomplish the desired resolution [7]. Fig.5 shows the structure of the comparator.

The pre-amplifier uses a nMOS input differential structure. Auto-zeroing is achieved by closing a unity gain loop around the pre-amplifier and storing the offset voltage on the input capacitors [7]. This stage yields a worst-case dynamic gain of around 40dB in 1μs, which is high enough to counteract the large input offset of the dynamic latch. The bias current of this block can be also programmed to adapt its power consumption to the required resolution and conversion rate. The power consumption of the overall comparator varies from 250nW to 1µW.

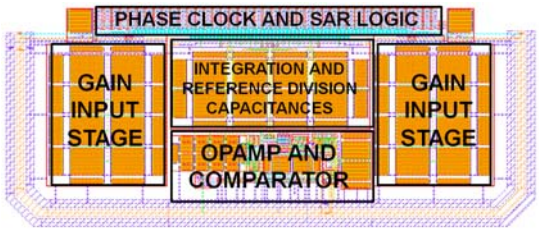

Fig. 6: Layout of the SA-ADC.

IV. SIMULATION RESULTS

The layout of the ADC, designed in ST 90-nm CMOS technology, is shown in Fig.6. Table I collects its main characteristics obtained from post-layout simulations under **P**rocess, **V**oltage and **T**emperature (PVT) variations and device mismatch.

TABLE I. Characteristics of the ADC

Resolution	6-12bit
Technology	ST 90nm
Voltage supply	1V
Conversion Rate	56kS/s
ENOB (1kHz input @ 1V supply)	10.4bit
SNDR (1kHz input @ 1V supply)	64.37dB
Gain error	0.05% FS
Offset error	0.1 LSB
Estimated Power Consumption @ 1V supply	3µW
Area	0.12mm^2

Fig.7 shows the results of a FFT analysis of the ADC, operating in 12-bit mode, for a 760Hz full-scale input tone, assuming nominal PVT. The conversion rate is 56kS/s with a 784kHz clock frequency and 1-V supply. It can be observed that all the spurious are below 74dB and the SNDR is 64.37dB, which corresponds to an ENOB of 10.4bit.

V. COMPARISON WITH CAPACITIVE DAC SOLUTIONS

The proposed architecture is advantageous versus capacitive DAC-based solutions regarding power consumption, area occupation and sensitivity to parasitic

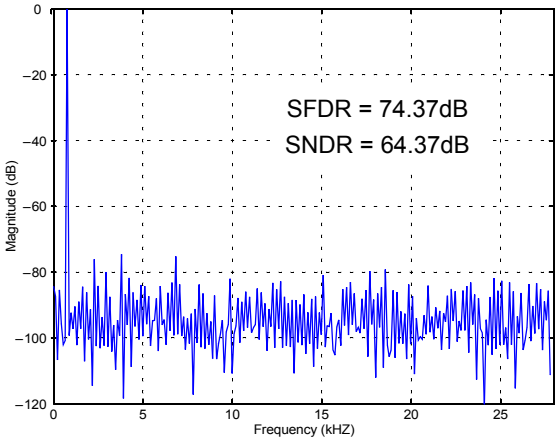

Fig. 7: FFT analysis in 12-bit operation mode (nominal PVT).

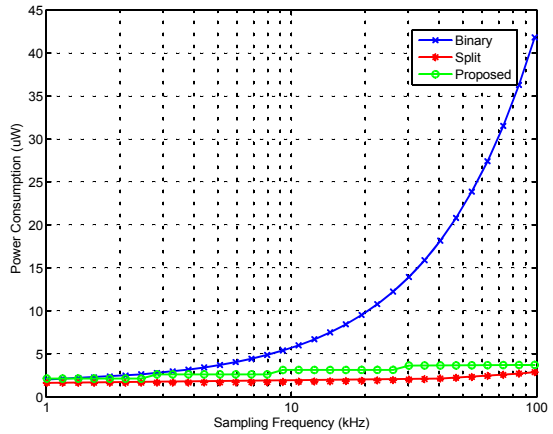

Fig. 8: Power Consumption versus Sampling Frequency of different capacitive DACs and the proposed solution.

capacitances.

Fig.8 shows the power consumption of the proposed SA-ADC in 12-bit configuration as a function of the sampling frequency. The figure also shows the power consumptions of most commonly used capacitive DAC-based solutions, binary weighted [1] and split ones [2-3] for the same resolution. The unitary capacitance for the capacitive DACs has been set to 200fF, a typical value used for this kind of converter. Most of the power dissipation in DAC-based solutions occurs during the reset phase, when the capacitive array is charged. During this phase large current spikes are drained from the supply source which puts stronger demands on the regulatory circuitry. Alternatively, the power consumption of the proposed solution is mainly due to the opamp whose power consumption remains nearly constant over the whole conversion period. Fig.9 compares the area occupation of the proposed architecture (without the programmable gain input stage) with the capacitive ones. It can be seen that the proposal is more efficient in terms of area from 9-bit of resolution onwards.

Although split solutions are more efficient in terms of power consumption, they are extremely sensitive to parasitic capacitances, as is shown in Fig.10. In this plot the ENOB is represented versus the parasitic capacitance per unit capacitance, including routing

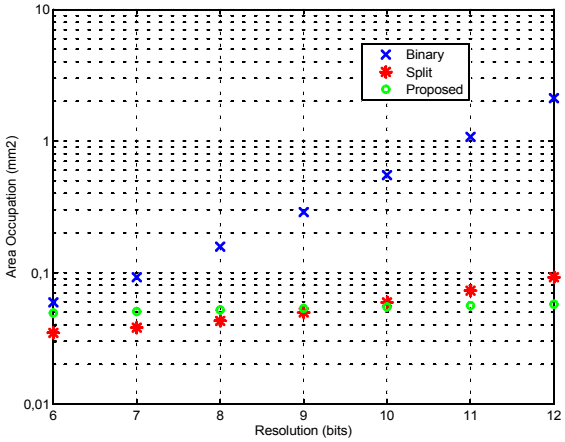

Fig. 9: Area Occupation versus resolution of different capacitive DACs and the proposed solution.

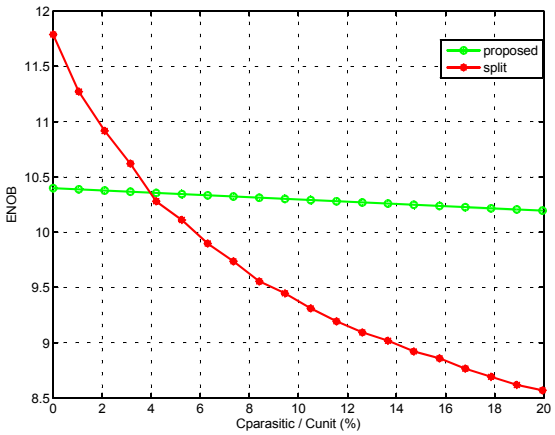

Fig. 10: ENOB versus parasitic capacitances of capacitive split DAC and proposed solution.

parasitics. These parasitics introduce non-linear errors in DAC-based topologies which degrade the resolution of the converter. However, the proposed solution remains nearly insensitive to them.

VI. CONCLUSIONS

A low-power, low-voltage SA-ADC based on SC techniques has been presented. The proposed architecture is highly reconfigurable in terms of input gain, resolution, and sampling rate. The power consumption is also adaptive in accordance to the required resolution by programming the tail current of the active blocks. This features make the ADC very suitable for wireless sensor networks applications. Additionally, the proposed converter has smoother (spike-free) current consumption, less silicon area, and lower sensitivity to parasitic capacitances than capacitive DAC-based SA-ADCs.

VII. ACKNOWLEDGMENTS

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