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This is an Accepted Manuscript of an article published by Taylor & Francis in Electric Power Components and Sytems on 13 Dec 2017.
Available online: http://www.tandfonline.com/10.1080/15325008.2017.1334161

To cite this paper: Umbría, F., Gordillo, F., & Salas, F. (2017). Modeling and full decoupling control of a grid-connected five-level diode-clamped converter. *Electric Power Components and Systems*, *45*(14), 1585-1598.

Modeling and Full Decoupling Control of a Grid-Connected Five-Level Diode-Clamped Converter

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***Abstract*—This paper presents a novel approach to deal with the regulation of the dc-link capacitor voltages and ac-side currents in a grid-connected five-level diode-clamped converter. Due to the controllability problems of this topology, guaranteeing a solid current control and, mainly, a correct dc-link voltage sharing, represents a complex technical challenge. With the purpose of coping with it, an averaged model that describes the system dynamics at both sides of the converter is presented, assuming that a modulation strategy is integrated in the system to generate the switching sequence. In order to derive the proposed model, no restriction concerning the use of only the three nearest vectors to the desired voltage reference is taking into account. Then, several changes of variables are carried out in the model equations to obtain control input decoupling for control purposes, while reducing the complexity of the model as well. Finally, the voltage and current controllers are designed separately using different control inputs in a straightforward way. Neither auxiliary hardware nor complicated mathematical calculations are required to achieve the control objectives. The effectiveness and good performance of the system under the proposed control approach is validated by simulation results, suggesting that the five-level diode-clamped converter can be a solid solution as an interfacing system connected to the utility grid for, e.g., industrial drives or renewable energy applications.**

***Index Terms*—Power conversion, multilevel converter, grid interface, diode-clamped converter (DCC), averaged system model, model-based control, full decoupling control, voltage balancing, pulse-width modulation (PWM).**

I. Introduction

Over the years, multilevel converters have emerged as one of the preferred choices of electronic power conversion for high-power and power-quality demanding applications [1]–[3]. They are commercially offered by different companies for industrial applications such as energy conversion and generation, manufacturing, transport or power transmission [4]. In addition, significant effort is being made in the field of developing new multilevel topologies and control algorithms, since this technology still presents numerous possibilities to explore and technical challenges to overcome [3].

Among the great variety of converter topologies [4]–[6], including both traditional and modern well-established multilevel topologies, the diode-clamped converter (DCC) is considered a standard solution for a wide range of applications in various sectors [3]–[5]. However, when the number of levels of the DCC is high, the industrial applications of this topology are not so extended. In this way, whereas the three-level DCC, also known as neutral-point-clamped (NPC) converter, has been well accepted by the industry, this situation does not occur for DCC configurations of four or more levels.

This fact is motivated by several factors, e.g., the complexity of the control circuitry or the requirement of large number of power semiconductor switches and clamping diodes. Nevertheless, the primary reason is due to controllability problems. More specifically, it is due to the complicated task of maintaining balanced the dc-link capacitor voltages of the converter, which cannot be properly balanced in all operating conditions when applying conventional modulation techniques [7]–[9]. In view of this, different approaches have been developed during the last years, being the balancing of the capacitor voltages still a subject of special attention and research in the field of power electronics [10]–[13]. Most of the proposed approaches require additional power hardware or auxiliary devices [14]–[19], and they lead to a significant increase in the converter cost, while adding complexity to the system. However, other control strategies have been also proposed based on (i) the implementation of modulation strategies that take into account the redundant switching states in order to optimize a cost function [20]–[25], (ii) the application of control schemes combined with modulation strategies [26]–[27], (iii) the use of predictive control techniques considering a discrete-time model of the DCC [28] or (iv) the analysis of the capacitor voltage imbalance issue as a problem of regulating the multiple outputs of a nonlinear system subject to exogenous disturbances [30]–[31]. In this manner, the inclusion of some kind of voltage balance regulation circuitry can be avoided.

As stated in [27], the balancing limitations of the dc-link capacitor voltages in DCCs are due to the use of modulation strategies such as the conventional nearest-three space vector pulse-width modulation (NT-SVPWM). This modulation strategy is carried out using only the three nearest vectors to the

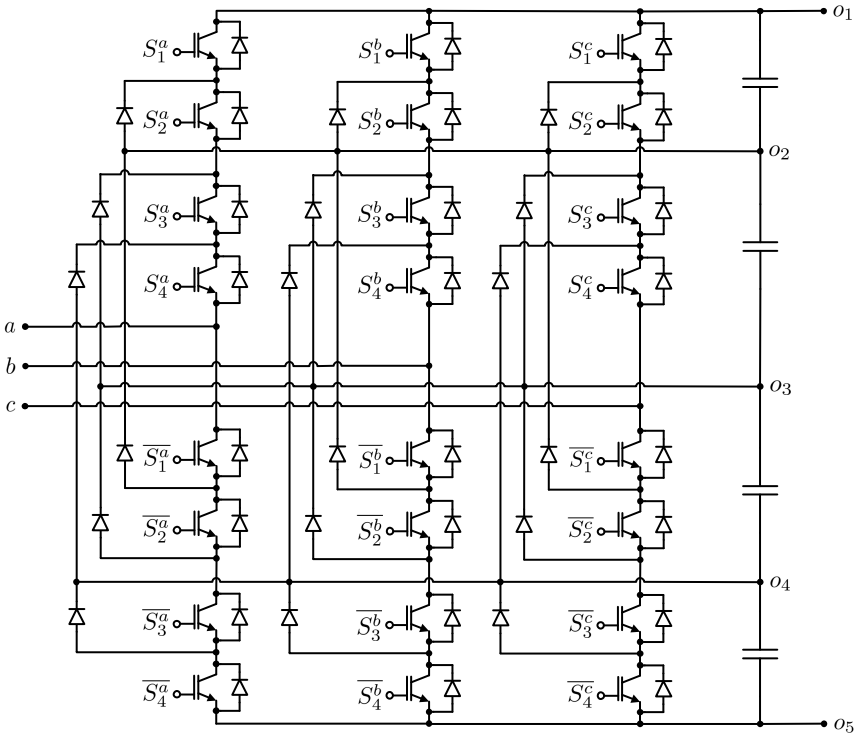

Fig. 1. Circuit of a three-phase five-level diode-clamped power converter.

desired voltage reference, so only a reduced number of voltage levels can be generated per phase in every switching cycle. Therefore, this result suggests that the control approach or modulation strategy to use should be defined without reducing the degrees of freedom of the system, that is, it should be defined considering a wider subset of voltage levels instead of only the reduced one [27].

In this way, this paper is focused on the five-level DCC topology, which is illustrated in Fig. 1, and presents a novel approach called full decoupling control to cope with the previously mentioned controllability problems of this converter. Taking into account the application of the DCC operating as an inverter connected to the utility grid, the basis of the approach is the definition of an averaged global model of the system dynamics that avoids the limitation of considering only a reduced subset of voltage levels per phase in every switching cycle that the use of NT-SVPWM imposes. This model adopts some modeling assumptions related to aspects of the system such as switching frequency or modulation strategy, which have been considered during the modeling process of different converter topologies [29]–[33], but they were not applied to the five-level DCC topology before.

Based on the derived model of the system, the novel approach to regulate not only the dc-link capacitor voltages but also the ac-side phase currents is developed. A key point of the proposed approach is the use of several changes of variables in such a way that (i) the equations of the system model are simplified and (ii) the control inputs are decoupled for control purposes. Thereby, the different control objectives can be addressed separately using a different set of control inputs for each one, designing the controllers in an extremely simple and efficient manner, with neither the need of auxiliary additional hardware nor complicated control algorithms that usually involve high computational time. Both system modeling and the proposed control approach represent, together with the controller design, the main contributions of the present work.

The outline of the paper is as follows. First, the application of the grid-connected five-level DCC considered in this paper is described in Section II, and a global dynamic model of the system is proposed. Then, Section III presents the model-based full decoupling current and capacitor voltage balance controllers. Afterwards, Section IV is devoted to the analysis of several constraints that should be satisfied when implementing the proposed controllers. Some simulation results obtained when these controllers are employed are shown and discussed in Section V. Finally, some conclusions are presented in Section VI.

II. Description and Modeling of the System

Figure 2 illustrates a schematic diagram of the five-level DCC operating as an inverter connected to the grid, which is the circuit configuration considered in this paper. The total dc-link voltage V_{dc} is assumed to be constant and is represented by a generic dc source connected to the converter. In this way, the voltage V_{dc} can be generated, for example, by industrial drives or by renewable energy sources such as hydropower, photovoltaic technology or wind energy, which have the largest

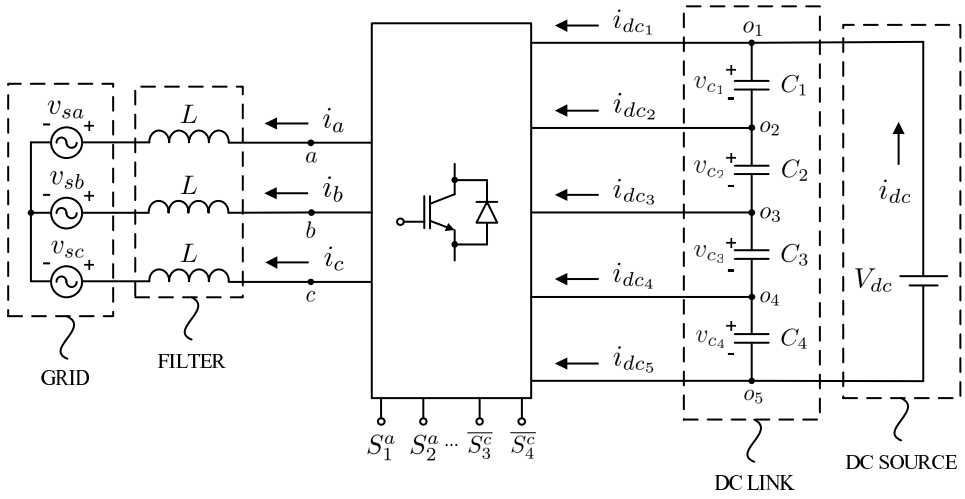

Fig. 2. Schematic diagram of the five-level diode-clamped converter operating as an inverter connected to the utility grid.

utilization nowadays. Therefore, the converter is working as a grid interfacing system [34]–[35].

The dc link of the converter is composed of capacitors C_1, C_2, C_3 and C_4, all of identical capacitance C. Their respective voltages are represented by v_{c_1}, v_{c_2}, v_{c_3} and v_{c_4}. Regarding the converter ac side, the phase voltages are denoted by v_{sa}, v_{sb} and v_{sc}, and the phase currents by i_a, i_b and i_c. The filter inductors are considered to be equal, i.e., they all present the same inductance L.

The voltages generated in points a, b and c, with respect to the dc-link midpoint o_3, are denoted by v_a, v_b and v_c, respectively. These generated voltages depend on the converter switching states, which are determined by the switching functions $f_{io_j} \in \{0, 1\}$, for $i = a$, b, c and $j = 1$, 2, 3, 4, 5, as follows

$$f_{io_1} = 1 \rightarrow \begin{cases} S_1^i \text{ on, } S_2^i \text{ on} \\ S_3^i \text{ on, } S_4^i \text{ on} \end{cases} \rightarrow v_i = v_{c_2} + v_{c_1} \quad (1)$$

$$f_{io_2} = 1 \rightarrow \begin{cases} S_1^i \text{ off, } S_2^i \text{ on} \\ S_3^i \text{ on, } S_4^i \text{ on} \end{cases} \rightarrow v_i = v_{c_2} \quad (2)$$

$$f_{io_3} = 1 \rightarrow \begin{cases} S_1^i \text{ off, } S_2^i \text{ off} \\ S_3^i \text{ on, } S_4^i \text{ on} \end{cases} \rightarrow v_i = 0 \quad (3)$$

$$f_{io_4} = 1 \rightarrow \begin{cases} S_1^i \text{ off, } S_2^i \text{ off} \\ S_3^i \text{ off, } S_4^i \text{ on} \end{cases} \rightarrow v_i = -v_{c_3} \quad (4)$$

$$f_{io_5} = 1 \rightarrow \begin{cases} S_1^i \text{ off, } S_2^i \text{ off} \\ S_3^i \text{ off, } S_4^i \text{ off} \end{cases} \rightarrow v_i = -v_{c_3} - v_{c_4}, \quad (5)$$

for $i = a$, b, c. Therefore, each switching function f_{io_j} represents whether the terminal i of the converter, for $i = a$, b, c, is connected to the dc-link point o_j, for $j = 1$, 2, 3, 4, 5, or not. In this manner, f_{io_j} is set to 1 for the first situation, while for the remaining one it is set to 0. Besides, it is worth mentioning that the following expressions

$$f_{io_1} + f_{io_2} + f_{io_3} + f_{io_4} + f_{io_5} = 1, \quad (6)$$

for $i = a$, b, c, should be satisfied for all time. In other words, each one of the converter ac-side points a, b and c should be connected to any of the points o_1, o_2, o_3, o_4 or o_5 of the dc link, and only to one of these five points, at all times.

A. General Switching Model

Considering these preliminaries as well as the well-known Kirchhoff's laws, the system switching model is described by the dynamics of the phase currents and by those of the dc-link capacitor voltages. Thus, it is expressed by

$$L\frac{di_a}{dt} = -v_{sa} + \frac{1}{3}(2v_a - v_b - v_c) \quad (7)$$

$$L\frac{di_b}{dt} = -v_{sb} + \frac{1}{3}(-v_a + 2v_b - v_c) \quad (8)$$

$$L\frac{di_c}{dt} = -v_{sc} + \frac{1}{3}(-v_a - v_b + 2v_c) \quad (9)$$

$$C\frac{dv_{c_1}}{dt} = -f_{ao_1}i_a - f_{bo_1}i_b - f_{co_1}i_c + i_{dc} \quad (10)$$

$$C\frac{dv_{c_2}}{dt} = -f_{ao_1}i_a - f_{bo_1}i_b - f_{co_1}i_c - f_{ao_2}i_a - f_{bo_2}i_b - f_{co_2}i_c + i_{dc} \quad (11)$$

$$C\frac{dv_{c_3}}{dt} = f_{ao_4}i_a + f_{bo_4}i_b + f_{co_4}i_c + f_{ao_5}i_a + f_{bo_5}i_b + f_{co_5}i_c + i_{dc} \quad (12)$$

$$C\frac{dv_{c_4}}{dt} = f_{ao_5}i_a + f_{bo_5}i_b + f_{co_5}i_c + i_{dc}, \quad (13)$$

where the model is derived assuming that the phase voltages are balanced, that is,

$$v_{sa} + v_{sb} + v_{sc} = 0. \quad (14)$$

Note also that the generated voltages v_a, v_b and v_c are defined, taking into account (1)-(5), by

$$\begin{aligned} v_i &= f_{io_1}\left(v_{c_2}+v_{c_1}\right)+f_{io_2}v_{c_2}-f_{io_4}v_{c_3} \\ &\quad -f_{io_5}\left(v_{c_3}+v_{c_4}\right), \end{aligned}$$

for $i = a,\ b,\ c$.

B. Averaged Model

Several modeling approaches such as time-varying and time-invariant averaged models, simplified switching models and small signal models, have been derived considering the DCC as well as other multilevel topologies and their different operating principles. A detailed classification can be consulted in [1]. Among them, an averaged state-space model in rotating dq coordinates was presented by Bordonau et al. in [33], for a three-level neutral-point-clamped inverter connected to a symmetric and balanced load, composed of a LC low-pass filter and a resistive load.

The essential idea of this model is that, when the frequency range of the system is much lower than the switching frequency, the moving average operator can be applied. As a result, the control inputs of the model are expressed in terms of the duty ratios obtained from applying moving average and dq transformation to the converter switching functions. Besides, during the modeling process it is assumed that a modulation strategy, e.g., pulse-width modulation (PWM), is integrated in the system for the purpose of generating the switching sequence.

In the present paper, the modeling approach proposed in [33] is adopted for the grid-connected five-level DCC. In this way, considering the general equations of the system switching model (7)-(13), the switching functions f_{ij} are replaced by their respective averaged values in a switching period, yielding the duty ratios d_{ij}, for $i = a,\ b,\ c$ and $j = 1,\ 2,\ 3,\ 4,\ 5$, i.e., the control inputs of the model. Thus, the averaged model is expressed by (15)-(20), where the new state variables

$$\begin{aligned} L\frac{di_a}{dt} &= -v_{sa}+\left(4d_{ao_1}+2d_{ao_2}-2d_{ao_4}-4d_{ao_5}-2d_{bo_1}-d_{bo_2}+d_{bo_4}+2d_{bo_5}-2d_{co_1}-d_{co_2}+d_{co_4}+2d_{co_5}\right)\frac{V_{dc}}{12} \\ &\quad +\left(4d_{ao_1}-2d_{ao_2}+2d_{ao_4}+4d_{ao_5}-2d_{bo_1}+d_{bo_2}-d_{bo_4}-2d_{bo_5}-2d_{co_1}+d_{co_2}-d_{co_4}-2d_{co_5}\right)\frac{v_{d_1}}{12} \\ &\quad +\left(4d_{ao_1}+6d_{ao_2}+2d_{ao_4}+4d_{ao_5}-2d_{bo_1}-3d_{bo_2}-d_{bo_4}-2d_{bo_5}-2d_{co_1}-3d_{co_2}-d_{co_4}-2d_{co_5}\right)\frac{v_{d_2}}{12} \\ &\quad +\left(2d_{ao_2}-2d_{ao_4}-d_{bo_2}+d_{bo_4}-d_{co_2}+d_{co_4}\right)\frac{v_{d_3}}{6} \end{aligned} \tag{15}$$

$$\begin{aligned} L\frac{di_b}{dt} &= -v_{sb}+\left(-2d_{ao_1}-d_{ao_2}+d_{ao_4}+2d_{ao_5}+4d_{bo_1}+2d_{bo_2}-2d_{bo_4}-4d_{bo_5}-2d_{co_1}-d_{co_2}+d_{co_4}+2d_{co_5}\right)\frac{V_{dc}}{12} \\ &\quad +\left(-2d_{ao_1}+d_{ao_2}-d_{ao_4}-2d_{ao_5}+4d_{bo_1}-2d_{bo_2}+2d_{bo_4}+4d_{bo_5}-2d_{co_1}+d_{co_2}-d_{co_4}-2d_{co_5}\right)\frac{v_{d_1}}{12} \\ &\quad +\left(-2d_{ao_1}-3d_{ao_2}-d_{ao_4}-2d_{ao_5}+4d_{bo_1}+6d_{bo_2}+2d_{bo_4}+4d_{bo_5}-2d_{co_1}-3d_{co_2}-d_{co_4}-2d_{co_5}\right)\frac{v_{d_2}}{12} \\ &\quad +\left(-d_{ao_2}+d_{ao_4}+2d_{bo_2}-2d_{bo_4}-d_{co_2}+d_{co_4}\right)\frac{v_{d_3}}{6} \end{aligned} \tag{16}$$

$$\begin{aligned} L\frac{di_c}{dt} &= -v_{sb}+\left(-2d_{ao_1}-d_{ao_2}+d_{ao_4}+2d_{ao_5}-2d_{bo_1}-d_{bo_2}+d_{bo_4}+2d_{bo_5}+4d_{co_1}+2d_{co_2}-2d_{co_4}-4d_{co_5}\right)\frac{V_{dc}}{12} \\ &\quad +\left(-2d_{ao_1}+d_{ao_2}-d_{ao_4}-2d_{ao_5}-2d_{bo_1}+d_{bo_2}-d_{bo_4}-2d_{bo_5}+4d_{co_1}-2d_{co_2}+2d_{co_4}+4d_{co_5}\right)\frac{v_{d_1}}{12} \\ &\quad +\left(-2d_{ao_1}-3d_{ao_2}-d_{ao_4}-2d_{ao_5}-2d_{bo_1}-3d_{bo_2}-d_{bo_4}-2d_{bo_5}+4d_{co_1}+6d_{co_2}+2d_{co_4}+4d_{co_5}\right)\frac{v_{d_2}}{12} \\ &\quad +\left(-d_{ao_2}+d_{ao_4}-d_{bo_2}+d_{bo_4}+2d_{co_2}-2d_{co_4}\right)\frac{v_{d_3}}{6} \end{aligned} \tag{17}$$

$$C\frac{dv_{d_1}}{dt} = -\left(d_{ao_1}+d_{ao_5}\right)i_a-\left(d_{bo_1}+d_{bo_5}\right)i_b-\left(d_{co_1}+d_{co_5}\right)i_c \tag{18}$$

$$C\frac{dv_{d_2}}{dt} = -\left(d_{ao_1}+d_{ao_2}+d_{ao_4}+d_{ao_5}\right)i_a-\left(d_{bo_1}+d_{bo_2}+d_{bo_4}+d_{bo_5}\right)i_b-\left(d_{co_1}+d_{co_2}+d_{co_4}+d_{co_5}\right)i_c \tag{19}$$

$$C\frac{dv_{d_3}}{dt} = d_{ao_4}i_a+d_{bo_4}i_b+d_{co_4}i_c \tag{20}$$

v_{d_1}, v_{d_2} and v_{d_3} are considered. These variables represent the differences between the voltages of the dc-link capacitors, and they are described by

$$\begin{aligned} v_{d_1} &= v_{c_1} - v_{c_4} \\ v_{d_2} &= v_{c_2} - v_{c_3} \\ v_{d_3} &= v_{c_3} - v_{c_4}. \end{aligned}$$

Note that, since the DCC is working as an inverter in this paper, the total dc-link voltage is set to a constant value, denoted by V_{dc}. Therefore, the system dynamics can be described considering v_{d_1}, v_{d_2} and v_{d_3} instead of variables v_{c_1}, v_{c_2}, v_{c_3} and v_{c_4}, without loss of generality.

In addition, it is important to point out that, in the model (15)-(20), the duty ratios d_{ao_3}, d_{bo_3} and d_{co_3} do not appear because they are associated with $v_i = 0$ and the switching functions (3), for $i = a, b, c$. In this way, they are related to values of the generated voltages equal to zero. Nevertheless, from (6) it follows that

$$d_{io_1} + d_{io_2} + d_{io_3} + d_{io_4} + d_{io_5} = 1, \tag{21}$$

for $i = a, b, c$. This constraint should be taken into account when considering the averaged model (15)-(20). Furthermore, the duty ratios should be defined such that

$$d_{io_j} \in [0, 1], \tag{22}$$

for $i = a, b, c$ and $j = 1, 2, 3, 4, 5$, leading to a further constraint to consider as well.

C. Averaged Model in $\alpha\beta\gamma$ Coordinates

In three-phase power systems, the variables of the system often are transformed from abc into stationary $\alpha\beta\gamma$ orthogonal coordinates to take advantage of some properties that this transformation provides, for example, control input decoupling for control purposes. To that end, the power-invariant form of the Clarke Transform described in Appendix can be used. Thus, applying this change of variables with the variables of the averaged model (15)-(20), it yields the expressions (23)-(27), which represent the system averaged model in $\alpha\beta\gamma$ coordinates. Thereby, in this new model, the phase currents are described by i_α and i_β, while the phase voltages are described by v_α and v_β. The duty ratios $d_{\alpha o_1}$, $d_{\beta o_1}$, $d_{\alpha o_2}$, $d_{\beta o_2}$, $d_{\alpha o_4}$, $d_{\beta o_4}$, $d_{\alpha o_5}$ and $d_{\beta o_5}$ are the control inputs, whereas the remaining duty ratios $d_{\gamma o_1}$, $d_{\gamma o_2}$, $d_{\gamma o_4}$ and $d_{\gamma o_5}$ do not appear in the model.

Besides, since the phase voltages are assumed to be balanced (14) and the phase currents are balanced in the same way, notice that the change of coordinates leads to

$$\begin{aligned} i_\gamma &= 0 \\ v_\gamma &= 0. \end{aligned}$$

As it was said before, a similar modeling approach was used in [33] for three-level DCCs. A key idea of the present paper is the manipulation of the derived model (23)-(27) in order to obtain an exact simplified expression of it. This idea has been previously applied for three-level DCCs in [36].

III. Controller Design: Full Decoupling Control

In order to regulate the system phase currents and to avoid the dc-link capacitor voltage unbalance, several controllers should be designed. For this purpose, more concretely, a current controller as well as a voltage balance controller, both based on the system model described in Section II-C, are presented in the following. In addition, the change of variables

$$\begin{cases} u_1 &= 2d_{\alpha o_1} + d_{\alpha o_2} - d_{\alpha o_4} - 2d_{\alpha o_5} \\ u_2 &= 2d_{\beta o_1} + d_{\beta o_2} - d_{\beta o_4} - 2d_{\beta o_5} \\ u_3 &= d_{\alpha o_1} + d_{\alpha o_5} \\ u_4 &= d_{\beta o_1} + d_{\beta o_5} \\ u_5 &= d_{\alpha o_1} + d_{\alpha o_2} + d_{\alpha o_4} + d_{\alpha o_5} \\ u_6 &= d_{\beta o_1} + d_{\beta o_2} + d_{\beta o_4} + d_{\beta o_5} \\ u_7 &= -d_{\alpha o_4} \\ u_8 &= -d_{\beta o_4}, \end{cases} \tag{28}$$

is considered. The definition of these new control variables, which is inspired by (23)-(27) and used during the controller design, constitutes a fundamental aspect of the proposed modeling and control approach. Notice that, when the change of variables (28) is applied into (23)-(27), the resultant model is not as involved as the equations (15)-(20) anticipated. Besides, the considered change of variables is invertible.

A. Current Controller

Concerning the regulation of the currents i_α and i_β, these two state variables should track their respective references i_α^r and i_β^r, minimizing the current errors

$$\begin{aligned} i_\alpha^e &= i_\alpha^r - i_\alpha \\ i_\beta^e &= i_\beta^r - i_\beta. \end{aligned}$$

It is worth stressing that, according to [37], these control objectives can also be defined in relation to the instantaneous powers of the three-phase circuit

$$p = v_\alpha i_\alpha + v_\beta i_\beta \tag{29}$$

$$q = v_\alpha i_\beta - v_\beta i_\alpha, \tag{30}$$

where variables p and q represent the instantaneous active and reactive powers, respectively. In this case, the controller should be designed in such a way that the instantaneous powers are regulated in order to transfer a desired amount of active power with a determined power factor, usually operating at unity power factor to inject the maximum amount of active power to the ac side.

With the goal of simplifying the current dynamics (23)-(24) to facilitate the controller design, the capacitor voltage imbalances are assumed to be small, that is, $v_{c_1} \simeq v_{c_2} \simeq v_{c_3} \simeq v_{c_4}$. Under this assumption, the current dynamics are approximated considering u_1 as well as u_2, both defined in

(28), by

$$L\,\frac{di_\alpha}{dt} \simeq -v_\alpha + \frac{1}{4}\,u_1 V_{dc} \tag{31}$$

$$L\,\frac{di_\beta}{dt} \simeq -v_\beta + \frac{1}{4}\,u_2 V_{dc}. \tag{32}$$

These derived current dynamics are similar to those of the two-level converter and can be easily transformed into dq coordinates or expressed in terms of the instantaneous powers (29) and (30). Hence, the current controller can be implemented adopting any of the numerous control strategies widely studied over the last years [38]–[42]. In this paper, the solution considered is described as follows

$$u_1 = \frac{4}{V_{dc}}\left(k_p\,(i_\alpha^r - i_\alpha) + k_i\int_0^t (i_\alpha^r - i_\alpha)\,d\tau + v_\alpha\right) \tag{33}$$

$$u_2 = \frac{4}{V_{dc}}\left(k_p\,(i_\beta^r - i_\beta) + k_i\int_0^t (i_\beta^r - i_\beta)\,d\tau + v_\beta\right). \tag{34}$$

In this way, the controller includes a PI-type control action, where customary tuning parameters k_p and k_i are the proportional and integral gains, respectively. Besides, it also includes some terms to cancel the voltage variables v_α and v_β that appear in (31) and (32). A schematic block diagram of the current controller is shown in Fig. 3.

Finally, considering the definitions of the instantaneous powers given by (29) and (30), the current tracking references i_α^r and i_β^r are defined by

$$i_\alpha^r = \frac{1}{v_\alpha^2 + v_\beta^2}\,(v_\alpha p^r - v_\beta q^r) \tag{35}$$

$$i_\beta^r = \frac{1}{v_\alpha^2 + v_\beta^2}\,(v_\beta p^r + v_\alpha q^r)\,. \tag{36}$$

It is important to note that constant parameters p^r and q^r are the desired values of the instantaneous active and reactive powers, respectively. They both determine the specific operating point of the system.

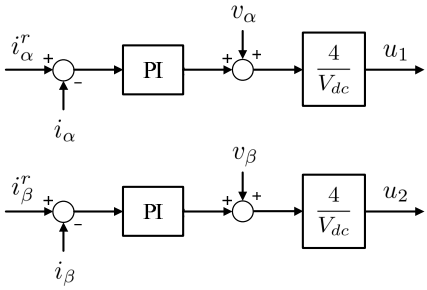

Fig. 3. Schematic block diagram of the current controller.

B. Capacitor Voltage Balance Controller

With regard to the regulation of the dc-link capacitor voltages, a novel model-based controller is proposed in this section. It is based on the particular equations of the dynamics of the voltage differences between the capacitors, which are expressed by

$$C\,\frac{dv_{d_1}}{dt} = -u_3 i_\alpha - u_4 i_\beta$$

$$C\,\frac{dv_{d_2}}{dt} = -u_5 i_\alpha - u_6 i_\beta$$

$$C\,\frac{dv_{d_3}}{dt} = -u_7 i_\alpha - u_8 i_\beta,$$

where control variables (28) are introduced in (25)-(27).

The key point of the proposed approach is that, when defining (28), it leads to a complete decoupling of the control variables. Thereby, whereas u_1 and u_2 are used, separately, to regulate the currents variables i_α and i_β, as described before, control variables u_3, u_4, u_5, u_6, u_7 and u_8 remain as degrees of freedom for keeping the capacitor voltage differences close to zero. Therefore, these control variables can be devoted to

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$$L\,\frac{di_\alpha}{dt} = -v_\alpha + (2d_{\alpha o_1} + d_{\alpha o_2} - d_{\alpha o_4} - 2d_{\alpha o_5})\,\frac{V_{dc}}{4} + (2d_{\alpha o_1} - d_{\alpha o_2} + d_{\alpha o_4} + 2d_{\alpha o_5})\,\frac{v_{d_1}}{4} + (2d_{\alpha o_1} + 3d_{\alpha o_2} + d_{\alpha o_4} + 2d_{\alpha o_5})\,\frac{v_{d_2}}{4} + (d_{\alpha o_2} - d_{\alpha o_4})\,\frac{v_{d_3}}{2} \tag{23}$$

$$L\,\frac{di_\beta}{dt} = -v_\beta + (2d_{\beta o_1} + d_{\beta o_2} - d_{\beta o_4} - 2d_{\beta o_5})\,\frac{V_{dc}}{4} + (2d_{\beta o_1} - d_{\beta o_2} + d_{\beta o_4} + 2d_{\beta o_5})\,\frac{v_{d_1}}{4} + (2d_{\beta o_1} + 3d_{\beta o_2} + d_{\beta o_4} + 2d_{\beta o_5})\,\frac{v_{d_2}}{4} + (d_{\beta o_2} - d_{\beta o_4})\,\frac{v_{d_3}}{2} \tag{24}$$

$$C\,\frac{dv_{d_1}}{dt} = -(d_{\alpha o_1} + d_{\alpha o_5})\,i_\alpha - (d_{\beta o_1} + d_{\beta o_5})\,i_\beta \tag{25}$$

$$C\,\frac{dv_{d_2}}{dt} = -(d_{\alpha o_1} + d_{\alpha o_2} + d_{\alpha o_4} + d_{\alpha o_5})\,i_\alpha - (d_{\beta o_1} + d_{\beta o_2} + d_{\beta o_4} + d_{\beta o_5})\,i_\beta \tag{26}$$

$$C\,\frac{dv_{d_3}}{dt} = d_{\alpha o_4} i_\alpha + d_{\beta o_4} i_\beta \tag{27}$$

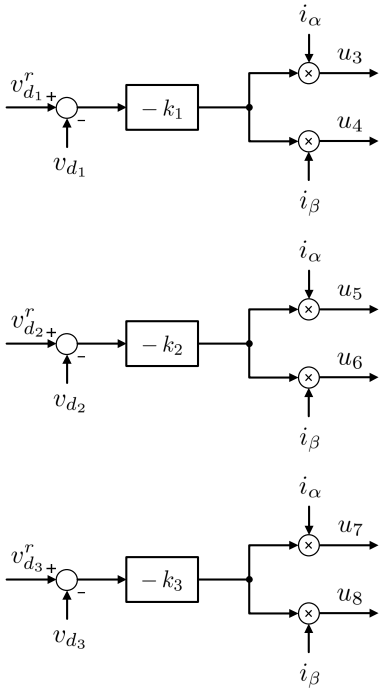

Fig. 4. Schematic block diagram of the voltage balance controller.

regulate the state variables v_{d_1}, v_{d_2} and v_{d_3}. In this way, they are defined in this paper by the expressions

$$u_3 = -k_1 i_\alpha \left(v^r_{d_1} - v_{d_1}\right) \quad (37)$$

$$u_4 = -k_1 i_\beta \left(v^r_{d_1} - v_{d_1}\right) \quad (38)$$

$$u_5 = -k_2 i_\alpha \left(v^r_{d_2} - v_{d_2}\right) \quad (39)$$

$$u_6 = -k_2 i_\beta \left(v^r_{d_2} - v_{d_2}\right) \quad (40)$$

$$u_7 = -k_3 i_\alpha \left(v^r_{d_3} - v_{d_3}\right) \quad (41)$$

$$u_8 = -k_3 i_\beta \left(v^r_{d_3} - v_{d_3}\right), \quad (42)$$

where k_1, k_2 and k_3 are design positive constants to select and $v^r_{d_1}$, $v^r_{d_2}$ and $v^r_{d_3}$ are the capacitor voltage difference references, which are set to zero. Figure 4 illustrates the schematic block diagram of this proposed controller.

Introducing these control laws in the system, the dynamics of the closed loop are described by

$$C\frac{dv_{d_1}}{dt} = k_1 i_\alpha^2 \left(v^r_{d_1} - v_{d_1}\right) + k_1 i_\beta^2 \left(v^r_{d_1} - v_{d_1}\right) \quad (43)$$

$$C\frac{dv_{d_2}}{dt} = k_2 i_\alpha^2 \left(v^r_{d_2} - v_{d_2}\right) + k_2 i_\beta^2 \left(v^r_{d_2} - v_{d_2}\right) \quad (44)$$

$$C\frac{dv_{d_3}}{dt} = k_3 i_\alpha^2 \left(v^r_{d_3} - v_{d_3}\right) + k_3 i_\beta^2 \left(v^r_{d_3} - v_{d_3}\right). \quad (45)$$

These expressions depend on time-varying current terms. Nevertheless, when the regulation of i_α and i_β is carried out satisfactory, these variables can be approximated by

$$i_\alpha \simeq i^r_\alpha = I_{\alpha\beta}\cos\left(2\pi f t + \theta\right) \quad (46)$$

$$i_\beta \simeq i^r_\beta = I_{\alpha\beta}\sin\left(2\pi f t + \theta\right), \quad (47)$$

where f and $I_{\alpha\beta}$ are, respectively, the frequency and amplitude of these variables and parameter θ is the phase. Hence, exploiting the knowledge and properties of (46) and (47), it yields the following expressions

$$C\frac{dv_{d_1}}{dt} \simeq k_1 I^2_{\alpha\beta}\left(v^r_{d_1} - v_{d_1}\right)$$

$$C\frac{dv_{d_2}}{dt} \simeq k_2 I^2_{\alpha\beta}\left(v^r_{d_2} - v_{d_2}\right)$$

$$C\frac{dv_{d_3}}{dt} \simeq k_3 I^2_{\alpha\beta}\left(v^r_{d_3} - v_{d_3}\right),$$

which are derived from (43)-(45) and do not depend of current variables. Note that the zero equilibrium point of the voltage difference dynamics is exponentially stable.

C. Change of Coordinates

Once the control variables u_1, u_2, u_3, u_4, u_5, u_6, u_7 and u_8 are calculated, they should be expressed first in terms of the original variables by using the expressions

$$\begin{cases} d_{\alpha o_1} = \frac{1}{4}\left(u_1 + 3u_3 - u_5 - 2u_7\right) \\ d_{\beta o_1} = \frac{1}{4}\left(u_2 + 3u_4 - u_6 - 2u_8\right) \\ d_{\alpha o_2} = -u_3 + u_5 + u_7 \\ d_{\beta o_2} = -u_4 + u_6 + u_8 \\ d_{\alpha o_4} = -u_7 \\ d_{\beta o_4} = -u_8 \\ d_{\alpha o_5} = \frac{1}{4}\left(-u_1 + u_3 + u_5 + 2u_7\right) \\ d_{\beta o_5} = \frac{1}{4}\left(-u_2 + u_4 + u_6 + 2u_8\right). \end{cases} \quad (48)$$

Then, these eight duty ratios are transformed into original abc coordinates leading to

$$d_{ao_i} = \sqrt{\frac{2}{3}}\left(d_{\alpha o_i} + \frac{1}{\sqrt{2}}\, d_{\gamma o_i}\right) \quad (49)$$

$$d_{bo_i} = \sqrt{\frac{2}{3}}\left(-\frac{1}{2}\, d_{\alpha o_i} + \frac{\sqrt{3}}{2}\, d_{\beta o_i} + \frac{1}{\sqrt{2}}\, d_{\gamma o_i}\right) \quad (50)$$

$$d_{co_i} = \sqrt{\frac{2}{3}}\left(-\frac{1}{2}\, d_{\alpha o_i} - \frac{\sqrt{3}}{2}\, d_{\beta o_i} + \frac{1}{\sqrt{2}}\, d_{\gamma o_i}\right), \quad (51)$$

for $i = 1, 2, 4, 5$. Notice that, at this point, the values of variables $d_{\gamma o_1}$, $d_{\gamma o_2}$, $d_{\gamma o_4}$ and $d_{\gamma o_5}$ should be chosen to carry

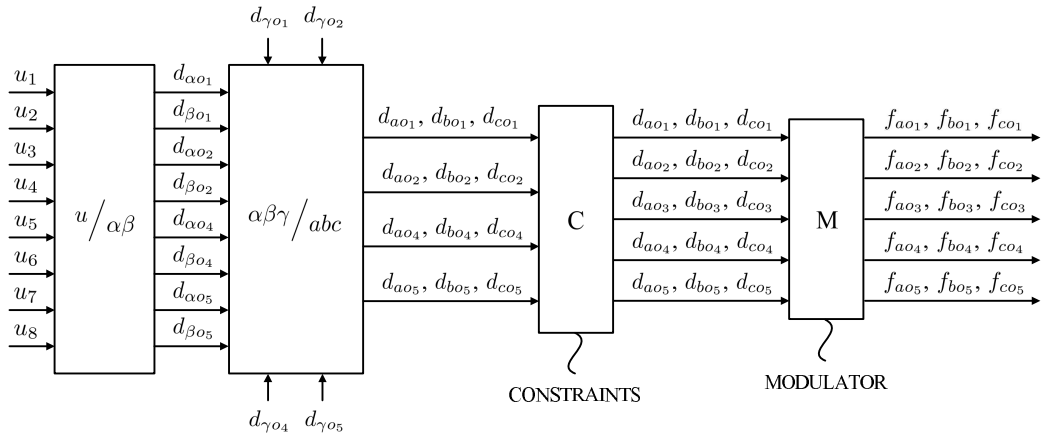

Fig. 5. Schematic block diagram of the steps to carry out for generating the switching functions f_{io_j}, for $i = a$, b, c and $j = 1, 2, 3, 4, 5$.

out the change of variables. The specific criterion adopted to select them is discussed in the following section of this paper.

Finally, taking into account (21), the remaining three duty ratios d_{ao_3}, d_{bo_3} and d_{co_3} are calculated, and the modulation is applied to provide the switching functions $f_{io_j} \in \{0, 1\}$, for $i = a$, b, c and $j = 1, 2, 3, 4, 5$, i.e., to generate the switching sequence. A schematic block diagram of the steps to carry out, including the different transformations mentioned, is illustrated in Fig. 5.

IV. Analysis of Constraints in Steady State

As pointed out previously in Section II, the averaged model of the system contains some constraints given by (21) and (22). Although in the design stage of the controllers these constraints have not been considered, they can not be neglected and should be included during the conversion of coordinates described in Section III-C. In fact, (21) is used to obtain the duty ratios d_{ao_3}, d_{bo_3} and d_{co_3} required to implement the modulation.

Concerning (22), variables $d_{\gamma o_1}$, $d_{\gamma o_2}$, $d_{\gamma o_4}$ and $d_{\gamma o_5}$ play a fundamental role, since they can be used to modify the duty ratio values in abc coordinates, as can be seen in (49)-(51). In particular, it is interesting to analyze this issue considering the system steady-state condition, meaning that the system variables are located around their respective steady-state references. To that end, it is assumed that state variables i_α, i_β, v_{d_1}, v_{d_2} and v_{d_3} can be approximated by i_α^r, i_β^r, $v_{d_1}^r$, $v_{d_2}^r$ and $v_{d_3}^r$, respectively. Besides, under this situation, the control variables u_1, u_2, u_3, u_4, u_5, u_6, u_7 and u_8 are defined by

$$u_1^{ss} \simeq \frac{4}{V_{dc}} v_\alpha$$

$$u_2^{ss} \simeq \frac{4}{V_{dc}} v_\beta$$

$$u_i^{ss} \simeq 0,$$

for $i = 3, 4, 5, 6, 7, 8$, where the superscript ss indicates the condition of steady state of the system. Consequently, the duty ratios in $\alpha\beta$ coordinates (48) are derived as follows

$$d_{\alpha o_1}^{ss} \simeq \frac{1}{V_{dc}} v_\alpha \tag{52}$$

$$d_{\beta o_1}^{ss} \simeq \frac{1}{V_{dc}} v_\beta \tag{53}$$

$$d_{\alpha o_5}^{ss} \simeq -\frac{1}{V_{dc}} v_\alpha \tag{54}$$

$$d_{\beta o_5}^{ss} \simeq -\frac{1}{V_{dc}} v_\beta \tag{55}$$

$$d_{io_j}^{ss} \simeq 0, \tag{56}$$

for $i = \alpha$, β and $j = 2, 4$. It is important to note that the phase voltages in $\alpha\beta$ coordinates can be expressed by

$$v_\alpha = V_{\alpha\beta} \cos(2\pi f t + \phi) \tag{57}$$

$$v_\beta = V_{\alpha\beta} \sin(2\pi f t + \phi), \tag{58}$$

where f is the grid frequency. Parameters $V_{\alpha\beta}$ and ϕ are, respectively, the amplitude and phase of these variables.

Introducing (52)-(56) in equations (49)-(51), the constraints (21) and (22) can be expressed in terms of $d_{\gamma o_1}$, $d_{\gamma o_2}$, $d_{\gamma o_4}$ and $d_{\gamma o_5}$. In this manner, it yields

$$\sqrt{2}\frac{V_{\alpha\beta}}{V_{dc}} \leq d_{\gamma o_i} \leq \sqrt{3} - \sqrt{2}\frac{V_{\alpha\beta}}{V_{dc}}, \tag{59}$$

for $i = 1, 5$, as well as the restrictions

$$d_{\gamma o_1} + d_{\gamma o_2} + d_{\gamma o_4} + d_{\gamma o_5} \leq \sqrt{3}$$

$$d_{\gamma o_j} \geq 0,$$

for $j = 2, 4$. Notice that these constraints are extremely conservative because they are calculated by substituting the phase voltage values by the upper and lower limits of both (57) and (58) accordingly. In view of this result, the criterion adopted in this paper is to keep constant during all time the values of the variables $d_{\gamma o_1}$, $d_{\gamma o_2}$, $d_{\gamma o_4}$ and $d_{\gamma o_5}$. Thus, they are set to the constant values $k_{\gamma o_1}$, $k_{\gamma o_2}$, $k_{\gamma o_4}$ and

TABLE I
SIMULATION PARAMETERS

Parameter	Value
Sampling frequency (f_s)	5 kHz
Switching frequency (f_{sw})	5 kHz
Grid frequency (f)	50 Hz
Phase voltages (v_{sa}, v_{sb}, v_{sc})	230 V_{RMS}
Inductors (L)	3.5 mH
Capacitors (C_1, C_2, C_3, C_4)	3300 μF
Total dc-link voltage (V_{dc})	800 V
Instantaneous active power reference (p^r)	10 kW
Instantaneous reactive power reference (q^r)	0 VAr
Current controller proportional gain (k_p)	0.5
Current controller integral gain (k_i)	3
Voltage balance controller constants (k_1, k_2, k_3)	0.5
Transformation constants ($k_{\gamma o_1}$, $k_{\gamma o_5}$)	0.7
Transformation constants ($k_{\gamma o_2}$, $k_{\gamma o_4}$)	0.1

$k_{\gamma o_5}$, respectively, which are defined taking into account the previous constraints. This fact represents an important benefit, because the values of $d_{\gamma o_1}$, $d_{\gamma o_2}$, $d_{\gamma o_4}$ and $d_{\gamma o_5}$ do not need to be computed each sampling period of time. Furthermore, a theoretical limit of operation

$$\frac{V_{\alpha\beta}}{V_{dc}} \leq \frac{1}{2}\sqrt{\frac{3}{2}},$$

for applying the proposed control approach is derived from (59). This conservative limit is commonly satisfied in practical applications.

To conclude with this section, the saturation scenario of the control inputs is discussed here briefly. Considering (22), in case that any of the derived duty ratios (49)-(51) is not located within the domain defined by $[\,0,\,1\,]$ at any particular moment, this specific duty ratio should be saturated. The saturations can also be considered at the controller design stage, that is, when the control variables u_1, u_2, u_3, u_4, u_5, u_6, u_7 and u_8 are defined, or even when they are transformed into $\alpha\beta$ coordinates. Some possible saturation strategies are discussed in [43], and they can be applied to the present saturation situation including some minor modifications. Nevertheless, as long as (22) is satisfied, no saturation strategy is needed.

V. PERFORMANCE EVALUATION

The aim of this section is to demonstrate the usefulness of the model-based full decoupling control approach proposed in this paper. To that end, the inverter configuration of the grid interfacing five-level DCC shown in Fig. 2, together with the current and capacitor voltage balance controllers described in Section III, have been implemented and executed under PSCAD environment. From the control signals calculated each sampling period of time, that is, from the duty ratios d_{io_j}, for $i = a,\ b,\ c$ and $j = 1,\ 2,\ 3,\ 4,\ 5$, the switching sequence has been generated by means of a PWM strategy. The values of the considered system parameters, including those of the proposed system controllers, are summarized in Table I.

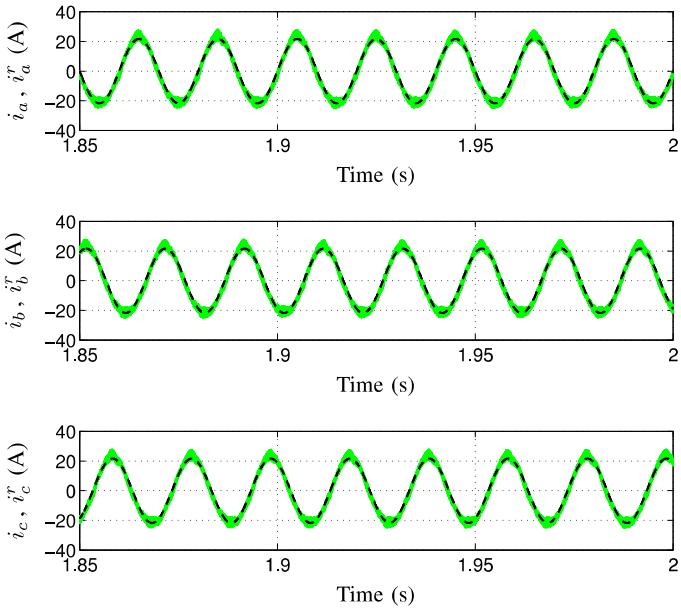

Fig. 6. Evolution of the phase currents i_a, i_b and i_c (solid) and their respective tracking references (dashed).

It is worth stressing that the duty ratios in abc coordinates have been derived applying the change of coordinates described in Section III-C. Thus, the control variables u_i defined by (33), (34) and (37)-(42) were computed at the beginning of each sampling period first, having applied then the transformation procedure illustrated in Fig. 5. For this purpose, the required variables $d_{\gamma o_1}$, $d_{\gamma o_2}$, $d_{\gamma o_4}$ and $d_{\gamma o_5}$ were set to the constant values $k_{\gamma o_1}$, $k_{\gamma o_2}$, $k_{\gamma o_4}$ and $k_{\gamma o_5}$, respectively, during the simulation carried out. These constants can be consulted in Table I and satisfy the steady-state constraints discussed in the previous section.

Figure 6 depicts the behavior in steady-state operation of the phase currents in abc coordinates and their tracking references. It can be noticed that the fundamental components of the currents and of their respective references are in phase. Besides, the current distortion is not high. Consequently, solid current regulation is ensured. It is important to point out that the current tracking references are defined considering (35) and (36), i.e., taking into account the instantaneous power references described in Table I. In this way, the time evolution of the instantaneous powers is illustrated in Fig. 7, and both instantaneous active and reactive terms p and q are maintained around their respective references. The behavior of the voltages v_a, v_b and v_c generated by the converter is also illustrated in Fig. 8.

Regarding the voltage difference variables v_{d_1}, v_{d_2} and v_{d_3}, their evolution in time is shown in Fig. 9. These three variables are kept close to zero at all times, avoiding the uncontrolled rise or fall of the dc-link capacitor voltages and guaranteeing in this way the correct balancing of these voltages. Since it is more intuitive to see directly the evolution of the dc-link capacitor voltages, their behavior is also illustrated in Fig. 10. Notice that the four voltages are maintained around their

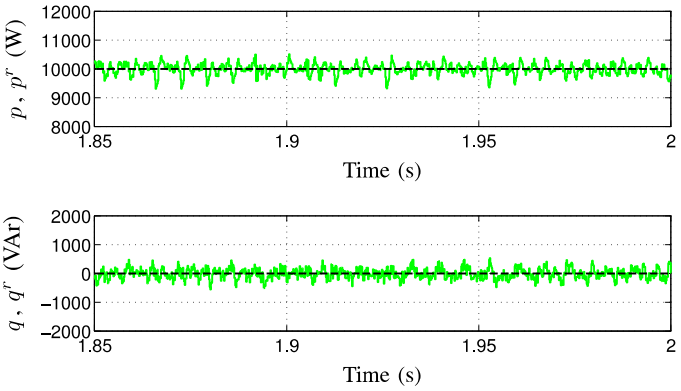

Fig. 7. Behavior of the instantaneous active and reactive powers p and q (solid) and respective reference values p^r and q^r (dashed) of these two variables.

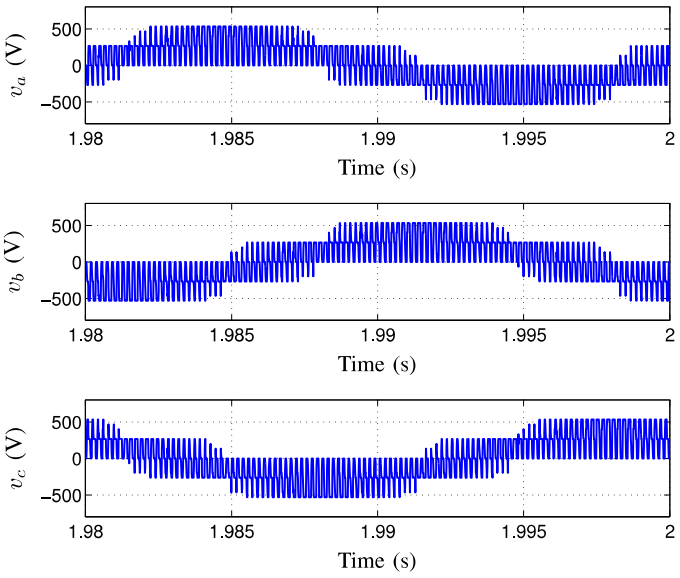

Fig. 8. Behavior of the generated voltages v_a, v_b and v_c.

reference, which is defined by the quarter of the total dc-link voltage value, that is, by 200 V.

Finally, the behavior of the system has been tested in order to illustrate clearer the requirements for a dc-link capacitor voltage balance controller in the five-level DCC topology. Thereby, the controller proposed in Section III-B and defined by (37)-(42) has been disconnected during a short period of time, from $t = 2.1$ s to $t = 2.3$ s. As can be seen in Fig. 11, the capacitor voltages start to fall or rise in an uncontrolled way at $t = 2.1$ s. However, when the controller is connected to the system again at $t = 2.3$ s, these voltages are rapidly controlled, beginning to move towards their reference value. Therefore, the controller presents a satisfactory performance with regard to the regulation of the dc-link capacitor voltages.

VI. Conclusions

This paper has presented a novel modeling and control approach to address the controllability problems of a five-level

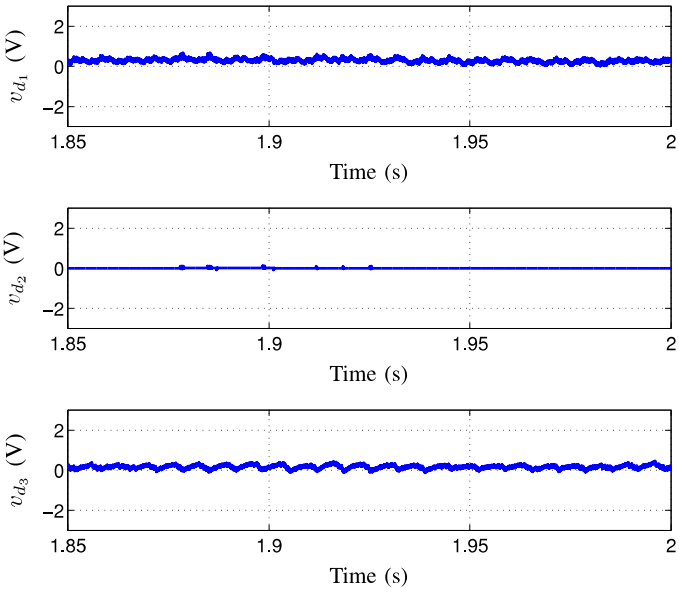

Fig. 9. Behavior of the voltage variables v_{d_1}, v_{d_2} and v_{d_3}.

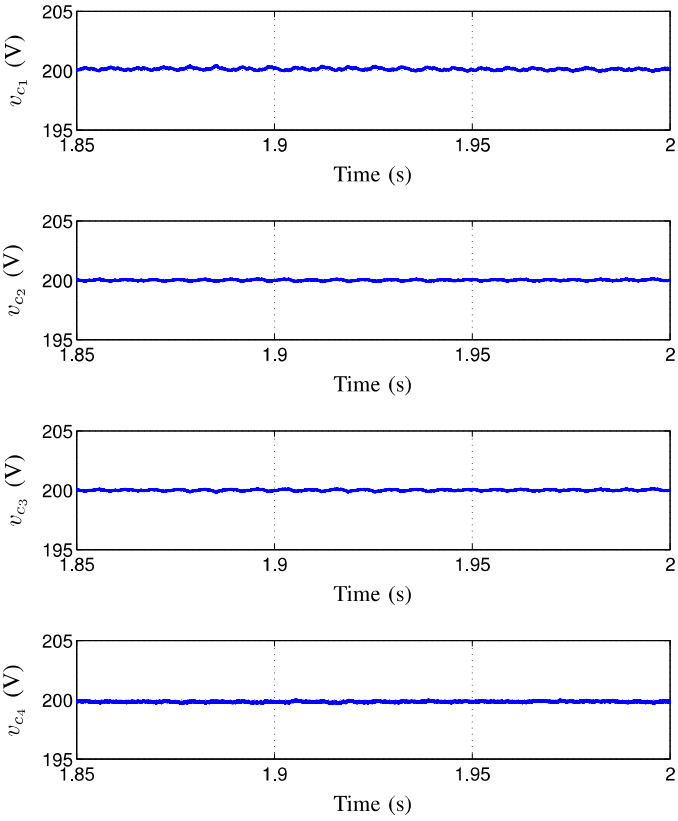

Fig. 10. Behavior of the dc-link capacitor voltages.

DCC operating as grid interface. The approach is based on an averaged dynamic model of the global system, which avoids the limitations of some modulation strategies where only a reduced subset of voltage levels can be accessed per phase in every switching cycle. The control approach introduces several variable transformations to simplify the model equations and

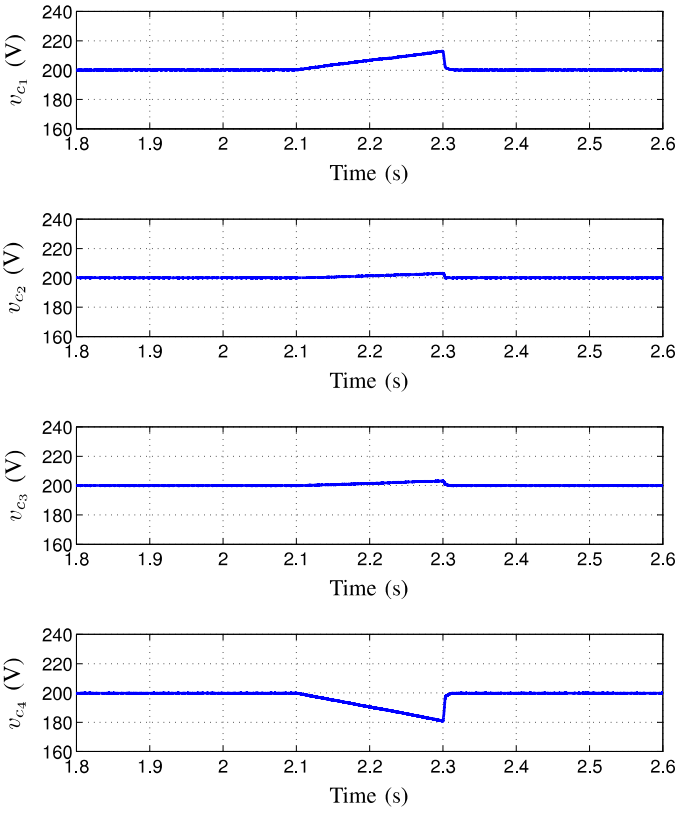

Fig. 11. Behavior of the dc-link capacitor voltages, when the proposed voltage balance controller is disconnected from $t = 2.1$ s to $t = 2.3$ s.

facilitate the controller design. Simulation results have shown the good performance of the system under the proposed controllers, which do not implement complex control strategies.

This is a key point to remark, since the design of the controllers is simple and different well-known control strategies can be applied, once the changes of variables are introduced in the model. For instance, for the current controller, a PI-type based control action is considered in this paper. In addition, the proposed approach require neither the utilization of auxiliary converters nor any other kind of additional circuitry. Compared with the vast majority of solutions proposed in the technical literature to cope with the regulation of five-level DCCs [14]–[19], it represents a relevant feature.

Furthermore, it is important to note that the proposed full decoupling control approach can also be applied to the rectifier configuration of the converter, considering some adjustments. To that end, the dynamics of the total dc-link voltage should be included in the model of the system and an accurate regulator of this voltage should be implemented. This is one of the future directions of research of the authors of this work, together with the extension of the modeling and control approach to the back-to-back five-level DCC topology.

ACKNOWLEDGMENTS

This work has been funded under grants MINECO-FEDER DPI2013-41891-R and DPI2016-75294-C2-1-R.

APPENDIX

Power-Invariant Form of the Clarke Transform

In a general manner, for certain given variables x_a, x_b and x_c, the power-invariant form of the Clarke Transform is defined by the change of variables

$$\begin{aligned} x_\alpha &= \sqrt{\frac{2}{3}}\left(x_a - \frac{1}{2}\,x_b - \frac{1}{2}\,x_c\right) \\ x_\beta &= \sqrt{\frac{2}{3}}\left(\frac{\sqrt{3}}{2}\,x_b - \frac{\sqrt{3}}{2}\,x_c\right) \\ x_\gamma &= \sqrt{\frac{2}{3}}\left(\frac{1}{\sqrt{2}}\,x_a + \frac{1}{\sqrt{2}}\,x_b + \frac{1}{\sqrt{2}}\,x_c\right). \end{aligned}$$

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