Behavioral Modeling of PWL Analog Circuits using Symbolic Analysis

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ABSTRACT[1]

Behavioral models are used both for top-down design and for bottom-up verification. During top-down design, models are created that reflect the nominal behavior of the different analog functions, as well as the constraints imposed by the parasitics. In this scenario, the availability of symbolic modeling expressions enable designers to get insight on the circuits, and reduces the computational cost of design space exploration. During bottom-up verification, models are created that capture the topological and constitutive equations of the underlying devices into behavioral descriptions. In this scenario symbolic analysis is useful because it enables to automatically obtain these descriptions in the form of equations. This paper includes an example to illustrate the use of symbolic analysis for top-down design.

1. INTRODUCTION

Circuit analysis is the cornerstone for electronic circuit engineering. On the one hand, it provides the keys to understanding the intricate mechanisms underneath the circuit operation. On the other hand, designers use analysis to obtain models of the circuit behavior – the basis on which this behavior can be predicted. However, manual analysis of even the simplest circuits encountered in practical applications is a complicated, time-consuming, and error-prone task. Symbolic analyzers are intended to relieve designers of systematic manual analysis tasks, thus letting them concentrate on creative issues.

The last generation symbolic analyzers are able to handle up to around 400 different symbols [1]. This permits, for example, to analyze circuits as complex as the rail-to-rail CMOS opamp of Fig.1(a) [2] with the small-signal transistor model of Fig.1(b) [3]-[5]. The analyzers capabilities include the calculation of *s*-domain expressions for all types of driving-point and transfer characteristics, the simplification of these expressions to retain only the dominant terms, the extraction of their poles and zeroes, etc.

Recently, different authors have focused also on the symbolic analysis of nonlinear circuits [6][7]. The most important advances have been obtained with those weak nonlinearities which can be represented through a few terms (typically

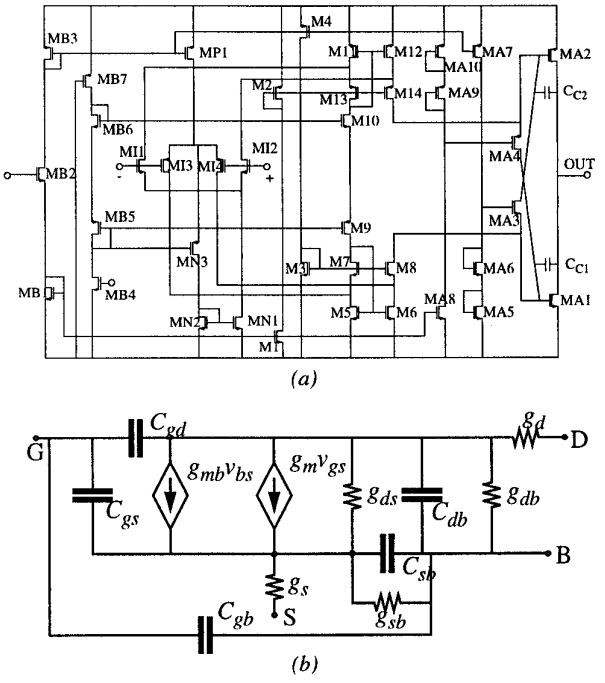

Figure 1. (a) Rail-to-rail opamp; (b) small-signal MOS transistor model.

3) of a power series expansion. In [6] systematic techniques are proposed for the automatic calculation of the Volterra kernels [8] that characterize the behavior of these weakly-nonlinear circuits in the frequency domain. However, the symbolic analysis of hardly-nonlinear circuits is yet in exploratory phase [7]. To date, no systematic technique is available to automate the calculation of a set of symbolic equations governing the large signal nonlinear behavior, either in the static or in the dynamic case.

This lack of nonlinear analysis limits the modeling capabilities of state-of-the-art symbolic analyzers. However, in many practical applications these limitations can be overcome by resorting to piecewise-linear (PWL) representations. For instance, these representations suffice to study the qualitative behavior of many practical dynamical circuits such as oscillators and comparators, as well as to approximate the transient response of opamps and comparators.

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2. BEHAVIORAL MODELING

A behavioral model is a set of equations that capture the operation of a circuit from its terminals. Behavioral models can also be given as circuital representations of these equations. Depending on the nature on the excitations and responses, the set of equations and its associated circuital representation can be static or dynamic, linear or nonlinear. For example, Fig.2 shows different behavioral models for an opamp. The first one is static and the others dynamic; the first two are linear and the others nonlinear. Circuital representations are included for each model.

The construction of a behavioral model does not strictly require to know the detailed circuit schematic. Neither the model circuital representation must reflect the circuit topology. Models can be built by, first, applying a suitable set of excitation-response pairs and, then, finding and tuning a math structure that reproduce these pairs within some prescribed error margin. Consider for example the OTA shown in Fig.3(a) and assume that we are interested only in its linear AC behavior. This can be modeled by h-parameters, which can be experimentally calculated in the lab by using a network analyzer in the configurations of Fig.3(c).

Alternatively, behavioral models can be constructed through the electrical analysis of the internal circuit schematic. For instance, assuming that the OTA schematic of

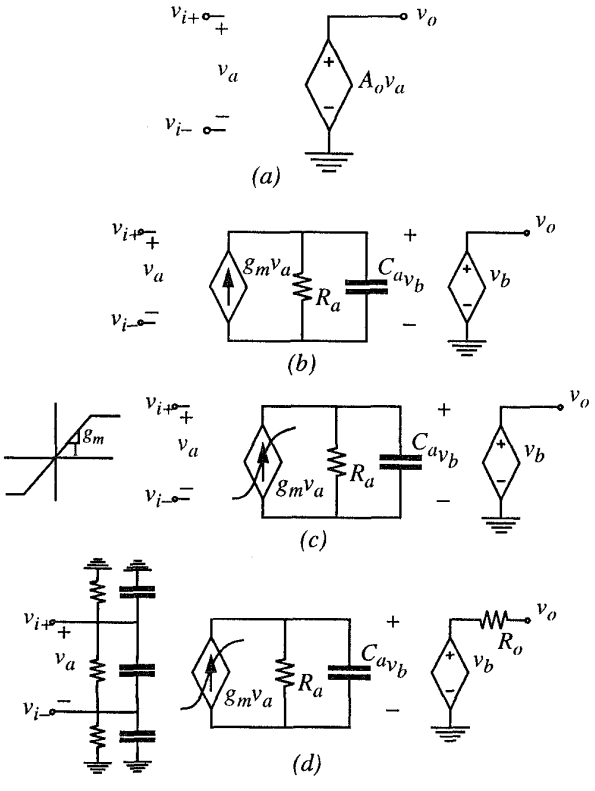
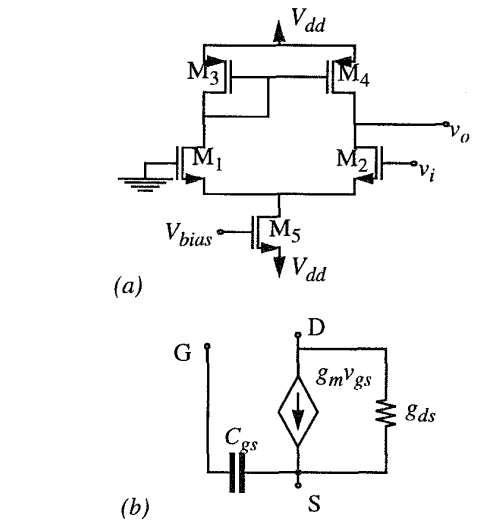


Figure 2. Opamp behavioral models.



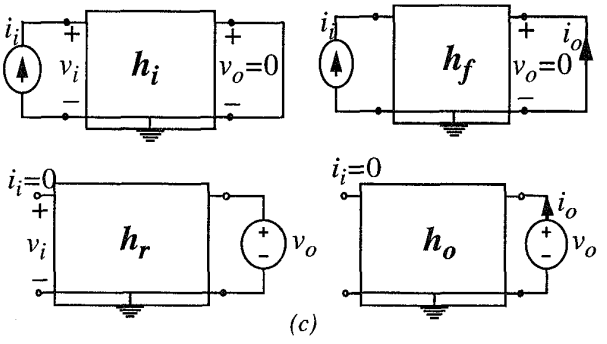


Figure 3. (a) Simple OTA; (b) simplified small-signal MOS transistor model; (c) black box modeling procedure for a two-port.

Fig.3(b) and the transistor model of Fig.3(c), a last generation symbolic analyzer such as SYMBA [9] would return the following h-parameter approximated expressions,

$$h_i(s) = \frac{g_{m3}(g_{m1}+g_{m2})}{sC_{gs2}g_{m1}g_{m3}+s^2C_{gs2}[g_{m1}(C_{gs3}+C_{gs4})+g_{m3}C_{gs1}]} + \frac{s[g_{m3}(C_{gs1}+C_{gs2})+(g_{m1}+g_{m2})(C_{gs3}+C_{gs4})]}{sC_{gs2}g_{m1}g_{m3}+s^2C_{gs2}[g_{m1}(C_{gs3}+C_{gs4})+g_{m3}C_{gs1}]}$$

$$h_f(s) = \frac{g_{ds1}g_{m3}+sg_{ds1}(C_{gs1}+C_{gs3}+C_{gs4})}{g_{m1}g_{m3}+s[g_{m1}(C_{gs3}+C_{gs4})+g_{m3}C_{gs1}]}$$

$$h_r(s) = \frac{g_{ds2}}{g_{m1}+sC_{gs1}}$$

$$h_o(s) = \frac{g_{ds1}g_{m3}+sg_{ds1}(C_{gs1}+C_{gs3}+C_{gs4})}{g_{m1}g_{m3}+s[g_{m1}(C_{gs3}+C_{gs4})+g_{m3}C_{gs1}]} \quad (1)$$

In practice, designers use their experience to build modular models, where functional substructures are used to represent the nominal circuit behavior as well as the parasitics. Thus, for example, Fig.2(a) captures the nominal opamp be-

havior; that of Fig.2(b) includes a first-order approximation to the dynamics associated to any voltage gain mechanism; and Fig.2(c) models the first stage transconductor nonlinearity. These three models focus on the transfer behavior. On the other hand, Fig.2(d) captures also to a first approach the driving-point behaviors at the circuit terminals.

The different functional substructures pertaining to a behavioral model can be tuned either through blackbox measurements or through analysis of the underlying circuit. In the case of PWL models, measurements are used to tune the nonlinear substructures while those linear ones are represented through their symbolic transfer functions. The example presented in the section below illustrates about the practical interest of these PWL models.

3. A PWL MODEL FOR TOP-DOWN TRANSIENT OPAMP OOPTIMIZATION

Consider the SC integrator of Fig.4(a) and assume the opamp represented by the PWL model of Fig.4(b) [10]. The transient observed in the transferring of the input voltage to the integrating capacitor contains a linear part an a nonlinear part. The linear part can be calculated symbolically from,

$$V_o(s) = \frac{C_i C_o}{\gamma_C}\frac{s^2+\frac{g_1}{C_1}s-\frac{g_{m1}g_{m2}}{C_1 C_o}}{s^2+2\alpha s+\alpha^2+\beta^2}\frac{V_I}{s}$$

$$V_1(s) = \frac{g_{m1}C_i(C_o+C_2)}{C_1\gamma_C}\frac{s+\frac{g_{m1}}{C_o+C_2}}{s^2+2\alpha s+\alpha^2+\beta^2}\frac{V_I}{s} \qquad (2)$$

$$V_a(s) = \frac{C_i(C_o+C_2)}{\gamma_C}\frac{\left(s+\frac{g_2}{C_o+C_2}\right)\left(s+\frac{g_1}{C_1}\right)}{s^2+2\alpha s+\alpha^2+\beta^2}\frac{V_I}{s}$$

where,

$$\gamma_C = C_iC_2+C_iC_o+C_2C_o+C_2C_p+C_oC_p$$
$$C_a = C_i+C_p+C_o$$
$$\alpha = \frac{g_2C_a}{2\gamma_C}+\frac{g_1}{2C_1} \qquad (3)$$
$$\beta = \sqrt{\frac{g_{m1}g_{m2}C_o}{C_1\gamma_C}+\frac{g_1g_2C_a}{2C_1\gamma_C}-\frac{g_1^2}{4C_1^2}-\frac{g_2^2C_a^2}{4\gamma_C^2}}$$

yielding,

$$\begin{aligned} v_o(t) &= A_{o1}+B_{o1}\exp(-\alpha t)\cos\beta t+C_{o1}\exp(-\alpha t)\sin\beta t \\ v_1(t) &= A_{11}+B_{11}\exp(-\alpha t)\cos\beta t+C_{11}\exp(-\alpha t)\sin\beta t \\ v_a(t) &= A_{a1}+B_{a1}\exp(-\alpha t)\cos\beta t+C_{a1}\exp(-\alpha t)\sin\beta t \end{aligned} \qquad (4)$$

where the coefficients are given as functions of the model parameters [10]. These equations remain valid while the following condition is fulfilled,

$$g_{m2}|v_1(t)| \le I_o \qquad (5)$$

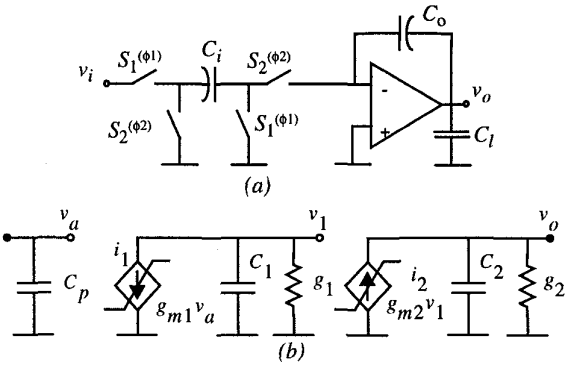


Figure 4. (a) SC integrator and, (b) opamp model.

Afterwards, the second model stage enters into saturation and the transient is described by the following equations,

$$V_o(s) = V_{o1}\frac{s+I_oC_a/(V_{o1}\gamma_C)}{s(s+g_2C_a/\gamma_C)}$$

$$V_1(s) = \frac{I_o}{g_{m2}}\left(\frac{s^2+\left(\frac{g_2C_a}{\gamma_C}-\frac{g_{m1}g_{m2}V_{a1}}{C_1I_o}\right)s-\frac{g_{m1}g_{m2}}{C_1\gamma_CI_o}(C_oI_o+g_2C_aV_{a1}-g_2C_oV_{o1})}{s(s+g_1/C_1)(s+g_2C_a/\gamma_C)}\right) \qquad (6)$$

$$V_a(s) = V_{a1}\frac{s+(C_oI_o+g_2C_aV_a-g_2C_oV_o)/(\gamma_CV_{a1})}{s(s+g_2C_a/\gamma_C)}$$

yielding,

$$\begin{aligned} v_o(t) &= A_{o2}+B_{o2}\exp[-p_2(t-t_1)] \\ v_1(t) &= A_{12}+B_{12}\exp[-p_1(t-t_1)]+C_{12}\exp[-p_2(t-t_1)] \\ v_a(t) &= A_{a2}+B_{a2}\exp[-p_2(t-t_1)] \end{aligned} \qquad (7)$$

where,

$$p_1 = \frac{g_1}{C_1} \qquad p_2 = \frac{g_2C_a}{\gamma_C} \qquad (8)$$

and the remaining coefficients are given as functions of the model parameters [10]. This second transient persists while the condition (5) holds. Afterwards, the transient is given by,

$$V_o(s) = \frac{V_{o2}}{s}\frac{s^2+\left(\frac{C_aI_o}{\gamma_CV_{o2}}+\frac{g_1}{C_1}\right)s+\frac{g_{m1}g_{m2}}{\gamma_CC_1V_{o2}}(C_oV_{o2}-C_aV_{a2})}{s^2+2\alpha s+\alpha^2+\beta^2} \qquad (9)$$

yielding,

$$v_o(t) = A_{o3}+B_{o3}\exp(-\alpha t)\cos\beta t+C_{o3}\exp(-\alpha t)\sin\beta t \qquad (10)$$

where the coefficients are, as in the previous expressions, given as functions of the model parameters.

The model has been validated by comparing its output waveform to that of obtained through detailed electrical simulation. The amplifier consisted of a fully-differential folded-cascode OTA whose core schematic and summarized performance are given in Fig.5. Said amplifier was designed to have small phase margin (around 45deg) to reduce power dissipation. Fig.6(a) shows the integrator output voltage during the integration phase obtained through electrical simulation (HSPICE) and that obtained using the model. Model parameters are also enclosed in Fig.5. A good concordance between both approximations is observed. A more general result is given in Fig.6(b) where the difference between the final value of the integrator output voltage and its ideal value is shown as a function of the input level.

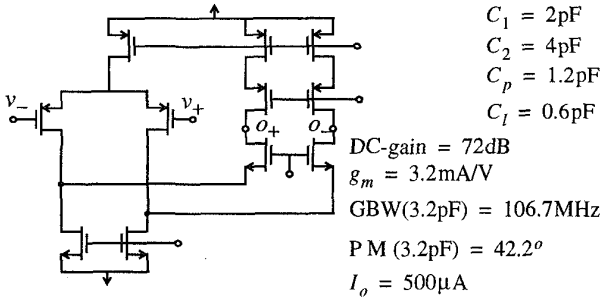


Figure 5. Fully differential OTA.

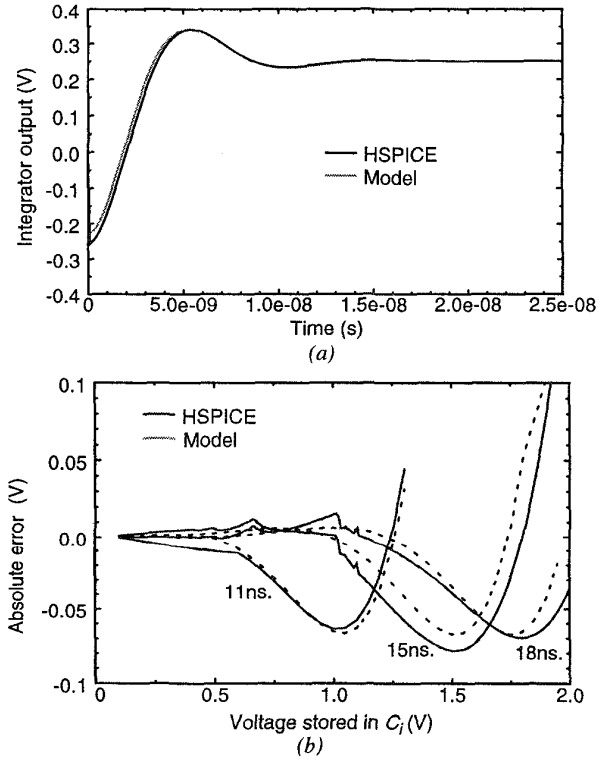


Figure 6. Simulated and calculated responses.

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