CMOS Current-Mode Chaotic Neurons

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ABSTRACT

This paper presents two nonlinear CMOS current-mode circuits that implement neuron soma equations for chaotic neural networks, and another circuit to realize programmable current-mode synapse using CMOS-compatible BJT's. They have been fabricated in a double-metal, single-poly 1.6μm CMOS technology and their measured performance reached the expected function and specifications. The neuron soma circuits use a novel, highly accurate CMOS circuit strategy to realize piecewise-linear characteristics in current-mode domain. Their prototypes obtain reduced area and low voltage power supply (down to 3v) with clock frequency of 500kHz. As regard to the synapse circuit, it obtains large linearity and continuous, linear, weight adjustment by explotation of the exponential-law operation of CMOS-BJT's. The full accordance observed between theory and measurements supports the development of future analog VLSI chaotic neural networks to emulate biological systems and advanced computation.

INTRODUCTION

Recent studies on real nerve membranes in neurophysiological experiments have shown that the dynamical behavior of biological neurons are much more complex (including chaotic response) than that exhibited by conventional models used in artificial networks, typically represented by simple threshold or sigmoid elements [1], [2]. Consequently, in the last years, new schemes of artificial neural networks have emerged whose purpose is to more realistically emulate the chaotic responses experimentally observed from biological systems. One of the simplest *chaotic neural networks* has been reported in [3], and constitutes a modification of the Nagumo-Sato model [4], where instead of following an all-or-none law for the action potential, modelled by an unit step output function $u(\bullet)$, the neuron shows a continuously graded stimulus-response curve, represented by a non-linear function $f(\bullet)$. The model in [3], illustrated in Fig. 1, is defined by the following finite-difference equations:

$$\begin{aligned} x_i(n+1) &= kx_i(n) - \alpha f(x_i(n)) + A_i(n) \\ y_i(n+1) &= f(x_i(n+1)) \end{aligned} \quad , \; n = 0, 1, \ldots \qquad (1)$$

where $x_i(n+1)$ and $y_i(n+1)$ are the internal state and the output of the ith chaotic neuron at the discrete time $n+1$, respectively; α and k are the scaling and damping factors of refractoriness (residual effect of a neuron once fired), respectively; and $A_i(n)$ is the input excitation at the instant n, given by

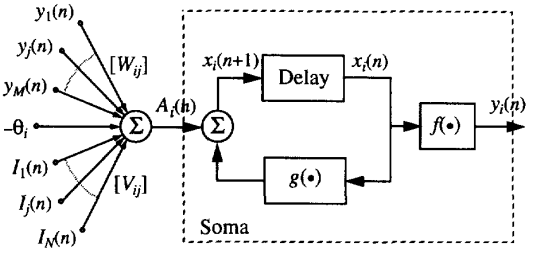


Figure 1 Analog computer concept for the chaotic neuron circuit. The nonlinear block is given by $g(x) = kx - \alpha f(x)$, according to (1).

$$A_i(n) = \sum_{j=1}^{M} W_{ij} y_j(n) + \sum_{j=1}^{N} V_{ij} I_j(n) - \theta_i \qquad (2)$$

where the first term computes the influence of the M neurons driving the ith neuron; the second, the excitation from the N external inputs, I_j; and θ_i is the threshold of the ith neuron. Lastly, $f(\bullet)$ constitutes the neuron output function represented by the piecewise-linear model

$$f(x) = \frac{|x+\varepsilon| - |x-\varepsilon|}{2\varepsilon} \qquad (3)$$

where ε is a positive number defining the steepness of the function.

Many studies on chaotic neural networks in general, and using the previous model in particular, reveal that such networks not only serve as an experimental vehicle in the study of sensory nerve systems, but also provide the means for important engineering applications. In this sense, chaotic neural networks have been proposed to solve difficult *optimization* problems [5], [6]; for *dynamical associative pattern classification* [7]; and for *signal detection* and *classification* in *noisy environments* [8], and it is foreseeable that new applications will arise in the near future.

In spite of the strong economical interest involving these applications, few up-to-date physical implementations of chaotic neurons have been proposed. Thus, it is advisable to give circuit realizations of these models. Furthermore, due to the technological trend towards system integration, these circuits must be well-suited for VLSI, and, if possible, compatible with standard low cost CMOS technologies.

The purpose of this communication is to provide monolithic implementations of the discrete-time chaotic

neuron described in (1), as well as for the Nagumo-Sato model that, previously stated, substitutes the nonlinear function in (3) by a unit step $u(\bullet)$. Also, a synapse circuit with continuous, linear programmability which employs CMOS-compatible BJT's is reported.

CURRENT MODE IMPLEMENTATIONS

Current-mode techniques have been employed to implement both neurons, following the conceptual diagram shown in Fig.1. Summation is easily realized exploiting KCL. The delay operation can be realized as a cascade of two track-and-hold switched-current stages, as proposed by Hughes et al. [9]. Fig. 2 shows the schematics for this block. Nonlinearities have been achieved using a novel, highly accurate CMOS circuit strategy to realize PL characteristics in current-mode domain. It is based on the rectifying characteristics of the current switch [10], which provides very high resolution and virtually zero current offset, not influenced by transistor mismatches (indeed, minimum size transistors were used in both prototypes). Fig. 3 shows the corresponding schematics for both PL functions. Current amplifiers can be implemented by properly ratioed bilateral current mirrors.

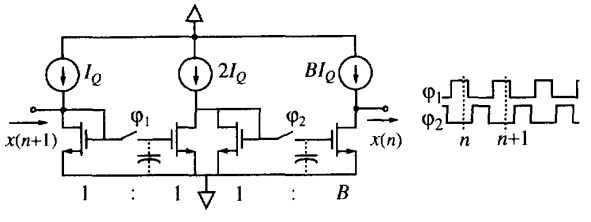
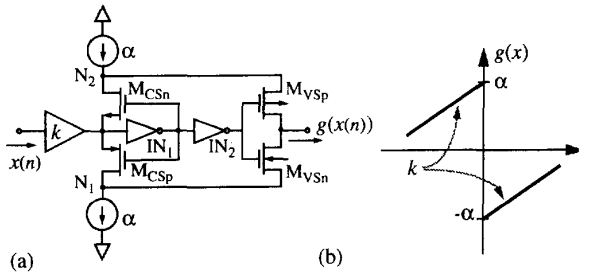
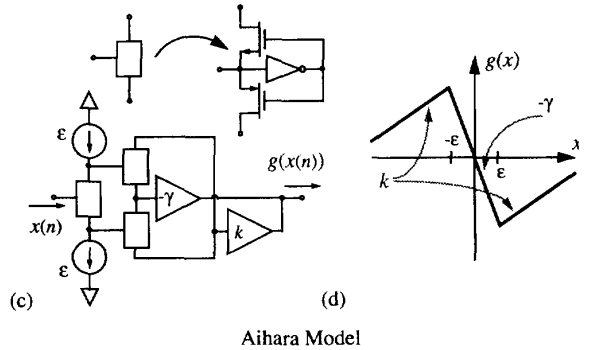


Figure 2 Current-mode track and hold circuit.



Nagumo-Sato Model



Aihara Model

Figure 3 Piecewise linear mapping circuits for the neurons.

Firstly, let us consider implementation of the nonlinear block, $g(\bullet)$, for the Nagumo-Sato model, according to the concept of Fig.1. Fig.3(a), which consists of two current sources (realized in practice by current mirror output branches), four transistors and two digital inverters, shows a conceptual schematic for the realization of the PL characteristics of Fig.3(b). Transistors M_{CSn} and M_{CSp} in Fig.3(a) operate as a current-controlled-current-switch, while transistors M_{VSn} and M_{VSp} operate as voltage-controlled current switches. Any positive input current increases the input voltage, turning M_{CSp} device ON, and since both devices in the current switch have the same gate voltage, M_{CSn} OFF. Simultaneously, the voltage at the second inverter output evolves to the high logic state, turning M_{VSn} ON and M_{VSp} OFF. Thus, a current $kx(n) - \alpha$ (obtained by KCL at node N_1) is directed to the output node through the transistor M_{VSn} -- the right-hand piece of Fig.3(b) is implemented in this manner. Similarly, negative input currents turn M_{CSn} and M_{VSp} ON, so that a current $kx(n) + \alpha$ circulates through M_{VSp} to the output node. The output response of the neuron can be taken from the voltage at the output of the inverter IN_2 which swings from rail to rail depending upon the sign of the input current, thus resembling the required unit step function in voltage mode. Obviously this binary signal must be combined with analog switches and current sources for properly driving other neurons in the network.

Since current discrimination in the proposed circuit relies on integration function performed at the input node, resolution is very high, not influenced by transistor mismatches (measurements from the CMOS prototype display resolution of 12pA's). Operation speed is also very high, limited mainly by nonlinear transients in the transistors that implement the current sources used to drive nodes N_1 and N_2. Also, the feedback created by inverter IN_1 yields significant reduction of the dead-zone exhibited by the driving point characteristics measured at the input node, that is proportional to $(V_{Tn} + |V_{Tp}|) / A_{inv}$, where V_{Tn} and V_{Tp} are the threshold voltages for the transistors and A_{inv} is the inverter DC gain. This is an appealing feature that enables reduction of interstage loading errors caused by finite equivalent MOS transistors Early voltages.

Concerning the implementation of the PL characteristic shown in Fig. 3(d) for the Aihara model, Fig. 3(c) shows the corresponding schematic. The current switches, together with the current sources, are used to discriminate the input current into three paths according if $x(n)$ is lower than $-\varepsilon$, greater than ε, or is comprised between both values. In the two first cases, the paths are routed to the same node and amplified by k, while if $x(n) \in [-\varepsilon, \varepsilon]$ the current is amplified by $-\gamma$, where $\gamma = \alpha/\varepsilon - k$, according to (1) and (3). The output of the neuron can be easily taken in this case by replication and scaling the output current of the amplifier with gain $-\gamma$.

PROGRAMMABILITY ISSUES FOR CURRENT MODE BLOCKS

In current-mode domain two different approaches to programmability can be considered depending on the nature of the associated controlling signals: discrete programmability, where controlling signals are digital, and continuous programmability, where controlling signals are analog. Discrete programmability can be incorporated in a very simple way, by analog multiplexing of current contributions from different mirrors. These mirrors can either implement fixed templates (with application, for instance, in cases where well-defined tasks must be sequentially performed), or be binary-weighted (for more general application). Discrete programmability provides ease of controllability and accurate results, at the cost of a strong area penalty.

For reduced area and continuous weight adjustment, analog programmability should be considered. A simple way to achieve analog programmability is using tunable transconductors, as the one shown in Fig. 4(a). Fig. 4(b) shows a programmable current mirror using this transconductor. Two different situations arise depending on whether transistors operate in weak or in strong inversion. Analysis for both operating conditions shows the following,

$$\left.\frac{i_o}{i_{in}}\right|_{strong} = \sqrt{\frac{\beta_2 I_{B2}}{\beta_1 I_{B1}}} \qquad \left.\frac{i_o}{i_{in}}\right|_{weak} = \frac{I_{B2}}{I_{B1}} \qquad (4)$$

As can be seen, the dependence is linear for weak inversion; hence, this latter case provides larger weight adjustment ranges. It is illustrated in Fig. 5, showing the current weight as a function of I_{B2}/I_B for different values of I_{B1}/I_B, where I_B is a normalization factor of value 10nA for weak inversion (Fig. 5(a)) and 50μA for strong inversion (Fig. 5(b)). Also, nonlinearity cancellation is exact in weak inversion due to the exponential nature of current to voltage characteristics, while it is only approximate for strong inversion: nonlinearity in the weak inversion case is less than 1% up to $i_o=I_{B2}$, while the corresponding value for strong inversion is $i_o=0.13I_{B2}$. Drawbacks of weak inversion are low accuracy, due to mismatch, and reduced speed. These can be overcome by using CMOS compatible lateral BJTs [11], which exhibit exponential feature for larger current ranges, and with excellent matching properties [12].

EXPERIMENTAL RESULTS

Both neurons have been fabricated in a double-metal, single-poly 1.6μm CMOS technology. Fig. 6 shows the corresponding microphotographs. Some extra miscellaneous circuitry has been added to both circuits to enable testing the output current and the possibility to either open or close the feedback loop. Dummy switches were also added to reduce the influence of clock feedthrough. All current amplifiers were binary-weighted for the issue of programmability. Bias current I_Q for the delay stages was set

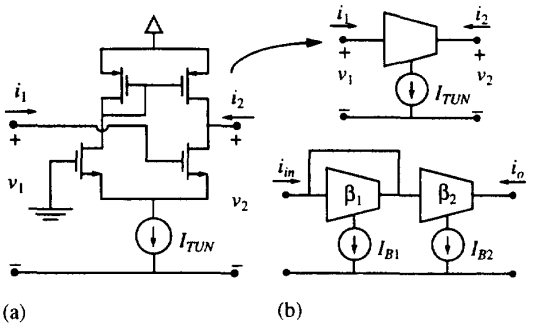


Figure 4 (a)Tunable transconductor. (b) Programmable current mirror.

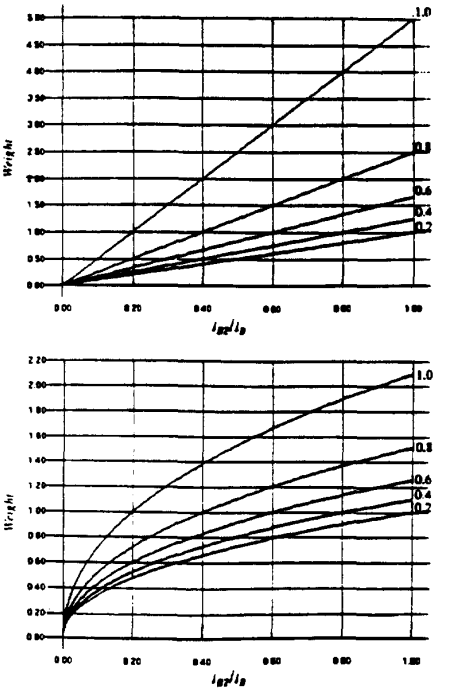
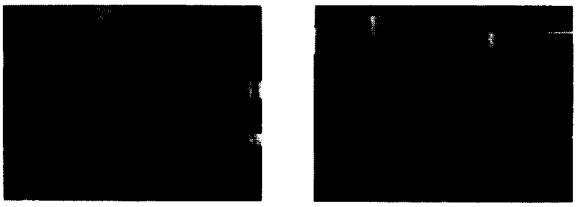


Figure 5 Weight (i_o/i_{in}) variation with I_{B2}/I_B for different values of I_{B1}/I_B in Fig. 4(b).
(a) Transconductors operating in weak inversion, I_B = 10nA.
(b) Transconductors operating in strong inversion, I_B = 50μA.

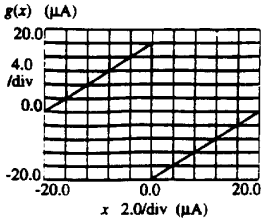
to 50μA. Total area occupation is 0.096mm^2 for the Nagumo-Sato neuron, and 0.225mm^2 for the Aihara neuron.

Fig. 7 shows the characteristics measured in open loop for both circuits, using the HP4145 semiconductor analyzer, with a rail-to rail power supply of only 3v. For the Nagumo-Sato neuron (Fig.7(a)), α = 20μA, k = 1 and the input ranges from −20μA to 20μA. For the Aihara neuron (Fig.7(b)), ε = 2μA, γ = 10 , k = 1 and the input sweeps from −10μA to 10μA. In both prototypes deviation from linearity is less than 0.2%, and the measured current offset amounts to few pA's.

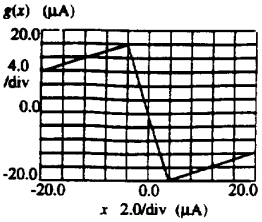


(a) Nagumo-Sato Model (b) Aihara Model

Figure 6 Microphotographs of the prototypes.



(a) Nagumo-Sato Model

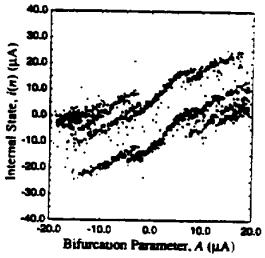


(b) Aihara Model

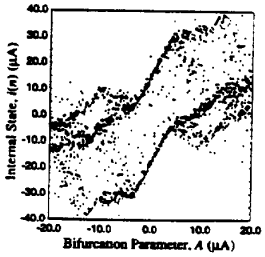
Figure 7 Measured open-loop characteristics.

Fig. 8 shows the experimental bifurcation trees for both neurons, when the damping factor $k = 0.5$ and the neuron excitation A, taken as the bifurcation parameter, varies from $-20\mu A$ to $20\mu A$. All other parameters were fixed to the values previously cited. Clock frequency was set to 500kHz.

All these measurements are in full accordance with the theoretical results. Also, given the reduced area, as well as operating with only 3v power supply, we believe both neuron implementations are very appropriate for high density chaotic neural networks on a single chip.



(a) Nagumo-Sato Model



(b) Aihara Model

Figure 8 Bifurcation diagrams.

RERERENCES

[1] G. Matsumoto, K. Aihara, Y. Hanyu, N. Takahashi, S. Yoshizawa and J. Nagumo: "Chaos and Phase Locking in Normal Squid Axons". *Physics Letters A*, Vol. 123 pp. 162-166, Aug. 1987.

[2] C. A. Skarda and W. J. Freeman: "How Brains make chaos in order to make sense of the world". *Brain and Behavioral Science*, Vol. 10, pp. 161-195, 1987.

[3] K. Aihara, T. Takabe and M. Toyoda: "Chaotic Neural Networks". *Phys. Lett. A*, Vol. 144, pp. 333-340, Mar. 1990.

[4] J. Nagumo and S. Sato: "On a Response Characteristic of a Mathematical Neuron Model". *Kybernetics*, Vol. 10, pp. 155-164, 1972.

[5] K. Judd and K. Aihara: "Neural Networks and Chaos". *Proc. of the* 1992 *IEEE Int. Symp. on Circuits and Systems*, pp. 2765-2768, May 1992.

[6] M. Inoue and A. Nagayoshi: "A Chaos Neuro-Computer". *Phys. Lett. A*, Vol.158, pp. 373-376, 1991.

[7] M. Adachi et al.: "Nonlinear Associative Dynamics in a Chaotic Neural Network". *Proc. of the 2nd International Conference on Fuzzy Logic & Neural Networks*, pp. 947-950, Jul. 1992.

[8] D. L. Birx and S. J. Pipenberg: "Chaotic Oscillators and Complex Mapping Feed Forward Networks (CMFFNS) for Signal Detection in Noisy Environments". *Int. Joint Conf. on Neural Networks*, Vol.II, pp. 881-888, Jun. 1992.

[9] J. B. Hughes, I. C. Macbeth and D. M. Patullo: "Switched Currents Filters". *IEE Proceedings*, Vol. 137, Pt. G, No. 2, pp. 156-162, April 1990.

[10] Z. Wang: "*Current-Mode Analog Integrated Circuits and Linearization Techniques in CMOS Technology*". Hartung-Gorre Verlag, Konstanz 1990.

[11] E.A. Vittoz: "MOS Transistors Operated in the Lateral Bipolar Mode and Their Application in CMOS Technology". *IEEE J. Solid-State Circuits*, Vol. SC-18, pp 273-279, 1983.

[12] T. Pan and A.A. Abidi: "A 50dB Variable Gain Amplifier Using the Parasitic Bipolar Transistors in CMOS". *IEEE J. Solid-State Circuits*, Vol. SC-24, pp 951-961, 1989.