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CMOS OTA-C High-Frequency Sinusoidal Oscillators

Bernabé Linares-Barranco, Angel Rodríguez-Vázquez,
Edgar Sánchez-Sinencio, and José L. Huertas

Abstract—**Several topology families are given to implement practical CMOS sinusoidal oscillators by using operational transconductance amplifier–capacitor (OTA-C) techniques. Design techniques are proposed taking into account the CMOS OTA's dominant nonidealities. Building blocks are presented for amplitude control, both by AGC schemes and by limitation schemes. Experimental results from 3- and 2-μm CMOS (MOSIS) prototypes showing oscillation frequencies up to 69 MHz are obtained. The amplitudes can be adjusted between 1 V peak to peak and 100 mV peak to peak. Total harmonic distortions from 2.8% down to 0.2% have been experimentally measured in the laboratory.**

I. INTRODUCTION

THE USE OF circuits composed of operational transconductance amplifiers and capacitors (OTA-C's) has been demonstrated to be potentially advantageous for the synthesis of high-frequency continuous-time monolithic analog operators, either linear [1]–[4], [11] or nonlinear [5]. One basic reason for the high-frequency potential of these circuits comes from the fact that the OTA is used in a local open loop. It means that no additional constraints are imposed on the frequency response due to local feedback-induced pole displacements [2]. Another advantage of open-loop OTA-based circuits is that the transconductance gain of the OTA is used as a design parameter. In a typical OTA architecture [12], this gain can be adjusted either by changing the tail current of a differential pair (fine adjustment) or by using digitally controlled current mirrors (coarse adjustment) [4]. Programmability is hence an inherent property of OTA-C circuits. Based upon the previous considerations, it may be expected that the transconductance amplifier–capacitor oscillators (TACO's) overcome the limitations in frequency and tunability of conventional op-amp-based *RC*-active oscillators. TACO's could then be applied for the design of high-frequency voltage-controlled sinusoidal oscillators (VCO's) with potential application in communication systems [6] and in the tuning of active filters [1]. In a companion paper [7] the authors have explored the synthesis of TACO's from classical oscillator models, namely quadrature and bandpass-based. The experimental results measured from discrete

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B. Linares-Barranco is with the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843 and the Departmento de Diseño Analógico, Centro Nacional de Microelectrónica, Universidad de Sevilla, 41012 Sevilla, Spain.

A. Rodríguez-Vázquez and J. L. Huertas are with the Departmento de Diseño Analógico, Centro Nacional de Microelectrónica, Universidad de Sevilla, 41012 Sevilla, Spain.

E. Sánchez-Sinencio is with the Department of Electrical Engineering, Texas A&M University, College Station, TX 77843.

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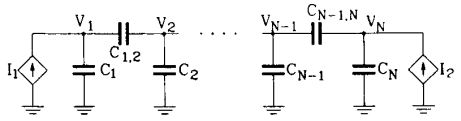


Fig. 1. General topology for the generation of second-order OTA-C oscillators.

bipolar prototypes showed good potential of the TACO's for high-frequency VCO's. Also, a 3-μm CMOS TACO including a limiting mechanism for controlling the amplitude has been reported [8] exhibiting a 10-MHz frequency and THD down to 0.2%. In this paper we first present a number of new architectures that can be systematically obtained from a general idealized TACO topology [9] and then provide experimental results for 2- and 3-μm CMOS prototypes up to 69 and 56 MHz, respectively. The results demonstrate that it is possible to implement high-frequency monolithic VCO oscillators based on simple OTA-C techniques and the modeling of the dominant OTA parasitic effects [3], [7]. Furthermore, we show that based on a general TACO structure, conventional and unconventional structures can be derived.

II. OTA-C Oscillator Structures

In this paper we are focusing on oscillators which can be ideally described by a second-order characteristic equation:

$$s^2 - bs + \Omega_0^2 = 0. \tag{1}$$

Fig. 1 shows a general topology for a second-order OTA-C oscillator structure [9]. The voltage-controlled current sources in this topology,

$$I_1 = \sum_{i=1}^{N} g_{1i} V_i \qquad I_2 = \sum_{i=1}^{N} g_{2i} V_i \tag{2}$$

can be implemented by connecting OTA's in parallel, one per each different term in (2).

Parameters b and Ω_0^2 are given as functions of the OTA transconductance gains g_{ij} and capacitor values. The basic TACO design goal is to achieve separate control of these former parameters with a minimum component count. We have systematically obtained different topologies from Fig. 1 to provide this feature. Some of the more interesting and practical ones are shown in Fig. 2. The corresponding expressions for b and Ω_0^2 are given in Table I. These structures involve a trade-off between complexity and degrees of freedom. At one end we will have structures with a minimum number of components but with a very limited degree of freedom. At the other, the structures will have larger component counts and more degrees of freedom. Nevertheless, we believe it is worthwhile to include the different structures since they are application dependent.

Ideally, for oscillation, the transconductance gains of Fig. 2 must be trimmed to yield $b = 0$. However, in practical oscillators, due to the influence of parasitics, the poles are displaced from their nominal positions ($s_p = \pm j\Omega_0$) to either the right or the left side of the complex frequency plane. For that reason, the oscillator must be designed to have its poles initially located inside the right-half complex frequency plane in order to assure self-starting operation, i.e., $b \geqslant \epsilon$, and ϵ is

TABLE I
Ideal Expressions of b and Ω_0^2 for the Different TACO Structures

$(g_{m1} - g_{m2})C_3$	b_c	2OTA3C
$\dfrac{g_{m1}g_{m2}}{(C_1 + C_3)(C_2 + C_3) - C_3^2}$	Ω_{0c}^2	
$\dfrac{g_{m3}C_2 - g_{m4}C_1}{C_1C_2}$	b_c	4OTA2C
$\dfrac{g_{m1}g_{m2} - g_{m3}g_{m4}}{C_1C_2}$	Ω_{0c}^2	
$(g_{m3} - g_{m4})C_2$	b_c	Quadrature
$\dfrac{g_{m1}g_{m2}}{C_1C_2}$	Ω_{0c}^2	
$(g_{m3} - g_{m4})\dfrac{C_1C_2C_3}{(C_1 + C_3)(C_2 + C_3)}$	b_c	4OTA4C
$\dfrac{g_{m1}g_{m2}\left(1 + \dfrac{C_1}{C_3}\right)\left(1 + \dfrac{C_2}{C_3}\right) - g_{m3}g_{m4}\dfrac{C_1C_2}{C_3^2}}{C_1C_2}$	Ω_{0c}^2	

a slightly positive number [6]. Besides, nonlinearities have to be considered to explain the existence of stable oscillations. Using the natural nonlinear saturation characteristics of the OTA is the simplest form of limiter. Connecting a nonlinear resistor with a driving-point characteristic [7] is another approach providing better controllability. Finally, exploiting the bias terminals of the OTA's to implement an automatic gain control (AGC) mechanism is a more sophisticated scheme requiring additional circuitry but providing reduced harmonic distortion. These two latter alternatives, external limitation and AGC, have been used in the practical implementations included herein.

III. Influence of OTA Parasitics

In Table I we assume that the OTA performs as an ideal voltage-controlled current source. Some experimental errors can be expected as a consequence of using such an ideal model. For extreme frequencies (both high and low) the resulting errors are very large to be tolerated. Hence, for accurate TACO design at these extreme frequencies, OTA parasitics cannot be ignored in analyzing the proposed structures. Experimental observations [7], [10] reveal that only three parasitics have to be considered to obtain a valid design technique up to at least 69 MHz, as is demonstrated in the experimental results included in this paper:

a) output conductance $G_{oj}, 1 \leqslant j \leqslant 4$,
b) output and input capacitances, and
c) transconductance frequency dependency, $g_{mj} \rightarrow g_{mj}\epsilon(s) \cong g_{mj}(1 - s/\omega_j)$, $1 \leqslant j \leqslant 4$.

The following characteristic equation is obtained by using the describing function approach and considering the influence of parasitics:

$$s^2 - b_c s + \Omega_{0c}^2 = 0 \tag{3}$$

where b_c and Ω_{0c}^2 are functions of the transconductances $g_{mj}(1 \leqslant j \leqslant 4)$, capacitances $C_i(1 \leqslant i \leqslant 3)$, output conductances $G_{oj}(1 \leqslant j \leqslant 4)$, and parasitic zeros $\omega_j(1 \leqslant j \leqslant 4)$.

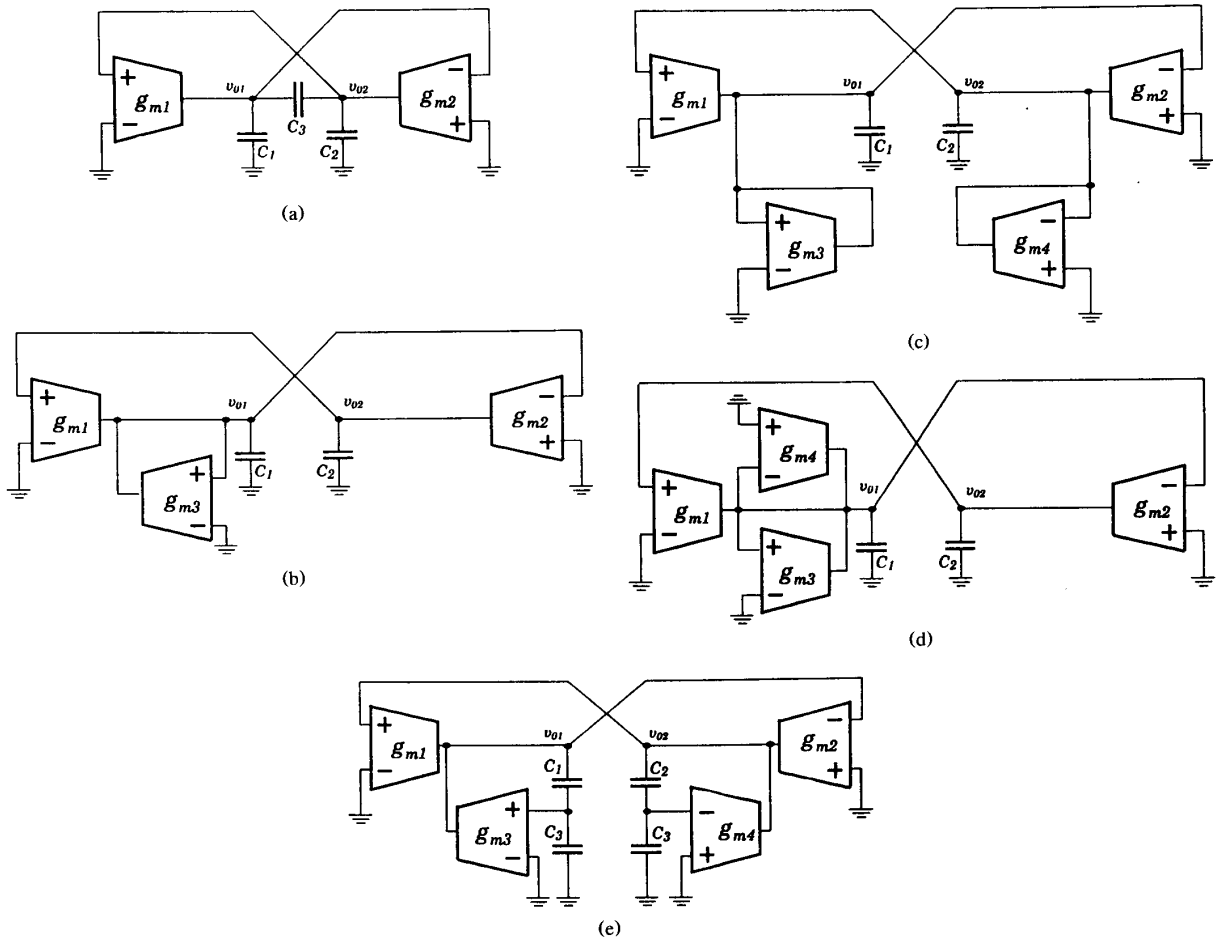


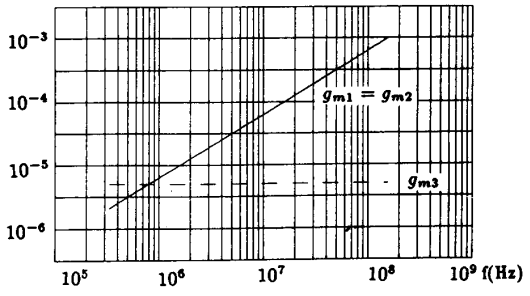
Fig. 2. OTA-C oscillator structures: (a) 2OTA3C, (b) 3OTA2C, (c) 4OTA2C, (d) quadrature, and (e) 4OTA4C.

Parasitics make the TACO oscillation condition b_c and the oscillator frequency Ω_{0c}^2 depend on all the transconductance gains. It means that any intent to change Ω_{0c}^2 by any transconductance gain will also produce a change in b_c and, hence, in the amplitude of the oscillations. For instance, in the 4OTA2C TACO, we can, ideally, change Ω_{0c}^2 via g_{m1} and g_{m2}, without affecting b. However, when parasitics are taken into account, g_{m3} and g_{m4} must also be tuned to maintain b_c constant. The influence of parasitics can be assessed from Fig. 3 corresponding to the 4OTA2C TACO. Fig. 3(a) shows trimming curves for the transconductance gains for the VCO operation and assuming the OTA's are ideal. Fig. 3(b) plots the corresponding curves in the case where parasitics are taken into account. Observe that one of the transconductance gains g_{m3} or g_{m4} can be made zero at any frequency. For low frequencies it is possible to make $g_{m4} = 0$ while at high frequencies $g_{m3} = 0$. At low frequencies, the output impedance (i.e., the OTA voltage gain) of the OTA's makes the oscillator deviate from the ideal (nonparasitic) behavior, while at high frequencies, it is the transconductance frequency dependence (excess phase) that produces the deviation. A way to avoid performance degradation due to parasitics and hence to yield high frequencies from the proposed TACO's is to use a predistortion technique based on the analysis of the parasitic's influence. We have used this method. The experimental results we have obtained confirm the validity of our approach.

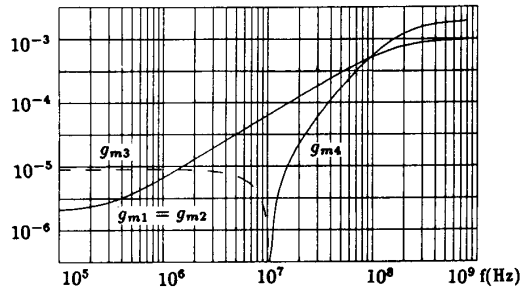
IV. Experimental Results

Three oscillator microchips were designed and fabricated in the CMOS p-well process, either 3-μm double metal or 2-μm double metal and double poly (through and thanks to MOSIS).

First Prototype: The prime objective of this first prototype, fabricated in the 3-μm double-metal process, was to obtain a high enough oscillating frequency so that it could be considered a radio frequency. To fulfill this requirement, an OTA with a very high transconductance g_m was needed. The OTA of Fig. 4 was designed for this purpose. Note that the architecture is a very simple one. The reason is that it can provide larger tuning ranges than linearized OTA's. On the other hand, since this OTA is going to be biased by a very large tail current (up to almost 10 mA), there is no need for a linearization scheme. Table II shows the basic dc parameters of this OTA as a function of the bias voltage. The



(a)



(b)

Fig. 3. Tuning of the g_m's for the VCO operation using the 4OTA2C: (a) without parasitics, and (b) with parasitics.

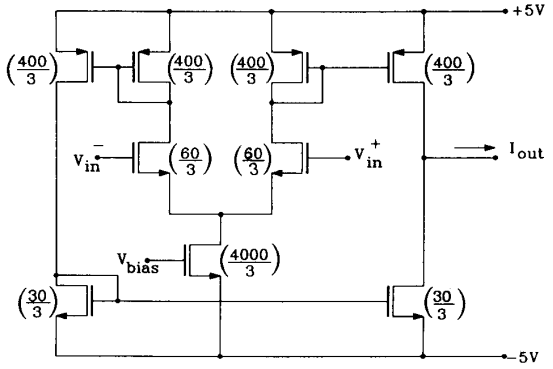


Fig. 4. A 3-μm CMOS OTA.

oscillator structure built was a quadrature oscillator (see Fig. 2(d)), in which the OTA of transconductance g_{m3} was suppressed according to the predistortion technique that results from the OTA parasitic's influence, as is shown in Fig. 3(b). External limiters were included to control the amplitude. The frequency of the oscillator could be tuned between 12.0 and 56.1 MHz. The distortion measured at 56.1 MHz was 2.5%. In Table III the dependence of the oscillation frequency on the biasing (see V_{bias} in Fig. 4) of the OTA's is shown. According to the parasitics' influence, the relation between oscillating frequency ($\Omega_0 = 2\pi f_0$), transconductance g_{mi} of the different OTA's, capacitors ($C_1 = C_2 =$ 5 pF), and parasitics (output impedances G_{oi}, and dominant

TABLE II
EXPERIMENTAL CHARACTERIZATION OF OTA

V_{bias}	R_0	g_m	I_b
−2.72	2.77 kΩ	2.49 mmhos	9.65 mA
−2.98	3.00 kΩ	2.38 mmhos	9.60 mA
−3.19	3.78 kΩ	2.12 mmhos	9.30 mA
−3.40	6.85 kΩ	1.90 mmhos	6.10 mA
−3.51	9.47 kΩ	1.76 mmhos	4.20 mA
−3.61	13.82 kΩ	1.61 mmhos	2.70 mA
−3.68	18.91 kΩ	1.43 mmhos	1.75 mA
−3.80	48.50 kΩ	0.932 mmhos	780 μA
−3.88	101.00 kΩ	0.638 mmhos	490 μA

TABLE III
EXPERIMENTAL CHARACTERIZATION OF OSCILLATOR

OTA1 OTA2	OTA4	Frequency
−2.9 V	−3.39 V	56.1 MHz
−3.19 V	−3.35 V	55.5 MHz
−3.40 V	−3.35 V	50.5 MHz
−3.51 V	−3.37 V	46.1 MHz
−3.61 V	−3.41 V	40.9 MHz
−3.68 V	−3.51 V	38.2 MHz
−3.80 V	−3.66 V	31.3 MHz
−3.88 V	−3.80 V	24.3 MHz
−3.96 V	−3.84 V	12.4 MHz
−3.98 V	−3.86 V	12.0 MHz

parasitic pole ω_i of g_{mi}) is given for this oscillator structure by [10]

$$\Omega_0^2 = \frac{g_{m1}g_{m2} + G_{o2}(g_{m4} + G_{o1} + G_{o4})}{C_2\left(C_1 - \dfrac{g_{m4}}{\omega_4}\right) + \dfrac{g_{m1}g_{m2}}{\omega_1\omega_2}}. \tag{4}$$

To verify the accuracy of this expression, let us focus on Table III for the case of 24.3 MHz of oscillating frequency. For this case, $g_{m1} = g_{m2} = 0.64$ mmhos, $g_{m4} = 0.93$ mmhos, $G_{o1}^{-1} = G_{o2}^{-1} = 101$ kΩ, $G_{o4}^{-1} = 48.5$ kΩ, $C_1 = C_2 \simeq 5$ pF, and $\omega_1 \simeq \omega_2 \simeq \omega_4 \simeq 2\pi \times 75$ MHz. According to (4) this would yield a frequency of

$$f_0 = \frac{\Omega_0}{2\pi} = 26 \text{ MHz} \tag{5}$$

which is very close to the 24.3 MHz experimentally measured.

Second Prototype: A second microchip was fabricated in the 2-μm double-poly, double-metal process in order to test the model oscillator structures proposed in this paper. The chip contains the three oscillators 2OTA3C, 4OTA2C, and 4OTA4C. This time a linearized OTA was used, as proposed by Nedungadi and Geiger [11]. The maximum bias current for the differential pair stage is less than 2 mA. To obtain large g_m values an additional current gain was added at the output current mirrors. In all these cases, the amplitude was controlled by limitation, using the CMOS nonlinear resistor of Fig. 5 [8], [10]. The maximum frequencies measured for the 2OTA3C, 4OTA2C, and 4OTA4C were 45.5, 49.8, and 69.0 MHz, respectively. Fig. 6 illustrates the variation of the frequency with the OTA bias voltage for each structure.

Third Prototype: A third microchip was designed in order to evaluate the performance of an OTA-C oscillator with AGC. A key component for the success of such a control loop is a peak detector. The oscillator will be made to operate between 3 and 13 MHz, approximately. In order for

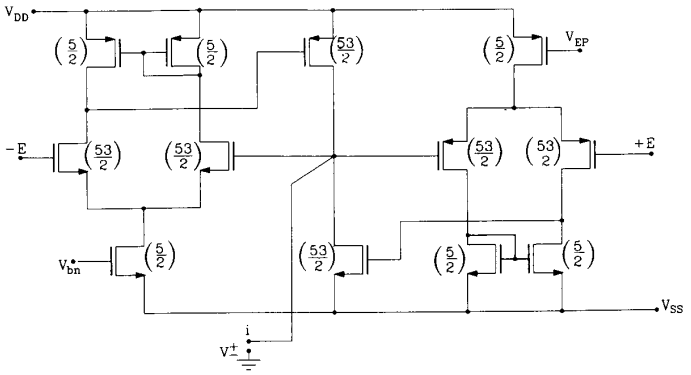


Fig. 5. CMOS implementation of the limiter.

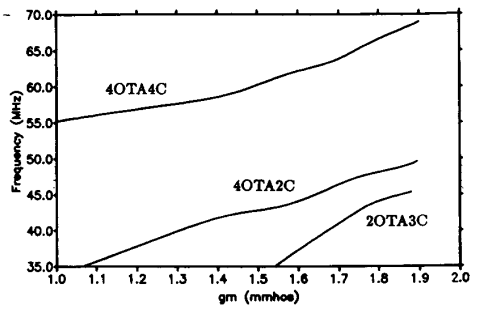


Fig. 6. Oscillation frequency versus OTA transconductances for 2OTA3C, 4OTA2C, and 4OTA4C oscillators.

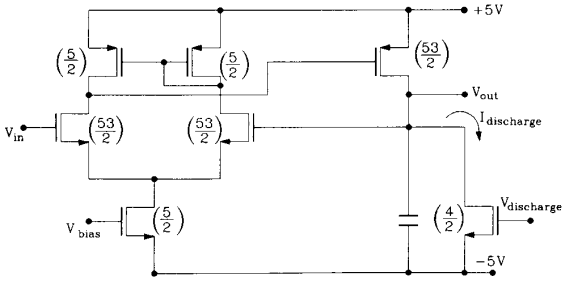


Fig. 7. CMOS peak detector.

the peak detector to cover this range and operate well at these frequencies a very simple circuit was chosen, as shown in Fig. 7. The performance of this peak detector was measured separately. By retuning the bias terminals V_{bias} and $V_{discharge}$ (see Fig. 7), the peak detector was able to extract a 1-MHz signal from a 40-MHz carrier, a 250-kHz signal from a 1-MHz carrier, or a 300-Hz signal from a 10-kHz carrier [10]. The oscillator structure used was a 4OTA2C, as shown in Fig. 8. The integrator and summer, added to the AGC loop in order to make it stable [10], are implemented using OTA-C techniques. The relationship between the oscillation frequencies and the bias voltage of OTA1 and OTA2 is shown in Fig. 9 for different values of the oscillation amplitude.

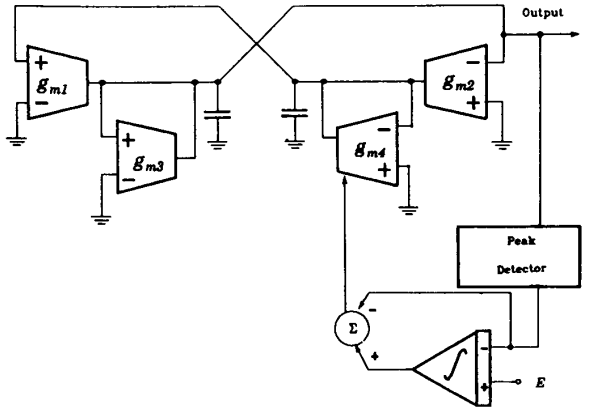


Fig. 8. 4OTA2C oscillator with AGC.

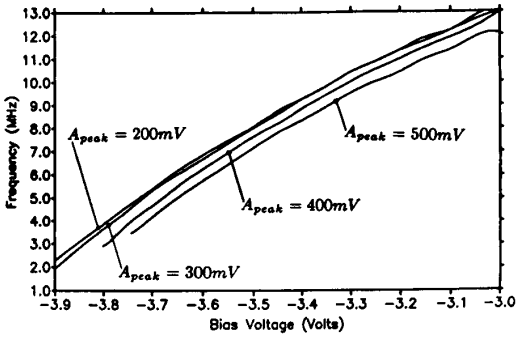


Fig. 9. Frequency versus bias voltage for different peak amplitudes.

V. Conclusions

A general approach for the systematic design of OTA-C oscillator structures is presented. Some novel oscillators are obtained and have been fabricated on silicon. Oscillation frequencies of up to 69 MHz were measured. A wide-range simple peak detector has been fabricated and included in an AGC loop of one of the oscillators. The influence of the OTA's basic parasitics is discussed and verified in the opera-

tion of the oscillators. In summary, the overall well-behaved performance of OTA-C oscillators for high frequencies has been demonstrated.

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Two Novel Fully Complementary Self-Biased CMOS Differential Amplifiers

Mel Bazes

Abstract—**Two novel CMOS differential amplifiers are presented. Both differ from conventional CMOS differential amplifiers in having fully complementary configurations and in being self-biased through negative feedback. The amplifiers have been applied as precision high-speed comparators in commercial VLSI CMOS integrated circuits.**

I. Introduction

THIS brief paper presents two novel CMOS differential amplifiers. The first differential amplifier is intended for applications in which the input common-mode range is relatively limited; this amplifier is denoted a complementary self-biased differential amplifier (CSDA) [1]. The second differential amplifier is intended for applications in which the input common-mode range is bounded only by the supply voltages; this amplifier is denoted a very-wide-common-mode-range differential amplifier (VCDA) [2].

The circuit configurations of both amplifiers differ from those of conventional CMOS differential-amplifier configurations in two important ways:

1) the amplifiers are completely complementary, i.e., each n-type device operates in push–pull fashion with a corresponding p-type device;
2) the amplifiers are self-biased through negative feedback.

These two differences in the amplifier configurations result in several performance enhancements:

- less sensitivity of active-region biasing to variations in processing, temperature, and supply;
- capability of supplying switching currents that are significantly greater than the quiescent bias current;
- nominal doubling of differential-mode gain (+6 dB).

These performance enhancements are particularly desirable in comparator applications in commercial digital CMOS VLSI integrated circuits, where precision, high speed, ease of interfacing to ordinary logic gates, and consistently high production yields are required. Both amplifiers have found application in commercial CMOS VLSI integrated circuits as precision comparators, as will be discussed below.

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The author is with Intel Israel, Ltd., 31015 Haifa, Israel.
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II. CSDA

A. Theory of Operation

A self-biased, but noncomplementary, CMOS differential amplifier has been reported [3], as has a fully complementary, but externally biased, CMOS differential amplifier [4].