CMOS Design of Chaotic Oscillators Using State Variables: A Monolithic Chua's Circuit

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***Abstract*—This paper presents design considerations for monolithic implementation of piecewise-linear (PWL) dynamic systems in CMOS technology. Starting from a review of available CMOS circuit primitives and their respective merits and drawbacks, the paper proposes a synthesis approach for PWL dynamic systems, based on *state-variable* methods, and identifies the associated analog operators. The GmC approach, combining quasi-linear VCCS's, PWL VCCS's, and capacitors is then explored regarding the implementation of these operators. CMOS basic building blocks for the realization of the quasi-linear VCCS's and PWL VCCS's are presented and applied to design a Chua's circuit IC. The influence of GmC parasitics on the performance of dynamic PWL systems is illustrated through this example. Measured chaotic attractors from a Chua's circuit prototype are given. The prototype has been fabricated in a 2.4-μm double-poly n-well CMOS technology, and occupies 0.35 mm^2, with a power consumption of 1.6 mW for a $\pm$2.5-V symmetric supply. Measurements show bifurcation toward a double-scroll Chua's attractor by changing a bias current.**

I. Introduction

DURING THE last decade, the possibility to *engineer* electronic *circuits* that display *controllable, deterministic chaos* has drawn research attention (see, e.g., [1], [2]). A primary motive for this interest is the fact that circuits provide the *simplest* vehicles for the *experimental* observation of chaotic phenomena (instead of only through computer simulation), which render them very useful *academic* tools. However, chaotic circuits are more than just academic toys; they are exploitable for industrial applications. For instance, the inherent unpredictability of deterministic chaos has been used to design improved white and colored noise generators [3]–[6], as well as for the generation of *secure random number* time-series [7], [8]. The randomness of chaos has also proved useful to improve the noise performance of switched-capacitor sigma–delta modulators, making these circuits operate in chaotic regime [9], [10]. Chaotic circuits also exhibit potential applications in nonlinear signal processing and neural computation. On one hand, the inherent robustness of chaotic *synchronization* can be exploited for signal *encryption* and *secure* communications [11]–[13]. On the other hand, the fact that chaos has been identified to be behind the sensory information processing performed by natural nervous systems [14], [15], motivates looking for artificial neural network paradigms based upon chaotic neurons, in an attempt to better emulate living beings [16], [17].

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In today's applied electronics, the term "circuits" is mainly synonymous with *microelectronic* circuits. Economic reasons dictate the convenience of having all component parts of electronic systems integrated on common silicon substrates instead of breadboarded by using off-the-shelf components. Monolithic integration becomes a must for applications requiring large-scale circuits, e.g., artificial neural networks. In this scenario, and before the potentials of chaotic circuits can be exploited into future marketable instrumentation, communication, and computing systems, it must first be demonstrated that chaos can be generated in a controllable and robust form by using monolithic circuits, preferably by using *standard* VLSI technologies. This is the basic objective of this paper, which focuses on CMOS technology.

A first step in CMOS chaotic oscillator design is to select a realizable mathematical model. Two different possibilities arise at this level:

1) *discrete-time* systems, described by finite-difference equations (FDE's)
2) *continuous-time* systems, described by ordinary differential equations (ODE's).

FDE-based systems have already been demonstrated in the monolithic CMOS arena, using *switched-capacitors* [4] and *switched-currents* [18]. Although these circuits are very simple and robust, their sampled-data nature restricts the maximum frequency attainable, because of the need to guarantee that the circuit evolve into steady state for each clock interval. This inherent performance limitation, together with functional limitations of FDE-based chaotic systems as compared to ODE-based ones (for instance, to our best knowledge, secure communication has not yet been demonstrated for discrete-time systems), move us to focus on ODE-based chaotic oscillators.

This paper presents a methodology for CMOS design of ODE-based dynamic systems with *piecewise-linear* (PWL) nonlinearities. This methodology is illustrated via the realization of a monolithic version of the Chua's circuit in a 2.4-μ m n-well CMOS technology. The Chua's circuit, whose discrete version is depicted in Fig. 1,[1] is worth considering as a demonstration vehicle for several reasons. First, it is the

[1] The Chua's circuit consists of four *passive* linear elements (one *inductor*, two *capacitors*, and one *resistor*) and one *active* nonlinear element (the Chua's diode) whose global driving-point characteristics are displayed in Fig. 1(b). In these characteristics, the region of interest for chaos generation is the inner one, drawn with solid lines. It has been shown that functions of similar but smoother shape than PWL qualify for chaos generation as well. The outer pieces, drawn with dashed lines in Fig. 1(b), are due to nonidealities in electronic implementations of the Chua's diode [19].

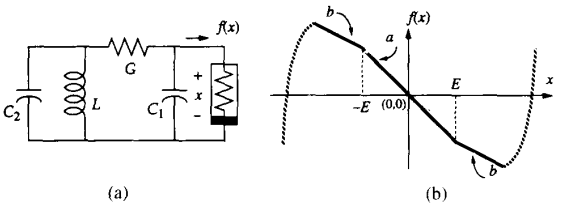


Fig. 1. (a) Chua's circuit. (b) Scaled Chua's diode nonlinearity.

simplest ODE-based chaotic autonomous circuit; it has been extensively studied, and its dynamics are well understood [2]. Besides, its implementation as an IC is challenging because of the lack of monolithic inductors, the large tolerances of monolithic passive and active components, and the large area penalty of IC passive resistors. Last, but not least, the Chua's circuit exhibits interesting features for signal encryption and secure communications [13], as well as reproducing wave propagation phenomena with potential application in image processing [20].

We have intended to write a survey paper, useful for a broad scope of readers. Section II is tailored to the needs of those readers with scarce previous experience in MOS IC design. Based on our conviction that electrical circuit design (in monolithic as well as discrete form) must rely on knowledge of the catalog of available components, this section surveys the basic CMOS passive and active primitives and their respective merits and drawbacks. Section III presents a general architecture to synthesize nonlinear dynamic systems, representing them via a state equation in normal form. We identify the basic analog operators required, survey two basic integrator concepts, and introduce a number of operators for PWL synthesis. Sections IV and V present CMOS circuit blocks for the state variable architecture: linear (Section IV) and nonlinear (Section V). We focus only on GmC circuits, based on transconductors, and cover basic circuit schematics together with a discussion of dominant nonidealities and some more advanced circuit strategies. Finally, Section VI is devoted to present design and measurements from a monolithic Chua's circuit in a 2.4-μm CMOS n-well double-poly double-metal technology.

II. CMOS Primitive Components

Monolithic implementation of the Chua's circuit, and in general of any ODE-based chaotic system, raises design issues similar to those encountered for analog filters or oscillators. One major issue arising is the reduced number of *available* components, much small than those available for discrete design techniques. For instance, the poor quality factor (due to ohmic losses) and large area occupation of IC-compatible *inductors* [23] render this component useless, except for frequencies in the GHz range. Thus, inductors are usually avoided for lower signal frequencies as required for instrumentation, audio, data recovery, and video applications. Likewise, the catalog of available *active* components is limited. Thus, in CMOS technologies, basically, there are only MOSFET's (n-channel and p-channel); other active devices cannot be used for CMOS monolithic realization.[2]

The useful range of component values is also much more reduced for monolithic circuits than for discrete circuits. Monolithic element values are determined by *sizes* and *shapes* of corresponding physical components, so that as a general rule, large element values imply large area occupation and large parasitics. Consequently, the *spreading* of component values into a given circuit must be kept as small as possible to reduce total area occupation and equalize parasitics.

The very poor *absolute* accuracy of integrable components is another important problem confronted by designers. Typical tolerance margins are about 20%, with large influence of temperature and aging, and, in many cases, large nonlinearities. On the contrary, tolerance of ratios between similar components is much smaller (as low as 0.1% [26]), and the same situation is encountered in the influence of temperature, aging, or even nonlinearities.[3] Consequently, monolithic circuit design techniques should rely on component *ratios* (capacitor, resistor, or transistor ratios), instead of on absolute component values, and should try to exploit simple schemes for nonlinearity cancellation. Following this approach, many design problems are reduced to guaranteeing that ratioed components remain *matched* to proper levels in spite of *random* perturbations during the IC fabrication process. This is again strongly dependent on component sizes and shapes—matching increases by increasing component sizes and by making ratioed components have homogeneous shapes [28], [29].

Fig. 2(a) shows a tridimensional view of an n-channel MOSFET, and Fig. 2(b) and (c) shows 2-D sections along (Fig. 2(b)) and across (Fig. 2(c)) the *channel*,[4] respectively. For convenience, Fig. 2(a) includes an NMOST symbol and associated voltages, referring to the substrate, and current. In most common n-well CMOS technologies, NMOS transistors are directly fabricated on the global p-type substrate as shown in Fig. 2, whereas PMOS transistors are made on *local* n-type substrate areas called *wells* that have been created on the global substrate via a local diffusion–implantation process.

Fig. 2 contains two *resistive* layers available in CMOS n-well technologies: *polysilicon* layer and N_+*-diffusion* layer. These layers can be used to take transistor terminal voltages to other points inside an IC, which constitutes a unique feature allowing increased device packing in MOS technologies. Besides, their ohmic losses render them exploitable as isolated devices, to implement *quasi-linear resistors*. Fig. 3(a) shows a top view of a typical passive resistor layout; resistance is directly proportional to the length of the strip and inversely proportional to its width. Other resistive layers available in standard CMOS n-well technology are well-diffusions and

[2] Although floating BJT's can also be implemented in CMOS by using lateral structures [24], [25], they contain large parasitics and are not usually characterized by manufacturers, which renders their use somewhat risky for reliable IC manufacturing.

[3] In analog circuit design, there are many examples of nonlinearity cancellation in a pair of highly nonlinear components, for instance, in a *current mirror* [27].

[4] Conduction in an MOS transistor takes place in the substrate portion comprising the diffused implanted areas, behind the area where thin dioxide is thinner. This portion of *length L* and *width W* is called the *channel* [30], [31].

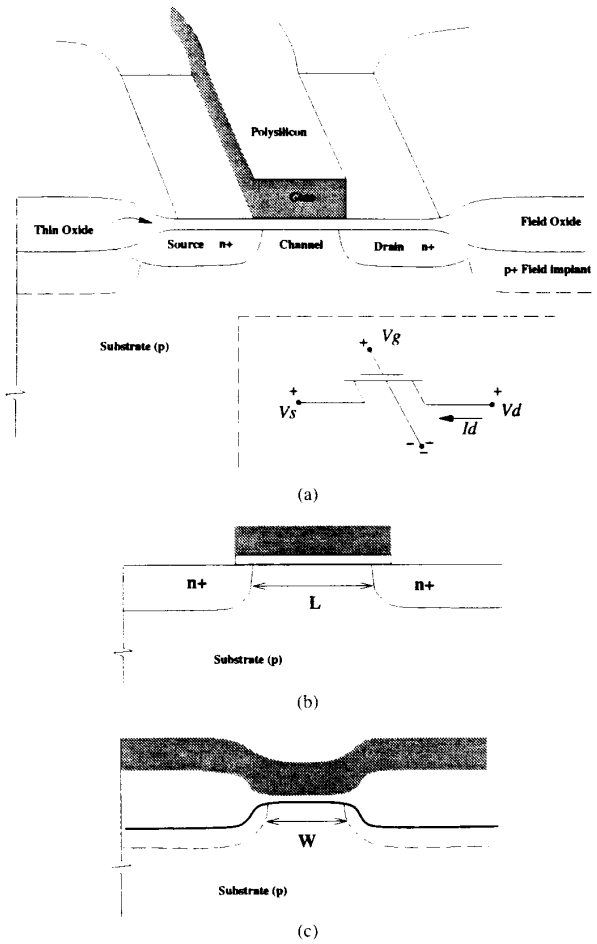


Fig. 2. (a) Three-dimensional view of a n-channel MOSFET. (b) Longitudinal section. (c) Transversal section.

P_+-diffusions. Smallest area occupations are provided by the well-diffusion at the cost of poor relative tolerances ($\sim$ 1–10%), large capacitive coupling to the substrate,[5] and some voltage dependency. On the other hand, the best relative tolerances ($\sim$ 0.1–1%), smallest capacitive parasitics, and largest linearity are provided by polysilicon layer, at the price of large area occupancy ($\sim 10^3$ μm^2 per KΩ, for typical layout in a 2-μm technology). However, in some advanced, analog-oriented technologies, these area figures can be reduced by about two orders of magnitude by using highly doped polysilicon layers.

In standard CMOS technologies, *thick* oxide capacitors can be formed between interconnecting layers (made of Al) and polysilicon layers, but area occupation is very large ($\sim 10^4$ μm^2 per pF), and the structure exhibits some nonlinearities because of lack of homogeneity in the silicon dioxide. Much smaller area occupation ($\sim 10^3$ μm^2 per pF, in a typical 2-μm technology) is possible by exploiting capacitive effects

[5]Since the substrate is ac ground, this coupling slows transient response. Also, substrate noise coupling increases noise in the signal path and degrades circuit performance [32].

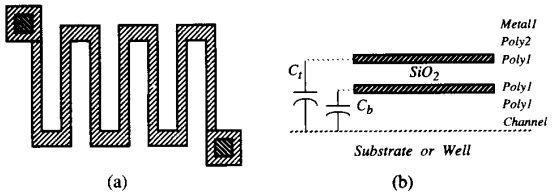


Fig. 3. (a) Typical CMOS resistor layout. (b) CMOS capacitor conceptual section and parasitics.

between gate and channel of an MOS transistor.[6] However, the MOSFET gate terminal must be properly dc biased and the gate voltage must vary only slightly in ac to maintain small nonlinearity [33]. Alternatively, many analog-oriented CMOS technologies provide two polysilicon layers and the possibility to grow a homogeneous thin-oxide between them [26], [34]. These structures display reasonable area figures ($\sim$ 2000 μm^2 per pF in a typical 2-μm technology) and excellent linearity. All CMOS capacitors have good relative accuracy (as low as 0.1%) and exhibit large, and in some cases highly nonlinear, parasitics capacitive coupling to the substrate. These parasitics may amount up to $\sim$ 20% of the nominal capacitor, and are illustrated in Fig. 3(b).

Let us now consider the primary CMOS active component, the MOSFET. It exhibits different operation, depending on current and voltage levels. Best *matching* properties (bear in mind that matching is a major issue for design techniques based upon component ratios) are obtained in *strong inversion* [27]–[29], for large enough values of V_G, where maximum saturated current levels are much larger than βU_t^2, and the current–voltage characteristics follow a *polynomial* law [31].[7] Still, two different regions are distinguished in strong inversion, which are described below by first-order approximative models [27], where, for convenience, we assume $V_D > V_S$ and the current polarity indicated in Fig. 2(a). Because of device symmetry, the other possibility ($V_S > V_D$) is reduced to this by changing current polarity and the role of terminals S and D.

(a) Ohmic Region: For small values of V_D and V_S:

$$I_D \approx k\frac{W}{L}\left[(V_G - V_{To} - nV_S)V_{DS} - \frac{n}{2}V_{DS}^2\right] \tag{1a}$$

valid for

$$V_G > V_{To} + nV_S \qquad V_{DS} < V_{DS\,\mathrm{sat}} \equiv \frac{V_G - V_{To}}{n} - V_S \tag{1b}$$

where V_{To} is a technological parameter (threshold voltage for zero substrate bias, $V_S = 0$) and n depends slightly on V_S and ranges typically from 1.2 to 1.5.

[6]The channel of a MOSFET accumulates charge when a voltage difference is created between gate and substrate—a capacitive effect. This voltage must be positive for NMOS and negative for PMOS. In any case, for a large enough drop, though under typical IC biasing conditions, charge accumulation is exponential so that the channel resembles a low-resistivity conducting layer, and, hence, the polyoxide-channel structure behaves as a linear capacitor [30], [31].

[7]$\beta = kW/L$ where k is a technological parameter, $\sim$ 50 $\mu A/V^2$, and $U_t = KT/q$ is the thermal voltage; W and L are the channel width and length, respectively.

(b) Saturation Region: For small values of V_S and large values of V_D:

$$I_D \approx \frac{k}{2n}\frac{W}{L}[V_G - V_{To} - nV_S]^2 \tag{2}$$

valid for $V_{DS} > V_{DS\,\mathrm{sat}}$ under the constraint of V_G given in (1b).

Both operating regions (as well as those obtained in *weak inversion* [27], for $I_D \ll \beta U_t^2$) are exploited for circuit design. First, consider the ohmic region and assume that nonlinear terms may be neglected. In this case, the MOSFET emulates a linear resistor. Interestingly enough, this *active* resistor has much smaller area occupation than passive polysilicon resistors, and its resistance can be adjusted by geometry and V_G. For instance, in a typical practical situation where $V_G - V_{To} - nV_S = 1$ V with $W/L = 1$, we get $R \sim 20\ k\Omega$, with an area occupation that can be as small as $\sim 10\ \mu\mathrm{m}^2$. Obviously, this usage as a linear resistor is valid only providing that either V_{DS} is small enough and/or some nonlinearity cancellation technique is used [35].

Now, consider the saturation region, and assume that (2) is expanded in a Taylor series around a bias point $I_D = I_Q$, $V_G = V_{GQ}$, for $V_S = 0$

$$\Delta I_D = g_m\,\Delta V_G + b_2\,\Delta V_G^2 \tag{3}$$

where $g_m = 2I_Q/(V_{GQ} - V_{To} - nV_S) = (2kWI_Q/Ln)^{1/2}$—electrically and geometrically adjustable. Assuming, as for the ohmic region, that the nonlinear term can be neglected, the MOSFET emulates a linear VCCS with adjustable transconductance: a fully exploitable primitive for analog circuit design. Since design techniques presented in this paper primarily exploit this MOSFET capability, it is convenient to identify dominant parasitics that degrade performance of emulated VCCS.[8]

First of all, performance is degraded because of *nonlinearities*, represented by the quadratic term in (3), as well as by dependence of parameter k on terminal voltages [36]. We will postpone discussing nonlinearities until Section 4.1. Two major linear parasitics can be identified: finite *output resistance* and limited *bandwidth*. The finite output resistance models change in output current because of changes in V_{DS}, $\Delta I_D = R_o\,\Delta V_D$, and can be represented via an equivalent *Early voltage*, V_A, so that $R_o = V_A/I_Q$. Early voltage value increases with channel length, being ~ 50 V for $L = 10\ \mu$m in typical 2-μm technologies. With respect to frequency response, limitations are due to parasitic capacitances; in particular, the input capacitance and feedforward capacitance between input and output terminals [37], [42]. A hybrid-π model representing most significant linear parasitics is shown in Fig. 4, with typical capacitance values for a 2-μm technology. A useful figure of merit to quantify MOSFET frequency limitations is the *transition frequency* [42], f_T, the frequency at which the magnitude of the transistor current gain with short circuit load

[8] Some CMOS analog design techniques exploit MOSFET transconductance in the ohmic region. They are based on biasing the transistor to keep V_D and V_S fixed under small signal excitation. Thus, a quasi-linear relationship is achieved between I_D and V_G, and, hence, a VCCS is implemented [68].

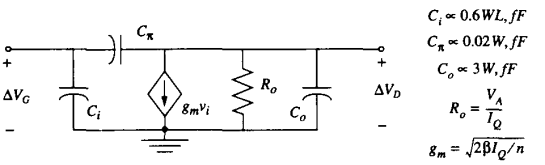


Fig. 4. Small-signal hybrid-π MOSFET model. (Capacitor values are typical for a 2 μm technology; all dimensions are in μms).

drops to zero

$$2\pi f_T \propto \frac{g_m}{0.6WL} \tag{4a}$$

where we have neglected C_π as compared to C_i. Taking into account the g_m dependency on bias, we calculate

$$2\pi f_T \propto \frac{k}{n}\frac{V_{GQ} - V_{To}}{0.6L^2}. \tag{4b}$$

This shows that the transition frequency increases with decreasing channel length and, consequently, as technology evolves towards smaller feature sizes. It also shows that the transition frequency is an increasing function of $(V_{GQ} - V_{To})$ and, consequently, I_Q. For typical 3-μm 5 V CMOS technologies and assuming an upper-limit practical bias of $(V_{GQ} - V_{To}) = 2.25$ V, the transition frequency is about 1 GHz.

Summarizing, design in CMOS standard VLSI technologies, for controlled sources as well as for passive element emulation, should preferably rely only on MOSFETS. For technologies including a second poly layer, Poly-SiO_2-Poly capacitors are a better choice for increased linearity; the same occurs regarding the use of poly layers as resistors. Whichever structure is used, designers should confront the issues of reduced component spread, large absolute tolerances, and layout-dependent matching properties for component ratios. A more detailed account of CMOS component matching and scaling properties is available in [26], [28], [29], [34], [38]–[41].

III. A State Variable Architecture for PWL Dynamic System Synthesis

Let us consider CMOS design of the Chua's circuit. A direct technique is active *element emulation*, using a VCCS-based gyrator for the inductor, and any MOSFET-based resistor configuration. A more systematic approach, valid for general PWL dynamic systems, whether associated with a *RLC* circuit structure or not, is to use a *state-variable* technique, focusing on the implementation of the system state equations. Consider, for instance, the system of equations representing dynamics of the Chua's circuit [21]:

$$\begin{aligned}\tau_x\frac{dx}{dt} &= \alpha[y - x - f(x)]\\ \tau_y\frac{dy}{dt} &= x - y + z\\ \tau_z\frac{dz}{dt} &= -\beta y\end{aligned} \tag{5a}$$

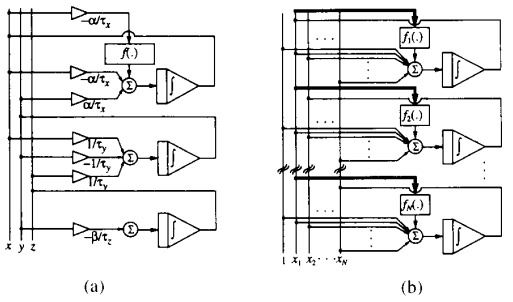


Fig. 5. (a) Conceptual state-variable block diagram of the Chua's circuit. (b) Conceptual state-variable block diagram of PWL dynamic systems. (Scaling blocks have been suppressed in this latter diagram for clarity.)

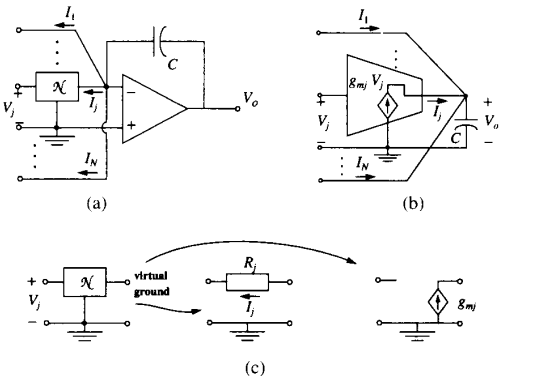


Fig. 6. (a) Generalized Miller integrator concept. (b) Open-loop integrator concept. (c) Realization of the black box $\mathcal{N}$.

where $f(x)$ is given by

$$f(x) = bx + \frac{a-b}{2}\{|x+E| - |x-E|\} \tag{5b}$$

and τ_x, τ_y, τ_z, α, β, a, b, and E are real parameters. These equations can be mapped on the conceptual state-variable block diagram of Fig. 5(a). Similarly, a general system with an N-dimensional state vector $\boldsymbol{x} = (x_1, x_2, \cdots, x_N)^T$ and dynamics given by a set of first-order state equations

$$\tau_i \frac{dx_i}{dt} = p_{i0} + \sum_{j=1}^{N} p_{ij}x_j + f_i(x, r). \qquad 1 \le i \le N \tag{6}$$

where $\{\tau_1, \tau_2, \cdots, \tau_N\}$, $\boldsymbol{p}$ and $\boldsymbol{r}$ are vectors of real parameters, can be mapped on the block diagram of Fig. 5(b).

The state-variable approach is similar to that followed in classical *analog computation* [43] and reduces implementation of PWL dynamic systems to the realization of a number of mathematical operations: *integration, summation, signal scaling*, and *rectification*. However, compared to circuit strategies used in these classical analog computers where operators are built around operational amplifiers in voltage mode [44], proper usage of CMOS primitives gives circuits where both voltage and current play a role, thus yielding much more compact realizations.

3.1. Integrator Concepts

Integrators are key components of the state variable approach. There is no unique, generally accepted manner to realize integrators using CMOS primitives. Fig. 6 shows two basic CMOS integrator concepts; *Miller* integrator (Fig. 6(a)) and *open-loop* integrator (Fig. 6(b)). Both concepts are based on driving a capacitor via voltage-controlled currents. Note that this enables concurrent implementation of the *summation* operator, exploiting KCL

$$V_o(t) = \frac{1}{C}\int_0^t \left[\sum_{j=1}^{N} I_j(\xi)\right] d\xi + V_o(0). \tag{7}$$

For both integrator concepts, the *scaling* operator is implemented through the voltage-to-current transformation used to drive the capacitor. In the case of Fig. 6(b), also known in literature as GmC or OTA-C integrator [45], this transformation is made through a VCCS. On the other hand, for Fig. 6(a), two different approaches can be considered for implementation of the voltage-to-current transformation performed by the box labeled $\mathcal{N}$. Fig. 6(c) illustrates both alternatives.

The first alternative in Fig. 6(c) uses a resistor, so that the scaling factor is the inverse of the associated resistance, $|I_j| = R_j^{-1}V_j$. Two possibilities still arise, depending on whether this resistor is passive or active. For technologies where a low-resistivity layer (like hypodopped polysilicon) is available, passive resistors provide good linearity with no excessive area penalty. For standard technologies, active resistors require much less area occupation at the cost of larger nonlinearity. An extended approach to implement active resistors is to use the ohmic region of a MOSFET, which defines the so-called MOSFET-C analog CMOS design technique [46]. As compared to passive resistors, whose resistance is determined only by geometry, in the MOSFET-C approach, integrator scaling factors are also determined by biasing:

$$R_j = \frac{L}{kW(V_G - V_{To} - nV_S)} \tag{8}$$

and consequently can be electrically trimmed. The second alternative for Miller integrators is to substitute $\mathcal{N}$ in Fig. 6(a) with a VCCS, so that scaling is made through transconductances, as is true for the open loop integrator.

To compare both integrator concepts on an unified basis, we limit ourselves to considering the case where $\mathcal{N}$ of Fig. 6(a) is realized by using a VCCS. For convenience, Fig. 7(a) and 7(b) again depict the two GmC integrator concepts to be discussed. Most of the conclusions to be obtained for Fig. 7(a) apply to the case where $\mathcal{N}$ is a resistor as well.

Ideally, Fig. 7(a) and (b) are *lossless* integrators with identical time constants

$$\tau = \frac{C}{g_m} \tag{9}$$

where g_m (the *transconductance gain*) is determined in the more general case by MOSFET geometry and biasing. For instance, if the VCCS is implemented by a single transistor $g_m = (2\beta I_Q/n)^{1/2}$. See footnote 7 for definition of β.

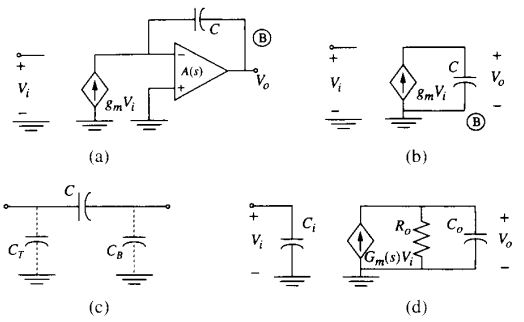


Fig. 7. GmC integrator concepts and parasitics. (a) Miller integrator. (b) Open-loop integrator. (c) Capacitor parasitics. (d) VCCS macromodel.

However, both integrators handle parasitics quite differently. First, consider parasitics associated with the capacitor, consisting of two additional capacitors (bottom plate and top plate), as depicted in Fig. 7(c). Note that one of the capacitor terminals at each integrator schematic is connected to a *low-impedance* point (a point where voltage changes only slightly for large current ranges). Consequently, they can both be made insensitive to C_B, connecting the capacitor bottom plate to the corresponding low-impedance point. On the contrary, the open-loop integrator of Fig. 7(b) cannot be made insensitive to the top plate parasitics, C_T, while its influence is attenuated by a factor A_0 (A_0 is the opamp dc gain) for Fig. 7(a), due to the *Miller* effect. Hence, the Miller integrator exhibits superior performance regarding the influence of CMOS capacitor parasitics.

Now consider the VCCS macromodel of Fig. 7(d), representing some more significant small-signal parasitics that degrade performance of CMOS transconductors, from dc up to tens of MHz [47]; namely, output resistance (R_o), terminal capacitances (C_i, C_o), and limited transconductance-gain bandwidth,[9] represented by:

$$G_m(s) = \frac{g_m}{1 + \frac{s}{\omega_g}}. \tag{10}$$

Further assume that the opamp of Fig. 7(a) is a low-output impedance, internally compensated device whose open-loop gain can be properly modeled by a single pole model [44]:

$$A(s) = \frac{A_0\omega_a}{s + \omega_a} \equiv \frac{\omega_{oa}}{s + \omega_a}. \tag{11}$$

Assuming that the poles of Fig. 7(a) are separate enough and that $\omega_{oa} \gg G_o/C$, the following general expression for the integrator transfer function can be obtained:

$$\frac{V_o(s)}{V_i(s)} = \frac{\mp 1}{s\tau\epsilon_\tau} T_\epsilon(s) \equiv \frac{\mp 1}{s\tau\epsilon_\tau} \frac{\frac{s}{p_1}}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)\left(1 + \frac{s}{p_3}\right)} \tag{12}$$

where the minus sign applies for Fig. 7(a), and ϵ_τ, p_1, p_2, and p_3 are given in Table I for each integrator structure. We

[9]This model is oversimplified. A higher-frequency model includes more poles inside $G_m(s)$ and a frequency-dependent input capacitor.

TABLE I
TIME CONSTANT ERROR AND PARASITIC POLES FOR GMC INTEGRATORS

Integrator	ϵ_τ	p_1	p_2	p_3
Open-loop	$1 + \frac{C_o + C_T}{C}$	$\frac{G_o}{C + C_o + C_T}$	ω_g	
Miller	$1 + \frac{G_o}{G\omega_{oa}} + \frac{C + C_o + C_T}{CA_0}$	$< \frac{G_o}{CA_0}$	ω_g	$\frac{\omega_{oa}C}{C + C_o + C_T}$

see that each structure displays magnitude and phase errors as compared to the ideal integrator transfer function for both low ($\omega < p_1$) and high frequencies ($\omega > (p_2, p_3)$). In addition, both structures exhibit magnitude errors in the pass-band for $p_1 \ll \omega \ll (p_2, p_3)$, which can be assimilated to deviations in the equivalent integrator time constant, via parameter ϵ_τ. However, note that these latter errors are smaller by a factor around A_0 for the Miller structure—a positive consequence of feedback. Similarly, low-frequency error, or, equivalently, losses, are also much smaller for the Miller structure; losses are proportional to the VCCS output resistance (R_o) for the open-loop integrator, while they are attenuated by $\sim A_0$ for the other. On the contrary, high-frequency errors are larger for the Miller integrator. The open-loop integrator has only a high-frequency pole, at ω_g, while the Miller integrator has two, at ω_g and $p_3 = \omega_{oa}C/(C + C_o + C_T)$. Also, as a consequence of the internal compensation used for the opamp, and assuming that the opamp and the VCCS are optimized, it is likely that $\omega_g \gg \omega_{oa}$, inferring poorer frequency response for the Miller integrator than for the open-loop integrator.

Summarizing, previous analysis shows that the open-loop integrator is preferable for high-frequency applications, though requiring *predistortion* to compensate for time constant errors. On the contrary, the Miller integrator is more appropriate for low- and medium-frequency ranges, requiring no predistortion. However, note that degradation of frequency response in the Miller structure is mainly a consequence of using internally compensated, general purpose opamps. High-frequency advantages of the open-loop structure are not so evident if simpler, custom opamps without internal compensation are used [48]. In addition, frequency response of Miller structure may perhaps be enhanced by ingenious exploitation of *active compensation* techniques [49] to properly shape the integrator high-frequency response, and thus combine the features of accuracy, small losses, and large-frequency bandwidth in a single structure.

3.2. On the Synthesis of PWL Functions

Besides weighted summators/integrators, the other building block for the state variable synthesis architecture is PWL function generation. A very convenient approach to synthesize PWL characteristics is to *decompose* them into a summation of simpler functions, preferably exploiting intrinsic MOSFET nonlinearities. For instance, Fig. 8 shows suitable decomposition for the Chua's diode nonlinearity, which enables implementing this element by exploiting saturation characteristics of an actual MOSFET VCCS, as shown in Section V and as used for the monolithic Chua's circuit prototype presented in Section VI. Circuit strategies are discussed in further detail

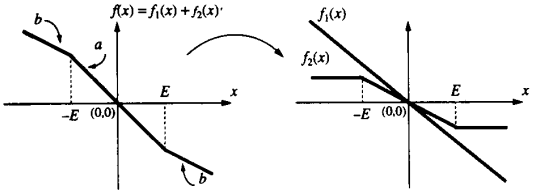


Fig. 8. Chua's diode decomposition.

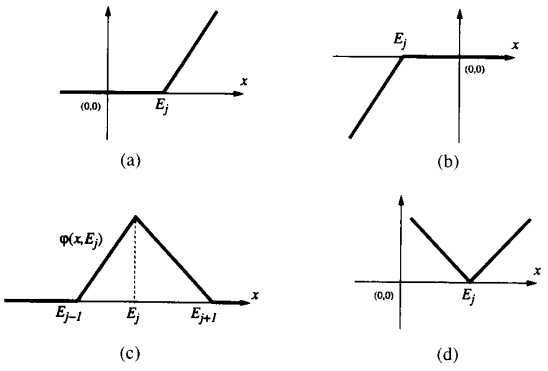


Fig. 9. Elementary functions for PWL synthesis. (a) Concave function. (b) Convex function. (c) PWL radial basis function. (d) Absolute value function.

in Section V. Here we present systematic approaches for PWL function decomposition and identify a number of elementary functions supporting PWL function synthesis.

Let us first consider *undimensional* functions. A first methodology relates to the *extension* operator concept [54, 55], based on the following expression:

$$f(x) = Ax + B + \sum_{j=1}^{N} M_j u_p(x - E_j) + \sum_{j=-N_n}^{-1} M_j u_n(x - E_j) \quad (13a)$$

where the functions $u_p(\cdot)$ and $u_n(\cdot)$ are defined as

$$u_p(x - E_j) = \begin{cases} (x - E_j), & x > E_j \\ 0, & \text{otherwise} \end{cases}$$

$$u_n(x - E_j) = \begin{cases} 0, & x > E_j \\ (x - E_j), & \text{otherwise} \end{cases} \quad (13b)$$

depicted in Fig. 9(a) and (b), and where parameters E_j represent breakpoints, and parameters A, B, and M_j can be easily calculated from the original function by inspection.

Another systematic decomposition technique for PWL functions uses *radial base* functions [56]

$$f(x) = \sum_{j=1}^{N-1} f(E_j)\varphi(x, E_j) \quad (14)$$

where $f(E_j)$ denotes the function value (interpolation data) at breakpoint E_j, and the base functions $\varphi(x, E_j)$ have the generic shape represented in Fig. 9(c), which involves two adjacent intervals of the PWL function domain partition.

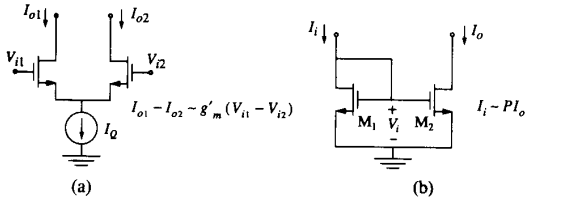


Fig. 10. Basic GmC quasi-linear building blocks. (a) Differential pair. (b) Current mirror.

Unlike the extension operator technique, decomposition by base functions is unique and hence more systematic. In addition, since each interpolation data, $f(E_j)$, influences only one term in (14), it is more appealing for programmable implementations over predefined partitions (E_j fixed).

Consider now *multidimensional* PWL functions. Assume the global PWL multidimensional *canonical* representation introduced by Kang and Chua [57] to alleviate the mass storage problem of conventional PWL representations:

$$f_i(x) = A^T x + B + \sum_{j=1}^{N} C_j |D_j^T x - E_j|, \qquad 1 \le i \le N. \quad (15)$$

According to (15), multidimensional PWL function synthesis requires only *absolute value* operators, depicted in Fig. 9(d).

IV. CMOS GmC Linear Building Blocks

Integrator outputs in the state variable architecture are in the form of voltages. We must be able to transform these voltages into currents, weigh these currents, and root them to different nodes into the architecture. These operations require implementing VCCS's and CCCS's. Fig. 10 shows elementary CMOS blocks to implement them; respectively, *differential amplifier* (Fig. 10(a)) and *current mirror* (Fig. 10(b)) [50]–[52]. The function performed by these blocks is displayed along with these figures and discussed in further detail in Section 4.1.

4.1. The Differential Amplifier

Assume that both transistors in Fig. 10(a) are identical, perfectly matched, and operating in a strong-inversion saturation region. Analysis using the square-law model of (2) yields the following *global* voltage-to-current characteristics:

$$I_{o1} - I_{o2} \approx \begin{cases} g_m V_i - \gamma V_i^3 + o(\cdot), & \text{for } |V_i| \le F \\ I_Q \operatorname{sgn}(V_i), & \text{otherwise} \end{cases} \quad (16a)$$

where $V_i \equiv V_{i1} - V_{i2}$, $I_o \equiv I_{o1} - I_{o2}$; the top expression is a Taylor expansion around $V_i = 0$; and

$$g_m = \sqrt{\frac{k}{n}\frac{W}{L} I_Q}; \quad \gamma = \frac{1}{8\sqrt{I_Q}} \left(\frac{k}{n}\frac{W}{L}\right)^{1.5}; \quad F = \sqrt{\frac{2n}{k}\frac{L}{W} I_Q} \quad (16b)$$

Fig. 11(a) shows a first-order approximation to (16a), for $\gamma = o(\cdot) = 0$. Note that the transconductance gain of this model, g_m' is different from g_m in (16)—a consequence of the fact that $I_Q \neq g_m F$. However, this representation is a graphic

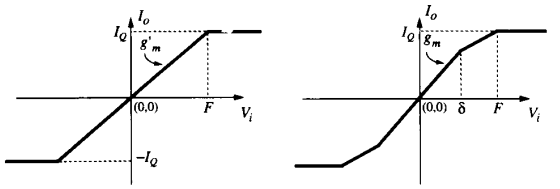


Fig. 11. PWL approximations to differential transconductance amplifier characteristics. (a) First-order approximation. (b) Second-order approximation.

display of the behavior of Fig. 10(a) as a *quasi-linear* VCCS, showing saturation characteristics centered around the origin, and no *offset* component. This latter feature is an appealing consequence of symmetry, which yields offset cancellation[10] —impossible to achieve with the simplest single-MOSFET VCCS (see (3)).

In practice, the $o(\cdot)$ terms in (16a) are negligible, meaning that deviations from the linear behavior are dominated by an *odd* nonlinearity, and consequently, neither even-order harmonics nor dynamic offset term will appear under ac excitation. It is illustrative to compare nonlinearities of the differential amplifier with those of a single MOSFET in case both operate as a VCCS. Note first that nonlinearity of the single transistor VCCS is *even* (see (3)), an important drawback as compared to the differential amplifier VCCS. Further comparison between both VCCS's requires calculating the maximum incremental input voltage under which deviation from linearity remains below a specific boundary

$$\epsilon \geq \left| \frac{\Delta I_o - g_m \Delta V_i}{g_m \Delta V_i} \right|, \qquad \text{for } |\Delta V_i| \leq \delta \tag{17a}$$

where ΔI_o and ΔV_i denote increments around the quiescent point (for differential amplifier $I_{oQ} = V_{iQ} = 0$). Analysis gives the following:

$$\delta = \begin{cases} 2\epsilon F & \text{for unilateral amplifier} \\ 2\sqrt{\epsilon} F & \text{for differential amplifier} \end{cases} \tag{17b}$$

where F is given in (16b). Since, for small linearity deviations, it must be $\epsilon \ll 1$, (17b) shows that linear range is much larger for the differential than for the single-MOSFET VCCS. For instance, the improvement is about one order of magnitude if maximum allowed deviation is 1%—a very common specification for GmC circuits.

Fig. 11(b) shows a second-order PWL model for the differential pair transfer characteristics. This model displays a quasi-linear interval, for $|V_i| \leq \delta$, and two transition regions towards saturation, for $\delta < |V_i| \leq F$. Interestingly enough, (16b) and (17b) show that the quasi-linear interval amplitude, δ, and the transconductance gain, g_m, can be separately controlled by geometry (W/L) and biasing (I_Q); all designs fulfilling that $I_Q W/L$ remains constant have equal transconductance gain, while their linearity range can be increased by increasing I_Q or by decreasing W/L. However, this increases $V_{DS\,\mathrm{sat}}$ (see (1b)) of the transistors at the quiescent point and careful design is needed to guarantee that transistors do not enter the ohmic region.

Together with issues related to transconductance gain and linearity ranges, differential amplifier design must confront *mismatches* and ac parasitics as well. Mismatches are mainly due to statistical variations of parameters k and V_{To} for both transistors in the differential pair. These variations appear even though both transistors are laid out with identical shape and orientation, and these increase proportionally with the distance between the physical devices and inversely to the channel are (WL) [28], [29].

A major consequence of mismatch is that circuit symmetry is destroyed, and consequently an offset term appears:

$$E_{os} = \Delta V_{To} - \sqrt{\frac{nLI_Q}{2kW}} \frac{\Delta k}{k} \tag{18}$$

where ΔV_{To} and $\Delta k/k$ denote threshold and transconductance mismatch. There is no way to attenuate the influence of threshold voltage mismatch by design; it can be reduced only by *layout*, using large area devices with minimum distance between them. On the contrary, the influence of k-mismatch can also be reduced by design, by making $I_Q L/W$ decrease. However, this compromises linearity and, consequently, forces the solution of design tradeoffs.

Regarding ac parasitics of the differential pair, the most dominant ones are represented in the model of Fig. 12(a), where we have implicitly assumed that the differential amplifier is symmetrically loaded via two identical frequency-dependent admittances $Y_L(s)$. Frequency-dependent transconductance and input admittance of this model are respectively given by the following equation:

$$\begin{aligned} G_m(s) &= g_m\left(1 - \frac{s}{z}\right) \\ Y_i(s) &= sC_\pi \frac{G_m(s) R_o}{1 + sR_oC_o + R_oY_L(s)} \end{aligned} \tag{19}$$

with C_π, C_o, and R_o being approximately as given in Fig. 4 and $z = g_m/C_\pi$. Two conclusions can be reached from previous equations: 1) Input impedance and frequency-dependence of the transconductance gain are determined by the transistor feedforward capacitor, C_π. Since C_π is proportional to W of the transistor, both parasitics are decreased by decreasing W. 2) The influence of C_π on the input admittance is largely amplified by the Miller effect, resulting in increased net input capacitance for low frequencies as well as dependence of the equivalent input capacitance on frequency. The loading effects of this large, frequency-dependent capacitance on the stages driving the differential amplifier introduce errors in GmC integrator operation and hence are important in proper design considerations.

4.2. The Current Mirror

Obtaining the left-hand side of (16a) requires that current I_{o2} be *weighted* with factor -1 and rooted to the same node as I_{o1}; thus, addition is achieved by KCL. The weighting and routing of individual current components is common practice in GmC systems, making it necessary to implement CCCSs. This is the basic function performed by Fig. 10(b).

[10]However, practical realization of this structure may exhibit offset due to random transistor mismatches [28], [29].

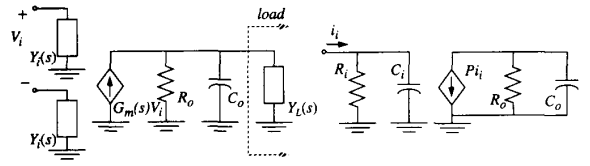


Fig. 12. (a) ac differential amplifier macromodel. (b) ac current mirror macromodel.

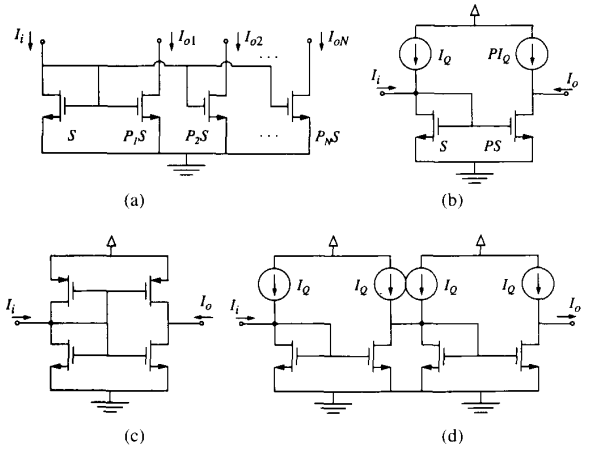


Fig. 13. Current mirror applications. (a) Scaled replication. (b) Bilateral signal weighting by bias shifting. (c) Bilateral signal weighting by complementary devices. (d) Current reversing.

Operation of the current mirror relies on *functional* nonlinearity cancellation between input and output transistors M_1 and M_2. Assume that these devices have different geometry factors, are matched (in the sense of having identical technological parameters, k, n, and V_{To}),[11] and that input and output terminals are equipotential. Then it can be seen that nonlinearity in the output transformation $I_o = f(V_i)$ cancels out that arising in the input transformation, $V_i = f^{-1}(I_i)$, thus yielding a linear, linearly scaled $I_o - I_i$ relationship:

$$I_o = S_2 f(V_i) = S_2 f\left[f^{-1}\left(\frac{I_i}{S_1}\right)\right] = \frac{S_2}{S_1} I_i = PI_i \qquad (20)$$

where $S_j \equiv (W/L)_j$, $j = 1, 2$. The basic mirror concept is easily extended to multiple current outputs, as Fig. 13(a) illustrates. Since fanout of a current source is strictly unity, this *replication* capability is needed to allow several nodes be excited by a common current. On the other hand, the fact that the different current output replicas can be scaled independently provides extra adjusting capability for GmC state variable design.

Figs. 10(b) and 13(a) operate properly only for positive input currents. Negative currents flowing into the input terminal of the mirror, $I_i < 0$, drive the input voltage, V_i, below the MOS threshold voltage V_{To}, and, hence, the input and output devices are cut off, yielding zero output current. Because of this inherent rectification, the scaled replication implemented by Fig. 13(a) is unilateral. For bilateral operation, current-shifted biasing at the input and output nodes or p-channel MOSFETs must be used, as shown in Fig. 13(b) and 13(c). On the other hand, note that bilateral current amplifiers of Fig. 13(b) and 13(c) are the *inverting* type (direction flow for output current differs from that for input current): Only negative scale factors are implemented. *Noninverting* amplification (i.e., positive scale factors) are achieved by cascading two bilateral mirrors, as shown in Fig. 13(d).

Current mirror behavior is degraded by random and systematic error sources. Systematic errors are mainly due to finite transistor Early voltages [62]. On one hand, this produces current offset in case mirror input and output terminals are not equipotential—a dc problem whose solution requires proper biasing. On the other hand, finite Early voltages cause the mirror output resistance not to be infinite as expected for an ideal current source. Another source of systematic ac current mirror errors is finite input resistance. Fig. 12(b) depicts an approximate ac model for current mirrors, including input and output resistances and capacitances whose approximate values for Fig. 10(b) are given by the following:

$$R_o \approx \frac{V_A}{I_o}; \qquad R_i \approx \sqrt{\frac{n}{2kS_1 I_i}}$$

$$C_i \propto 0.6(W_1 L_1 + W_2 L_2); \qquad C_o \propto 3W_2 \qquad (21)$$

where V_A is the transistor Early voltage and $S_1 = W_1/L_1$. Since V_A increases with channel length, the mirror output and input resistances can both be improved by adjusting transistor sizes, though compromising mirror area and, consequently, parasitic capacitances.

As for differential amplifiers, random transistor mismatches also degrade current mirror operation, causing errors in the current gain. For unity-gain mirror, this current gain error is given by the following equation:

$$\frac{\Delta I_o}{I_o} = \frac{\Delta k}{k} - \sqrt{\frac{2kW}{nLI_o}}\,\Delta V_{To} \qquad (22)$$

from which we can infer approaches for reduction.

4.3. Advanced Linear Building Blocks and Circuit Strategies

Transistor dimensioning itself does not guarantee optimum values for all specifications involved in the design of the elementary circuit structures of Fig. 10. For instance, linearity of the differential amplifier can be enhanced by increasing L/W, but this deteriorates transconductance gain and random offset. Similarly, output resistance of Fig. 10(b) can be increased by increasing L, thus making the input resistance increase as well and deteriorating mirror reactive behavior. This section reviews most common circuit strategies to increase linearity of differential pairs and to enhance input and output resistance of current mirrors. We present as well some common mirror-to-amplifier interconnection strategies to obtain VCCS's with unilateral output current.

[11] For better matching, both devices should have equal channel length and should be split into a parallel connection of several devices of identical size and shape.

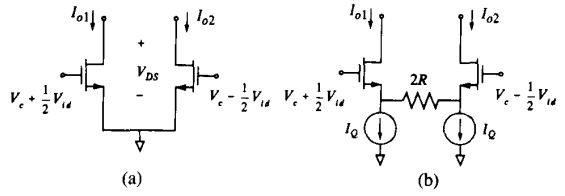


Fig. 14. (a) Concept of linearized ohmic transconductors. (b) Concept of degenerated differential pair.

4.3.1) On Linearization Techniques for Differential Amplifiers: Linearization of CMOS differential transconductor characteristics has drawn strong attention in analog circuit design literature [51]–[53], [65]–[76]. The basic objective is to obtain circuit structures whose linearity range is, by construction, larger than that obtained for the simple differential amplifier of Fig. 10(a). Following the classification scheme in [66], three major approaches can be identified:

1) Ohmic transconductors [68]–[71]
2) degenerated differential pairs [72], [73]
3) square-law transconductors [74]–[77].

Ohmic transconductors exploit MOSFET operation in ohmic region and are well suited for high-frequency operation. Fig. 14(a) illustrates the principle. Assuming that both transistors are perfectly matched and that $V_{DS1} = V_{DS2} \equiv V_{DS} < V_{DS\,\mathrm{sat}}$ (see (1)), it follows that

$$I_{o1} - I_{o2} = \left(k\frac{W}{L}V_{DS}\right)V_{id} \tag{23}$$

perfectly linear voltage-to-current transfer characteristics whose transconductance gain can be electrically trimmed via V_{DS}. Actual implementation of this concept differs in the approach used to maintain drain terminals equipotential, independent of the differential input voltage. A major source of nonlinearity for all of them is due to dependence of parameter k on terminal voltages [36].

Fig. 14(b) illustrates the principle of degenerated differential pairs, which achieve large linearity at the cost of large area occupation and small transconductance gain values. The circuit exploits feedback to maintain V_{GS} of the transistors practically constant for large differential input voltage variations. Proper operation requires that sufficiently large feedback is applied, which infers fulfilling $g'_m R \gg 1$, where g'_m denotes the transistor transconductance gain. Consequently, it obtains the following:

$$I_{o1} - I_{o2} = \frac{g_m}{1 - g'_m R}V_{id} \approx R^{-1}V_{id} \tag{24}$$

which shows that the external transconductance gain is determined by the feedback resistor. An excellent comparative review of different degenerated differential pair implementations can be found in [73].

The last group of linearized transconductors include structures that obtain linear operation by algebraic combination of square-law functions, for instance, the following:

$$(a+b)^2 - (a-b)^2 = 4ab. \tag{25}$$

These structures hence exploit transfer characteristics of MOSFETs operating in strong inversion inside saturation. A great number of structures that follow this general principle have been reported in literature [65], [67], [74–77]. Fig. 15 shows examples of some of them. As for ohmic region transconductors, a main limitation of these structures is the dependence of parameter k on terminal voltages [36], which produces deviation from the ideal square-law operation.

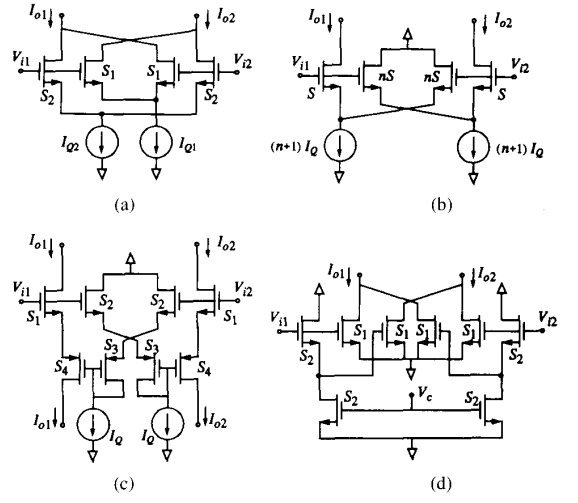


Fig. 15. Illustrative square-law MOS transconductors. (a) Cross-coupling [74]. (b) Adaptive biasing [75]. (c) Class AB [76]. (d) Voltage shifting [77].

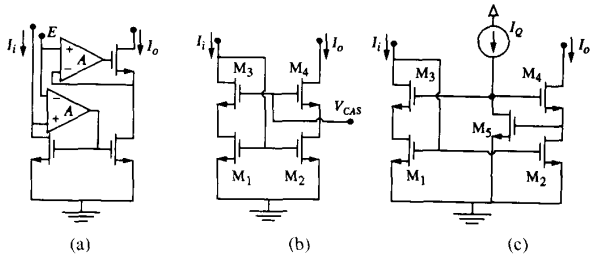


Fig. 16. Improved current mirrors. (a) Active. (b) Cascode. (c) Regulated cascoded.

4.3.2) Improved MOS Current Mirrors: Fig. 16 shows three improved mirror structures. Fig. 16(a) employs feedback to keep input and output equipotential, thus reducing DC errors in the mirror operation [63]. Furthermore, since feedback causes the input and output voltages to remain practically fixed, the mirror input and output resistances improve proportionally to the amount of feedback applied. Fig. 16(b) and 16(c) display alternative improved current mirror structures using cascode transistors. They are aimed to keep drain voltage of transistor M_2 fixed, thus increasing R_o. In Fig. 16(b), it is achieved through the cascode transistor M_4, exploiting the fact that its source voltage follows the cascode biasing voltage V_{CAS}. For Fig. 16(c), the cascode action is further reinforced by feedback [64]. Any of the mirror structures in Fig. 16 enables increasing R_o/R_i several orders of magnitude as compared to the simple mirror of Fig. 10(b), and requiring no large channel areas.

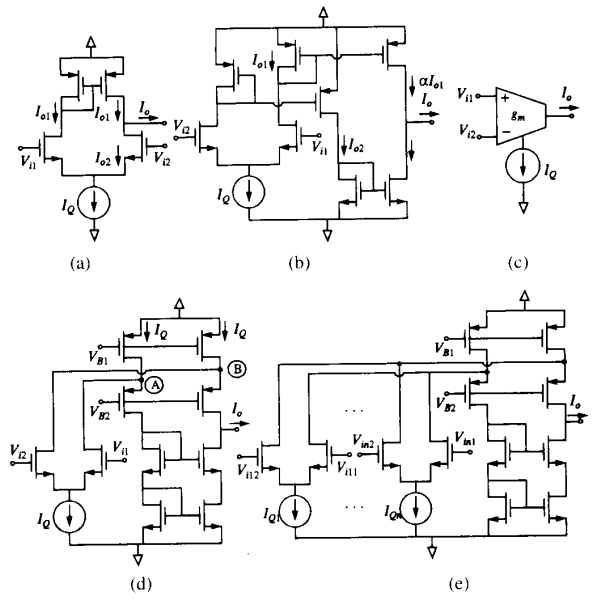


Fig. 17. (a) Simple transconductance amplifier. (b) Symmetric load transconductance amplifier. (c) Symbol. (d) Folded cascode structure. (e) Multiple inputs transconductance amplifier.

4.4. Circuit Strategies for Unilateral Output Transconductors

For Fig. 10(a), as for most linearized transconductor structures, the linearized output variable is obtained as a difference of two currents. There are many ways to connect a differential transconductor and current mirrors to obtain the difference of amplifier output currents rooted to a single output node. Fig. 17 illustrates some structures used in common practice. We refer to the resulting block as a *transconductance amplifier* and use the symbol of Fig. 17(c) to represent it. This is the basic building block for the scaling operation required in the state variable architecture. Note that its associated transconductance gain parameter g_m can be controlled by biasing (I_Q) as well as by adjusting sizes of amplifier and mirror transistors.

The simplest circuits of Fig. 17(a) and (b) have some drawbacks for accurate applications, especially when used in open-loop integrators. Apart from their reduced linearity, which can be enhanced by using linearized transconductors, they both have low output resistance, because of finite transistor Early voltage. In addition, they cannot simultaneously achieve low systematic offset and large output voltage ranges, because of inherent lack of symmetry between mirror inputs and outputs. A solution to these Early-voltage-related drawbacks is to use some improved current mirror structure. Another possibility is to use a *folded-cascode* structure, such as that represented in Fig. 17(d) for the simplest transconductor case. Interestingly enough, since nodes A and B of Fig. 17(d) remain practically unchanged because of the cascode action performed by transistors biased by V_{B2}, this structure is well suited for extension to multiple inputs, as Fig. 17(e) illustrates. Further improvements for this multiple input case can be achieved by applying local feedback around the A and B terminals, similar to what is done for the mirror of Fig. 16(a).

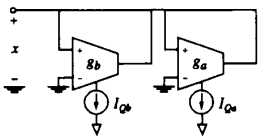


Fig. 18. Chua's diode implementation using saturated transconductance amplifier.

V. PWL GmC CMOS Building Blocks

5.1. Exploitation of Global Differential Amplifier Characteristics

The global transfer characteristics of differential amplifiers can be exploited for approximate PWL synthesis. An example of this possibility corresponds to the Chua's diode decomposition illustrated in Fig. 8. It can be implemented by using the circuit of Fig. 18, consisting of two transconductance amplifiers connected in parallel with transconductance gains $g_a \propto a - b$ and $g_b \propto b$. The former must be designed to saturate at $V_i = \pm E$:

$$E = \sqrt{\frac{2n}{k}\left(\frac{L}{W}\right)_a I_{Qa}} \tag{26a}$$

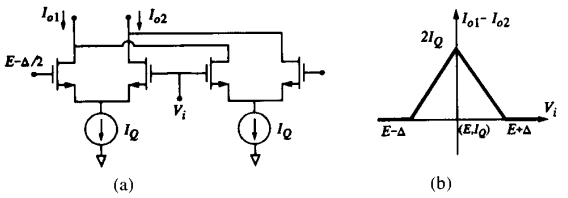
while the latter must be designed to handle the largest possible input voltage range linearly

$$E_{BB} = \sqrt{\frac{2n}{k}\left(\frac{L}{W}\right)_b I_{Qb}} \tag{26b}$$

where E_{BB} denotes power supply voltage. (We assume symmetrical supplies at $\pm E_{BB}$.)

Many different *symmetric* PWL characteristics can be approximately implemented by using a similar approach in *ad hoc* manner. However, systematic function generation based on global differential amplifier characteristics is also possible, using the approach of radial basis functions and the basic building block of Fig. 19(a), similarly to the techniques used in [58], [59]. Assume that both differential amplifiers in this figure are identical, that their characteristics are represented by the first-order model of Fig. 11(a), and that Δ of Fig. 17(a) equals $2F$ of Fig. 11(a). It can be seen that the transfer characteristics of the circuit are as shown in Fig. 17(b)—a PWL radial basis function with interpolation data I_Q. Consequently, this block can be used to support systematic quasi-PWL synthesis,[12] based on the decomposition given in (14). Significant design issues for this approach are mismatch and the handling of large common-mode input voltages. Mismatch originates offsets and, hence, errors at the interpolation points. On the other hand, large common-mode voltages cause transistors to enter in ohmic region, producing distortion in the transconductance gain.

[12] Functions obtained by Fig. 19(a) are softer than PWL because of differential amplifier nonlinearities. However, they are still radial basis functions, and the concept of data interpolation remains valid.



(a) (b)

Fig. 19. (a) Radial basis function implementation via parallel connected differential pairs. (b) First-order transfer characteristic.

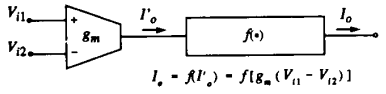
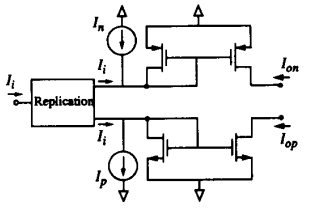


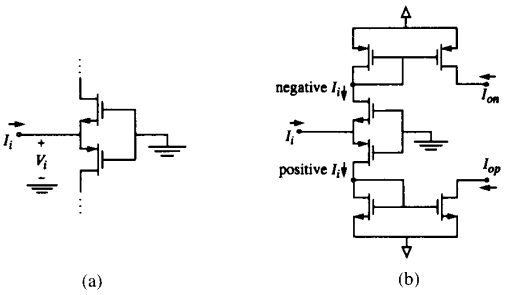
Fig. 20. GmC PWL generation by current shaping.



(a)

(b) (c)

Fig. 21. Current rectification via current mirror cutoff.



(a) (b)

Fig. 22. (a) CMOS current switch. (b) Current rectification via current switching.

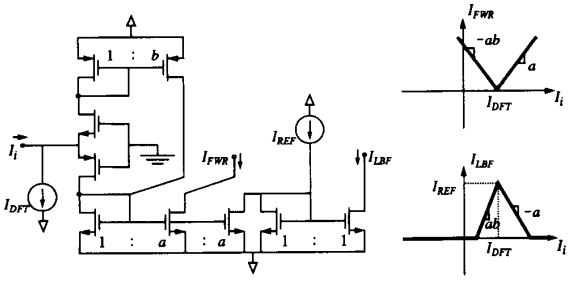


Fig. 23. Full-wave current rectification and linear base function implementation with positive interpolation data via a current switch rectifier.

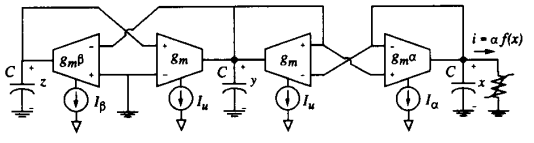


Fig. 24. Conceptual GmC Chua's circuit.

5.2. GmC PWL Generation by Current Shaping

Another approach for GmC PWL function generation consists of generating the nonlinear function in current domain and using a front-end quasi-linear transconductance amplifier [60]. Fig. 20 illustrates this concept.

Let us focus on the current-mode PWL block. It can be approached in a systematic way by using either an extension operator (see (13)) or radial basis functions. The functions $u_p(\cdot)$ and $u_n(\cdot)$ required for an extension operator can be implemented by exploiting inherent mirror rectification as illustrated in Fig. 21. The upper mirror of Fig. 21(a) becomes cutoff for input currents above $-I_n$, yielding $I_{on} = 0$. Otherwise, the net current entering the input device is scaled at the output, yielding $I_{on} = P(I_i + I_n)$. The characteristics of Fig. 21(b) are implemented in this manner. Similar considerations for the bottom mirror of Fig. 21(a) lead to the characteristics of Fig. 21(c).

In Fig. 21(a), the current source to the mirror input devices in the cutoff region produces an accumulation of charge at this node, which may lower the operation speed because this extra charge must be removed when any of the mirrors start conducting again. A *current switch*, shown in Fig. 22(a), can be used for increased current rectification speed [65]. The operation principle is very simple: Any positive input current increases the input voltage, turning the bottom device ON. Since both devices have the same gate voltage, the top device turns OFF. Likewise, the input voltage decreases for negative input currents, so that the top device turns ON and the bottom turns OFF. In sum, positive input currents are drawn to the bottom device, while negative currents are drawn to the top device.

Fig. 22(b) shows a schematic to implement the PWL extension operator functions using a current switch. Because of the intrinsic class AB operation, this structure allows greater operation speed than Fig. 21(a). The current switch rectifier also provides a simple, natural way to implement PWL radial basis functions and the absolute value operator required for canonical PWL multidimensional functions. Corresponding generic schematics are shown in Fig. 23. Output current I_{FWR} constitutes the shifted full-wave rectification of the input current I_i, while I_{LBF} corresponds to a base function for positive interpolation data. Slopes of the base function are given by current mirror gains, while the position and height of the breakpoint are provided by the dc biasing currents I_{DFT} and I_{REF}, respectively. Negative interpolation data are realized by interchanging the functions of up and bottom

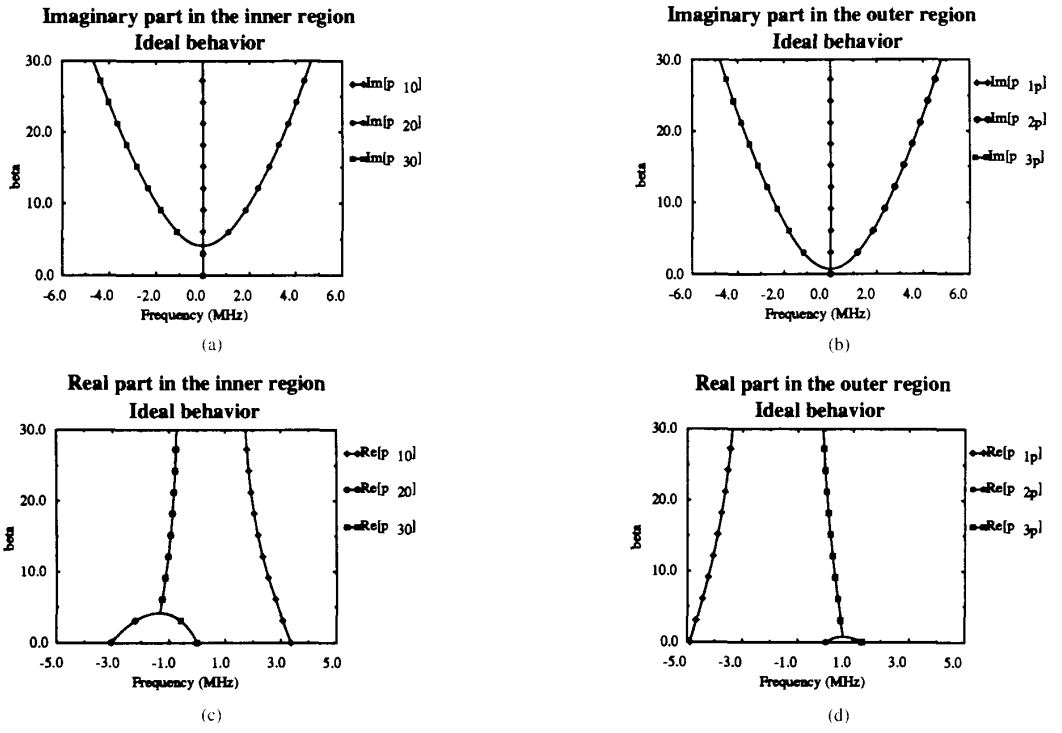


Fig. 25. Ideal pole positions as function of the control parameter β.

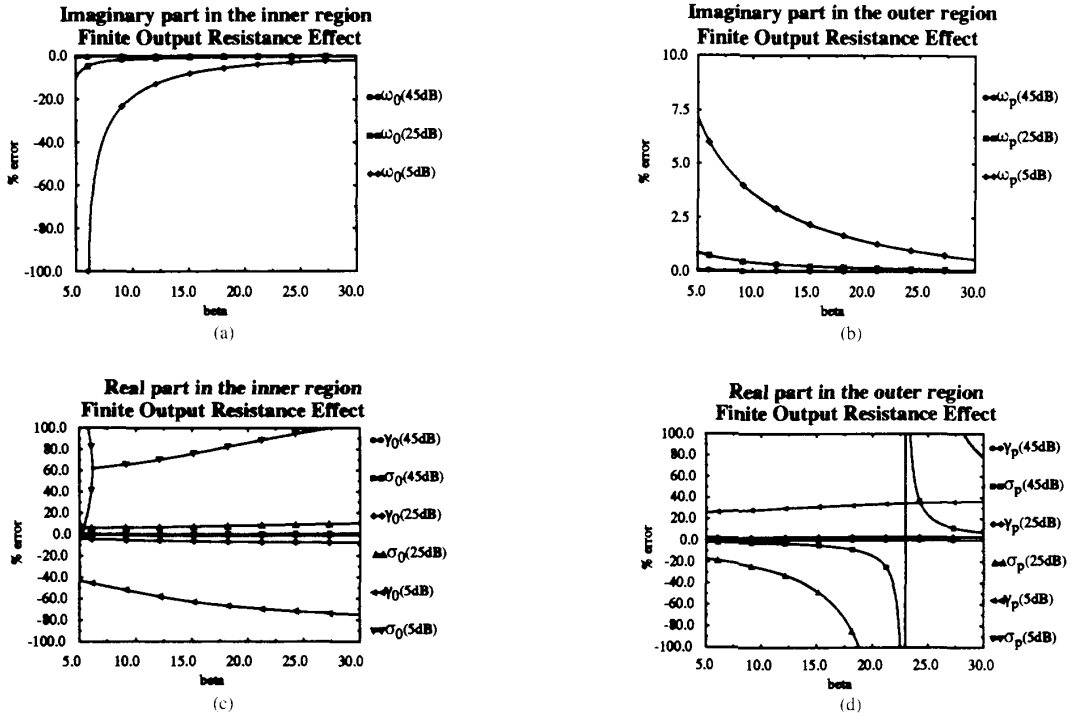


Fig. 26. Paramaterized curves showing the deviations from the ideal behavior when the finite output resistance of the integrators are considered.

transistors in Fig. 23. Due to the integration performed at the input of the current switch, very high resolution and virtually zero current offset are obtained, without relying on precise device matching.

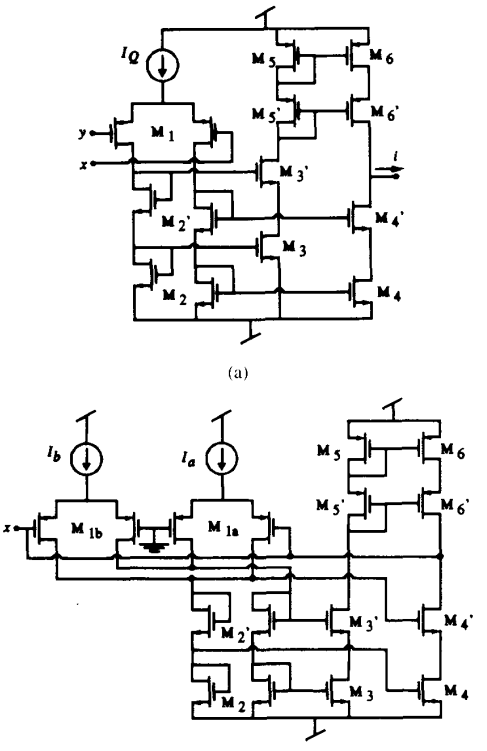


Fig. 27. (a) CMOS schematics for the transconductance amplifiers in the GmC Chua's circuit. (b) CMOS Chua's diode.

VI. A 2.4-μm CMOS Chua's Circuit Prototype

The use of the state-variable methodology and open-loop integrator concepts enables mapping (4) into Fig. 24, consisting of three capacitors, four transconductance amplifiers, and a nonlinear resistor. As explained in Section 5.1, this latter block can be implemented by using the schematic in Fig. 18. Prior to assessing the design of a monolithic prototype at a geometric level, it is important to analyze the effect of the block nonidealities, since it may lead to fundamental limits of the proposed techniques that must be considered for correct performance.

6.1. Effect of Nonidealities

We have intensely analyzed Fig. 24, taking into account both the linear and nonlinear dominant transconductor large-signal nonlinearities, modeling them at the behavioral level, and trying to assess their influence on the operation of the system of equations. These analyses show that the system tolerates transconductor large-signal nonlinearities very well; thus, simple transconductor topologies can be used. Concerning the influence of small-signal parasitics, we have studied displacements of the natural frequencies at the equilibria that are due to transconductor finite output resistance and transconductance gain internal pole. This analysis is crucial, since these eigenvalues determine the system dynamics.

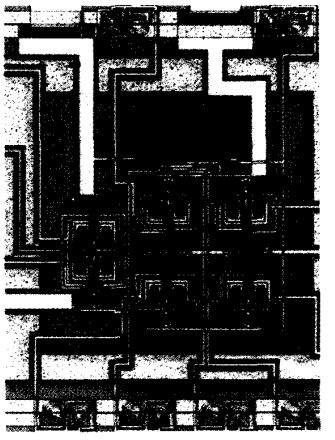


Fig. 28. Microphotograph of the CMOS prototype.

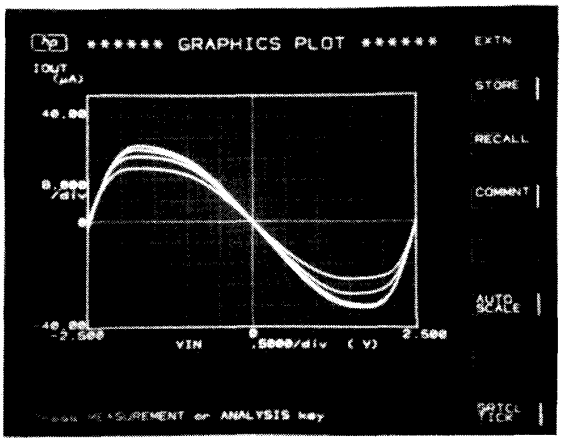


Fig. 29. Experimental family of characteristic curves for the nonlinear resistor.

The following nominal parameter values have been chosen for both analysis and implementation purposes:

$$(\alpha, \beta, a, b) = \left(9, \frac{100}{7}, -\frac{8}{7}, -\frac{5}{7}\right) \tag{27}$$

with all the time constants equal, $\tau_x = \tau_y = \tau_z = C/g_m$, and a nominal C/g_m of 1μs. This set of parameter values corresponds to the well-known *double-scroll* [21] attractor. However, the double-scroll is not an isolated circumstance in the Chua's circuit operation, but rather the final step in a typical period-doubling sequence toward chaos. Assume that β is chosen as the bifurcation sequence control parameter and is controllable via current source I_β in Fig. 24. Calculating the exact range of β values where bifurcation sequence takes place is a difficult task, even for the ideal equation. Instead, following the simple technique proposed in [22], we calculate an extended range that guarantees the existence of bifurcation phenomena. In the ideal case where all transconductance amplifiers have infinite output resistance and no phase error in the transconductance gain, such range is between $\beta = 9$ and 25.

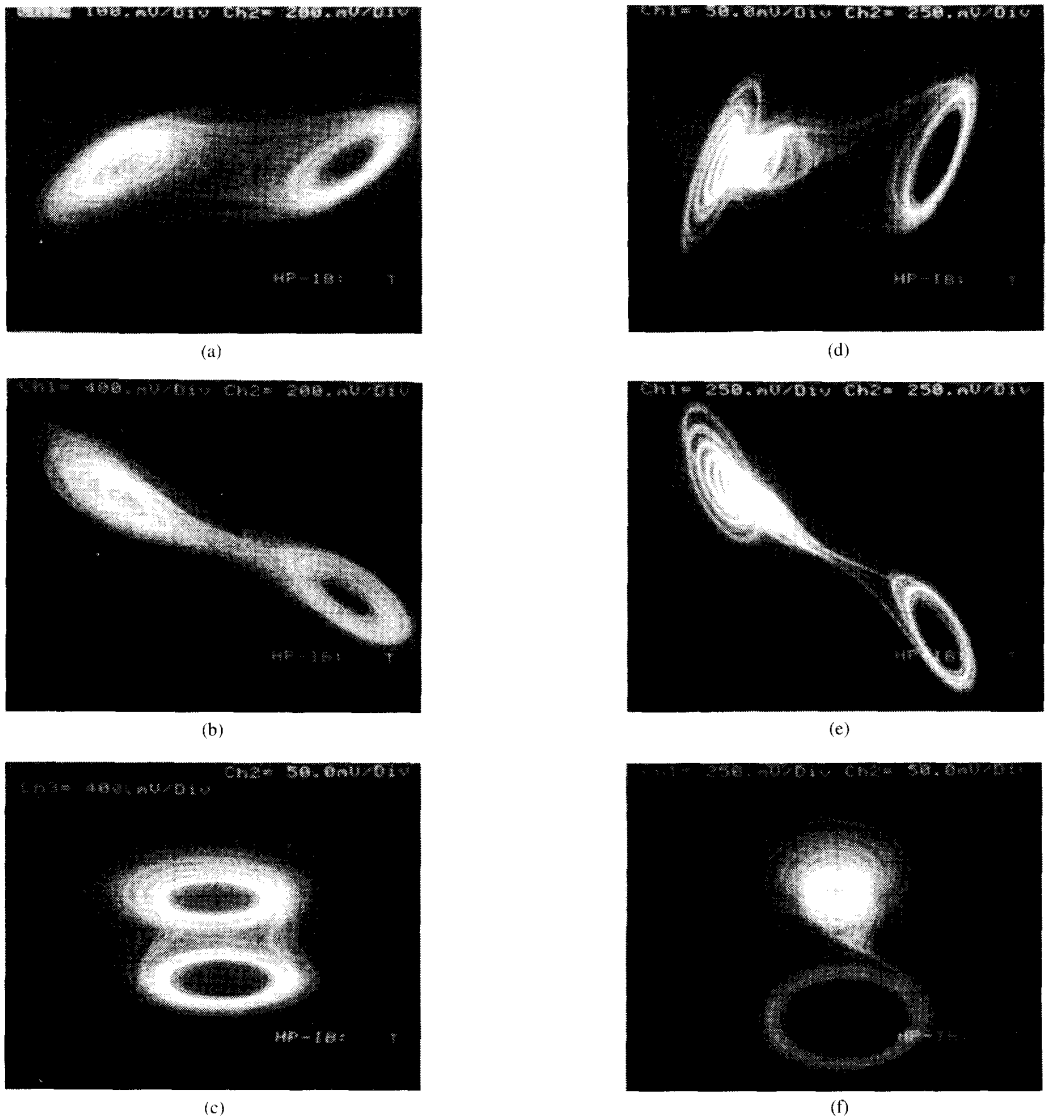


Fig. 30. Measured attractors. Scales are indicated in the pictures where Ch1 refers to the vertical axis and Ch2 refers to the horizontal axis. (a) and (d) are projections onto the (x, y) plane. (b) and (e) are projections onto the (x, z) plane. (c) and (f) are projections onto the (y, z) plane.

Taking into account the fact that nonlinearity of the Chua's circuit is odd-symmetric, only two sets of natural frequencies must be considered:

Inner Region:

$$p_{10} = \gamma_0$$
$$p_{20}, p_{30} = \alpha_0 \pm \omega_0 \tag{28a}$$

Outer Region:

$$p_{1p} = \gamma_p$$
$$p_{2p}, p_{3p} = \sigma_p \pm \omega_p. \tag{28b}$$

Fig. 25 shows the evolution of the natural frequencies (assuming ideal transconductance amplifiers) as a function of the control parameter β. We aim to evaluate displacements of these natural frequencies when integrator nonidealities are considered. Let us first analyze the effect of the transconductance amplifier finite dc gain (equivalently, finite output resistance). Assume all transconductors have equal output resistance. The set of graphics in Fig. 26 display percentage errors in the locations of the natural frequency as compared to the ideal case (infinite output resistance). Three different values of the dc gain are considered: 5, 25, and 45 dB. Note that the most critical parameter is σ_p (Fig. 26(d)) and that errors may be larger than 100% for small output resistance.

Sensitivity analyses show that to maintain σ_p deviation below 1%, the transconductance amplifier dc gain must be larger than 56.7 dB, which is easily achievable with improved transconductor topologies like that in Fig. 17(d). Smaller

values also significantly reduce the bifurcation range for β parameter.

Similar analysis has been done to assess the influence of the integrator nondominant poles, modeling them according to (19). Again, the most critical parameter is σ_p. To maintain deviations in this parameter lower then 1%, the excess phase must be lower than 0.1°. However, unlike finite output resistance, the bifurcation range does not decrease because of transconductance gain phase lag; on the contrary, it increases slightly. Thus, the attractor is not destroyed because of the influence of nondominant poles; only the qualitative behavior of the attractor is altered.

6.2. Design and Layout

Fig. 27(a) shows the schematics used for the transconductor amplifiers, and Fig. 27(b) corresponds to the nonlinear resistor. Note that the latter has been simplified with respect to the concept shown in Fig. 18, making both differential pairs share the same output stage, which yields higher output resistance. Unity gain current mirrors were chosen to simplify design. Bias currents, as well as transistor widths, were calculated by using a proprietary analog cell optimization tool [78] according to the system requirements. We included equations for the dispersion of the random technological parameters, according to the formulation in [28], [29], and used them to minimize offset during the optimization process. Fig. 28 shows a microphotograph of the fabricated prototype with an area of 0.35 mm^2. Total power consumption was 1.6 mW for ±2.5-V biasing.

Fig. 29 shows a family of characteristics curves for the nonlinear resistor, measured for different values of I_a. Offset for these characteristics was 3 mV. The outer pieces correspond to voltage saturation of the current mirrors and are not exploited for the circuit operation, since they have little influence on the shape of the attractor. Fig. 30 shows a gallery of views of different attractors obtained from the prototype. Fig. 30 (a)–(c) constitute the projections onto the coordinate planes of the well-known Chua's double scroll. However, note that the double scroll shows one lobe denser than the other. This asymmetry is due to both the difference in magnitude of the breakpoints and the deviations on the outer slopes of the Chua's diode characteristic, which imply differences in the natural frequencies of the global circuit. However, this does not modify the qualitative behavior of the attractor; rather, it confirms the tolerance of the Chua's diode characteristic to deviations from the ideal piecewise-linear model. Fig. 30 (d)–(f) show the measured attractor from the same prototype for an increased value of I_a, which implies greater deviations on the outer slopes. Note that the left lobe in Fig. 30(d) changes with respect to the double-scroll attractor (Fig. 30(a)) in the sense that the trajectory diverges to the other scroll via a spiral.

VII. Conclusions

Summarizing, this paper has presented a systematic approach for CMOS design of PWL dynamic systems using state variable techniques. We have surveyed most significant circuit-level issues for GmC design technique, with the exception of time constant *tuning*. For this very important issue, the reader is referred to [53], [79]–[81]. We have also presented the first reported monolithic implementation of an intentionally chaotic continuous-time circuit, inspired by the Chua's circuit. Taking into account recent developments in nonlinear signal processing and neural computation, monolithic chaotic circuits, like those designed following techniques reported here, may become basic building blocks for future VLSI communication and advanced computational systems.

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