Electrical-level synthesis of pipeline ADCs

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Abstract – **This paper presents a design tool for the synthesis of pipeline ADCs which is able to optimally map high-level converter specifications, such as the required effective resolution, onto electrical-level parameters, i.e., transistor sizes and biasing conditions. It is based on the combination of a behavioural simulator for performance evaluation, accurate models of the converter components, and an optimization algorithm to minimize the power and area consumption of the circuit solution. The design procedure is herein demonstrated with the complete design of a 0.13μm CMOS 10bits@60MS/s pipeline ADC, which only consumes 11.3mW from a 1.2V supply voltage. A close agreement between behavioural- and electrical-level simulations is obtained with only 0.2bit deviation on the measured *ENOB*.**

I. Introduction

Conventional design methodologies for the synthesis of pipeline Analog-to-Digital Converters (ADCs) use a two-step *top-down* strategy. In a first system-level step, converter specifications are mapped onto requirements of the building blocks, e.g. amplifiers, comparators and switches [1]-[5]. Then, in a second electrical-level step, the transistor sizes and biasing conditions of such blocks are calculated. Design targets during this latter step are commonly expressed in terms of open-loop specifications, such as the DC gain, gain-bandwidth product or phase margin of amplifiers.

This design procedure suffers from two main shortcomings: 1) parasitic capacitances are only roughly estimated during system-level design and, therefore, derived open-loop specs are affected by a large uncertainty; and 2) open loop specs does not guarantee achieving the targeted performance when the feedback loops around the amplifiers are closed. Hence, in practice, the above synthesis process must be refined by time-consuming *bottom-up* iterative simulation loops until the high-level specifications are met or a sub-optimum solution with oversized building blocks is assumed.

To overcome these drawbacks, a novel simulation-based synthesis tool for pipeline ADCs is herein presented. It directly maps high-level converter specifications onto electrical-level parameters. Hence, there is no need for costly bottom-up electrical simulations. A simulated-annealing based optimization algorithm using an event-driven behavioural simulator for performance evaluation defines the core of the synthesis tool. The simulator includes highly-accurate models for the noise and settling performance of the building blocks, accounting both small- and large signal effects. Design targets for these blocks are expressed in terms of high-level requirements (*SNDR*, *ENOB*,...) instead of open-loop specifications. The tool, developed in the MATLAB®-Simulink® framework, also includes routines for the estimation of parasitic capacitances and transistor sizes, as well as, for the evaluation of area/power consumptions.

The paper is organized as follows. Section II briefly describes the proposed behavioural simulator for pipelined ADCs. Next, Section III illustrates the synthesis procedure and explains how the behavioural simulator, models of the building blocks and optimization algorithm are combined to map high-level converter specifications onto electrical-level realizations. As a demonstration of the technique, Section IV presents the complete design of a 10bits@60MS/s pipelined ADC in a 0.13μm CMOS technology, and illustrates the close agreement between behavioural- and electrical-level simulations. Finally, Section V concludes the paper.

II. Behavioural simulator of pipelined ADCs

Fig.1 shows the generic diagram of a pipelined ADC, consisting of an arbitrary cascade of k stages and a Sampled-and-Hold (S/H) circuit at the front. Each stage resolves partial code words of length n_j, $j = 1, \ldots, k$, which are all re-ordered and combined at the digital correction block to obtain the N bit output of the converter. As illustrated in Fig.1(b), the inner structure of a pipelined stage comprises four blocks: a flash ADC with $N_j \le 2^{n_j}$ output codes, a Digital-to-Analog Converter (DAC) with N_j output levels, a substractor, and a S/H residue amplifier with gain G_j. The blocks within the shaded area of Fig.1(b) are implemented in practice by a single subcir-

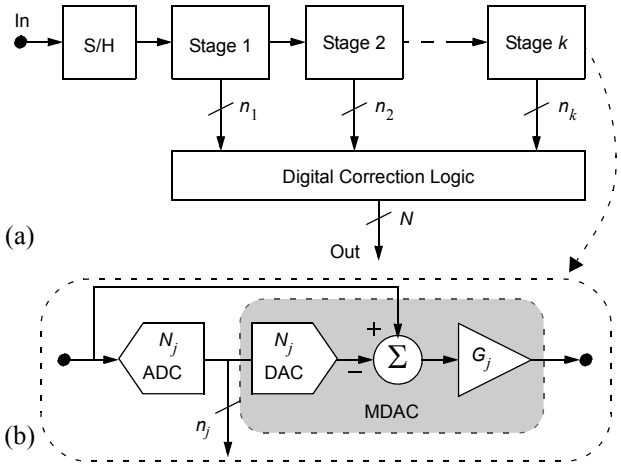

Figure 1. Generic pipeline ADC architecture. (a) Conceptual block diagram; (b) Single stage.

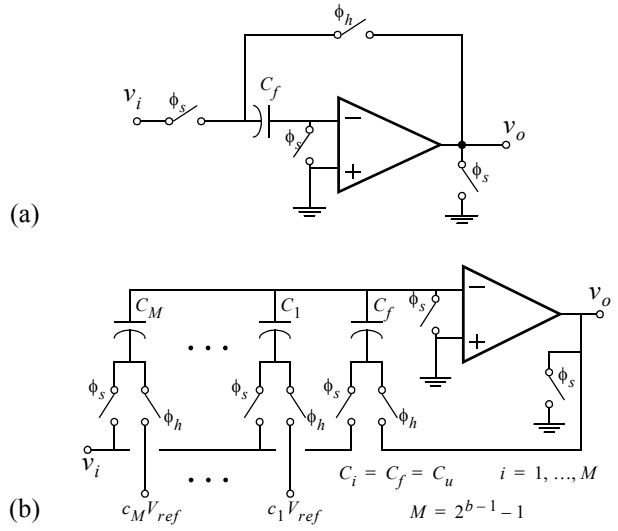

Figure 2. (a) S/H and (b) b-bits MDAC schematics.

cuit which is referred to as Multiplying DAC (MDAC). Typical circuit-level schematics for the S/H and MDAC are shown in Fig.2(a) and Fig.2(b), respectively.

An event-driven behavioural simulator for pipelined converters, including accurate models for the aforementioned blocks, has been developed. Special attention has been paid on the settling performance modelling of the S/H and MDAC blocks [6]. Such models not only accounts for small-signal effects, but other important large-signal phenomena, namely: 1) the jumps of the initial conditions caused by charge redistribution between consecutive clock phases; 2) the limitations of internal currents due to transistor non-linearities; 3) the impact of the change of the DC gain of amplifiers with the signal level. This latter effect induces movements on the poles and zeros of the system and, hence, variations on the small signal parameters. Besides, models have been developed under actual closed loop conditions, so that there is no need to emulate the impact of the driving and feedback capacitors onto equivalent loading values, as it is done in open-loop configurations. In addition, the modelling effort has not only focused in single-stage amplifier topologies, but also on two-stage compensated structures, more suitable under low-voltage operation conditions. Besides S/H and MDAC blocks, we have also developed accurate behavioural models for the flash sub-ADCs accounting for offset, hysteresis and mismatching errors.

In order to reduce the computational cost of the behavioural simulator, all the models have been coded and compiled in C language and embedded in MATLAB®-Simulink® libraries. This approach allows to create arbitrary pipelined architectures by simply interconnecting the parameterized blocks available in the libraries, as shown in Fig. 3. Together with the building blocks already mentioned, e.g., S/H, MDAC and flash sub-ADC, these libraries also include other specific instances to support time-interleaved architectures, such as demultiplexers, multiplexers and input-sources with jitter noise and gain errors.

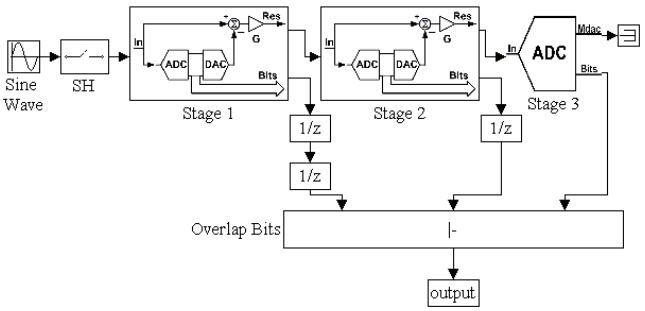

Figure 3. Building a 3-stage pipelined ADC in the proposed tool.

Additionally, the libraries also incorporate models to support dynamic power-saving strategies, such as the opamp sharing technique [7].

III. Synthesis procedure

The objective of the proposed synthesis procedure for pipeline ADCs is to optimally map high-level converter specifications onto electrical-level parameters of its building blocks, with the minimum power consumption and silicon area.

Fig. 4 shows the basic flow diagram of the procedure. It implements a simulation-based strategy which uses an optimization algorithm to explore the design space and a performance evaluator to quantify the ADC at each iteration in terms of a user-defined cost function. Our synthesis tool uses as evaluator the behavioural simulator described in Sec. II, and as exploration algorithm a simulated annealing based optimizer [8].

Basic running variables in the optimization loop of Fig. 4 are the unitary capacitances (C_u), overdrive voltages of transistors (v_{dsat}) and amplifier time constants (τ_u). They represent the variables of the pipeline converter design space. At each iteration of the optimization procedure, their values are used by a set of internal processing routines to estimate parasitic capacitances and electrical-level parameters (transistor sizes and biasing conditions), as well as, the area and power

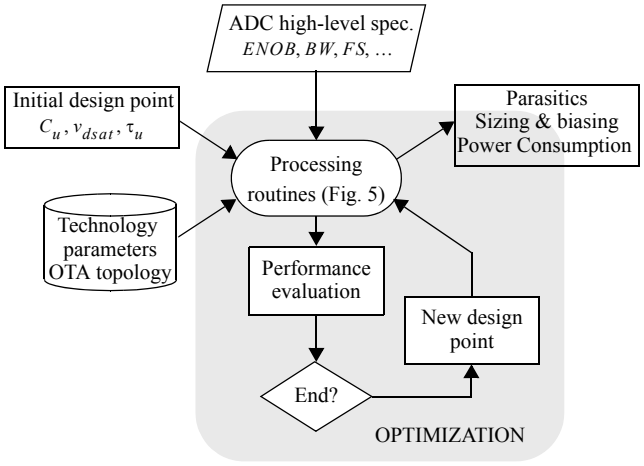

Figure 4. Basic diagram block of the synthesis procedure.

consumption of the converter instance. Then, the performance of such instance is evaluated by means of a behavioural simulation and, according to the results, a new movement in the design space is generated. In order to avoid local minima, the exploration of the design space is divided into a coarse phase, based in simulated annealing, and a fine phase which uses deterministic techniques to let the final solution.

Fig. 5 shows the flow diagram of the operations carried out at the processing block of Fig. 4. Using the values of the design space variables, inherited from the main optimization loop, as well as, parameters from the technological process, a first estimation of the OTA parasitics is guessed. These values, together with the required resolution-per-stage, are then used to size switches and compute the required dc gain of the OTAs. Afterwards, using these gain values and the position in the design space, OTAs are fully dimensioned [6]. At this point, parasitic capacitances can be realistically evaluated and compared to the previously estimated values. If discrepancies are higher than a user-defined tolerance value, δ, the iterative process is repeated again until convergence is reached. In spite of the apparently cumbersome procedure, these routines only take three or four iterations to converge.

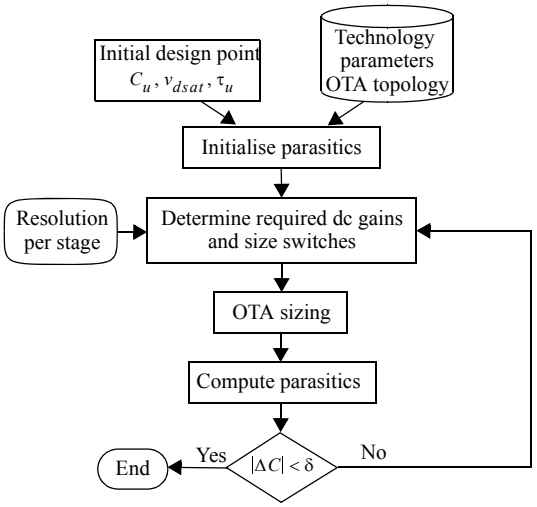

Figure 5. Matlab routines procedure in detail.

IV. Synthesis of a 10bits@60ms/s ADC.

Using the synthesis procedure described above, the design of a 10bits@60MS/s ADC in a 0.13µm CMOS technology is carried out. Design specifications are 9.5 effective bits of resolution for a 0.8Vpp input range, assuming 1.2V supply. The target pipelined architecture consists of 7 stages, the two first stages have 3 output bits whereas the remaining stages have 2 output bits. Due to the reduced supply voltage, a two-stage Miller-compensated amplifier topology, shown in Fig. 6, is considered for the realization of the S/H and MDACs.

The synthesis procedure takes about 20 minutes of CPU time and 600 iterations (using a 1.7GHz@1GB RAM computer). Results are summarized in Table I and include both esti-

Table I. Synthesis results

	Parameters	S/H		MDAC1		MDAC2		MDAC3		MDAC 4-6	
		Estimated	Electrical	Estimated	Electrical	Estimated	Electrical	Estimated	Electrical	Estimated	Electrical
OTAs	$W_{1,2}/L_{1,2}$ (µm/µm)	72/0.3	75/0.3	131/0.3	140/0.3	59/0.3	60/0.3	31/0.3	32/0.3	30/0.3	32/0.3
	$W_{3,4}/L_{3,4}$ (µm/µm)	72/0.3	75/0.3	131/0.3	140/0.3	59/03	60/0.3	31/0.3	32/0.3	30/0.3	32/0.3
	W_5/L_5 (µm/µm)	79/0.2	90/0.2	261/0.3	290/0.3	65/0.2	65/0.2	35/0.2	35/0.2	34/0.2	35/0.2
	$W_{6,7}/L_{6,7}$ (µm/µm)	8/0.2	6/0.2	25/0.3	22/0.3	7/0.2	4/0.2	4/0.2	2/0.2	4/0.2	2/0.2
	$W_{8,9}/L_{8,9}$ (µm/µm)	8/0.2	6/0.2	25/0.3	22/0.3	7/0.2	4/0.2	4/0.2	2/0.2	4/0.2	2/0.2
	$W_{12,13}/L_{12,13}$ (µm/µm)	246/0.2	240/0.2	453/0.3	460/0.3	120/0.2	104/0.2	84/0.2	75/0.2	74/0.2	75/0.2
	$W_{14,15}/L_{14,15}$ (µm/µm)	47/0.2	44/0.2	87/0.3	87/0.3	23/0.2	23/0.2	16/0.2	16/0.2	15/0.2	16/0.2
	W_{18}/L_{18} (µm/µm)	93/0.2	93/0.2	173/0.3	145/0.3	46/0.2	35/0.2	32/0.2	26/0.2	29/0.2	26/0.2
	DC-gain	1821	2266	6842	7300	3103	3379	3050	2700	3050	2693
	Output swing (V)	-0.2/0.2	-0.33/0.47	-0.2/0.2	-0.35/0.43	-0.2/0.2	-0.35/0.44	-0.2/0.2	-0.35/0.45	-0.2/0.2	-0.35/0.45
	Overdrive volt. (mV)	125	125	100	100	100	100	100	100	100	100
	Compensation cap. (pF)	3.06	3.05	0.8	0.8	0.35	0.35	0.45	0.45	0.4	0.4
	Eq. input noise (nV/√Hz)	3.75	4.33	3.46	3.47	5.08	5.54	7	7.9	7.12	7.93
	GBW (MHz)	131	128	617	589	582	559	254	239	273	270
	PM (degrees)	63	60	12	5	9	5	20	17	16	16
	Power consump. (mW)	3.5	3.5	2.2	2.3	1.0	1.1	0.7	0.71	0.6	0.71
Switch	$r_{on,\phi_s}/r_{on,\phi_h}$ (kΩ)	0.1/0.1	0.1/0.1	0.55/0.55	0.55/0.55	1/1	1/1	0.65/1	1/1	1/1	1/1
Cap.	Unitary capacitor (pF)	2.25	2.25	0.35	0.35	0.1	0.1	0.15	0.15	0.1	0.1

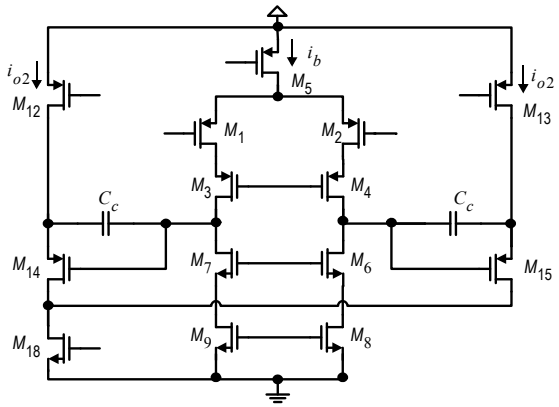

Figure 6. OTA topology used in each stage.

mated values from the synthesis tool and measures from electrical-level simulations. In this latter case, transistor dimensions have been manually adjusted to guarantee that pMOS and nMOS transistors carry the same currents through the amplifier branches and, thereby, avoid systematic offset errors. As can be seen, sizing deviations rarely exceed 10%.

Fig.7 compares the power spectra of the ADC for a full-scale input tone at 28MHz obtained both from electrical and behavioural simulations. Note that there is a close agreement between both spectra with only 0.2bits deviation in the effective number of bits.

Fig.8 shows the Integrated-Non-Linearity (*INL*) of the ADC evaluated both from electrical and behavioural simulations [9]. Also in this case the agreement is excellent and an *INL* nonlinearity lower than ±0.5 LSB (Least-Significant-Bit (LSB) is predicted.

The converter performance is summarized in Table II.

V. Conclusions.

A simulation-based synthesis tool for the design of pipeline ADCs has been presented. It is based on the combination of an accurate behavioural simulator, a simulated-annealing optimizer and a set of auxiliary routines for estimating transistor sizes, parasitics and area/power consumption. The proposed tool is able to synthesize pipeline ADCs in very short design times, in the order of minutes, while obtaining an excellent agreement between behavioural- and electrical-level simulations, with only 0.2bit deviation on the measured *ENOB*.

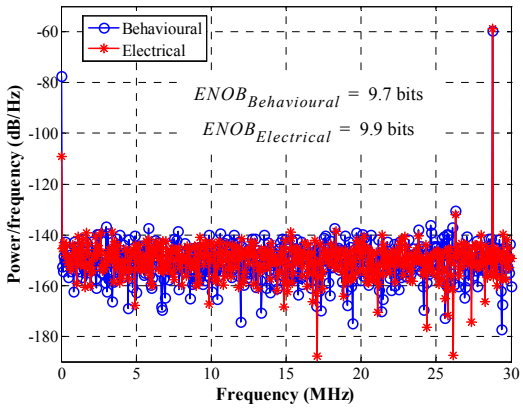

Figure 7. Comparison between electrical- and behavioural simulations.

Table II. Performance summary of the ADC

Technology	0.13 µm
Voltage supply	1.2 V
Resolution	10 bits
Conversion rate	60 MSPS
Input range	0.8 Vpp differential
ENOB @ Nyquist	9.5 bits
SFDR @ Nyquist	73 dB
INL@ 10 bits	< 0.5 LSB
Power consumption[a]	11.3 mW

a.Including SH, MDACs and flash sub-ADCs.

Acknowledgments

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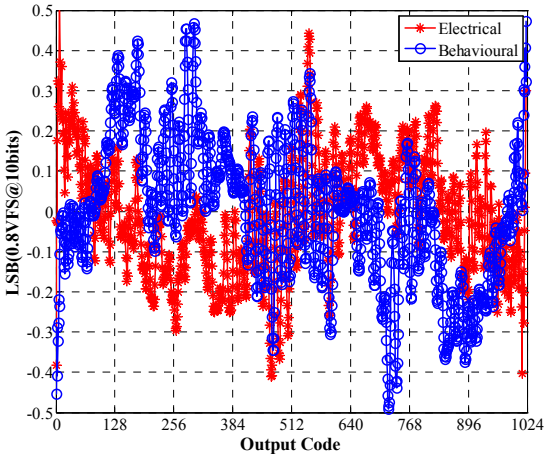

Figure 8. INL measurement (3023 samples/ 101 cycles)