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Expandible High-order Cascade ΣΔ Modulator with Constant, Reduced Systematic Loss of Resolution

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Abstract *- An arbitrary order sigma-delta modulator cascade architecture is presented with only 1-bit loss of resolution due to scaling issues, even with single-bit quantization. This loss is kept with a high overloading point, regardless of the order. Simulations reveal that circuit imperfections can be tolerated up to 6th order, so that 90-dB SNDR can be obtained with x16 oversampling, without multi-bit quantization.*

I. INTRODUCTION

The increasing demand for broadband access to the internet has stimulated the industrial interest in high-performance A/D converters able to achieve between 12- and 16-bit accuracy for signal bandwidths exceeding 1MHz [1]. These specifications seem a priori better suited for pipeline architectures. However the larger linearity and simpler circuitry of oversampled, sigma-delta modulator (ΣΔM) converters render them worth exploring for the implementation of wireline modems as mixed-signal systems on-chip. This is only feasible if ΣΔM architectures are devised capable to feature those resolution levels with low values of the oversampling ratio M. This involves either increasing the modulator order or using multi-bit quantization, or a combination of both. Among the alternatives explored, many designers have focused on cascade architectures (including single-bit or multi-bit quantization) to provide up to 6th-order, low oversampling ratio A/D conversion over the xDSL band [2]-[6].

Two considerations are important for fully exploiting the potential of cascade ΣΔMs. On the one hand, signals in the cascade must be properly scaled to prevent a premature overload of the modulator stages. Digitally compensating such scale factors causes a systematic loss of resolution. The larger the number of stages, the more evident the overloading problem becomes, so that the systematic loss increases with the modulator order. On the other hand, the integrator finite DC-gain and the weight mismatches impact cascade architectures, causing imperfect cancellation of the low-order quantization error produced by the first stages.

In this paper the order of the cascade ΣΔM is extended arbitrarily while the systematic loss of resolution is not increased. A 2-1-...-1 cascade together with a set of integrator weights and a simple cancellation logic are proposed to reduce the systematic loss to 1bit, regardless of the order and without changing the overloading point. We show that the degradation due to circuit imperfections can be tolerated up to 6th order for an oversampling ratio of 16, which makes it possible to obtain 15-bit resolution in the ADSL band and without multi-bit quantization.

II. MODULATOR ARCHITECTURE

Fig.1 shows an Lth-order cascade architecture consisting of $L-1$ stages: a second-order ΣΔM, acting as a first stage, and $L-2$ identical first-order stages. All quantizers are also identical comparators. The cancellation logic is also easily expandible, requiring just right shifters and delay blocks. The key to run this architecture, and what makes it advantageous with respect to other high-order cascades, is the integrator weight selection. It has been made according to the following criteria:

(a) ideally, the quantization error generated by all stages other than the last one must be removed by the cancellation logic;
(b) the modulator must preserve a high overloading point;
(c) the output swing needed in integrators must be physically achievable according to the supply voltage;
(d) the number of branches required for each integrator and the total number of unitary capacitors should be minimized.

Combining behavioural simulation and statistical optimization we obtain:

$$g_0 = g_0' = 0.25 \qquad g_1 = 1, g_1' = 0.5$$
$$g_k = 1, g_k' = 0.5, g_k'' = 0.5 \qquad k = 2, \ldots, L-1 \tag{1}$$

which, under ideal conditions, leads to the following z-domain output,

$$Y(z) = X(z)z^{-L} + 2(1-z^{-1})^L E_{L-1}(z) \tag{2}$$

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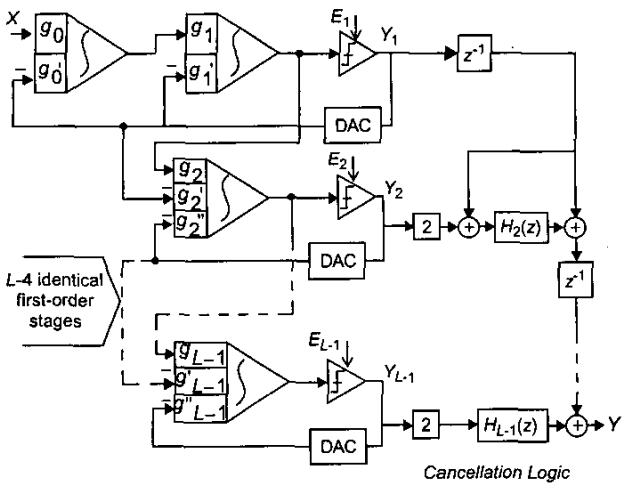

Fig. 1. Lth-order 2-1^{L-2} ΣΔM. $H_k(z)=(1-z^{-1})^k$, $k = 2 \ldots L-1$

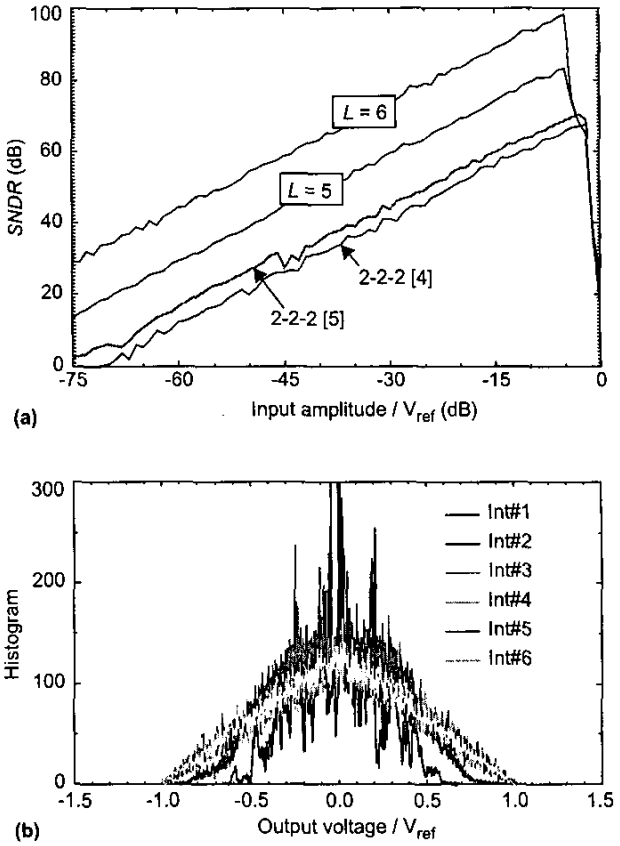

Fig. 2. (a) *SNDR* vs. input level under ideal conditions. (b) Histograms of the integrator outputs relative to the reference voltage.

where $E_{L-1}(z)$ stands for the last-stage quantization error. Note that its transfer function contains an amplifying factor of 2, which means a systematic loss of only 1bit, or 6dB signal-to-(noise + distortion) ratio (*SNDR*), with respect to an ideal Lth-order ΣΔM. This loss is considerably smaller than the systematic loss in other cascade architectures and does not increase with the modulator order. Neither the overloading point (−5dB below full scale) is modified by the increasing order. To illustrate this, Fig.2(a) shows the *SNDR* vs. input level for two versions of a 6th-order 2-2-2 cascade [4] [5], and the one in this paper with $L = 5$ and 6. Note that even with $L = 5$ the *SNDR* is improved with respect to the 6th-order 2-2-2 cascades.

Returning to the proposed coefficients, note that the largest weight of each 3-weight integrator ($k = 2, \ldots, L-1$) can be obtained as the summation of the others, so that no 3-branch SC integrators are required. This also minimizes the number of unitary capacitors to $2(4L+1)$ in a fully-differential implementation.

Finally, the total output swing required in all integrators equals the quantizer full-scale. This interesting feature for implementation in low-voltage technologies is illustrated in Fig.2(b) for the case $L = 6$.

III. CIRCUIT IMPERFECTIONS

Apart from other circuit imperfections whose impact is, to a first order, independent of L, integrator weight mismatch and finite DC-gain produce incomplete cancellation of the quantization noise induced in the first stages, which may mask the ideal one, thus imposing an upper bound to the feasible values of L. In order to estimate this limit under realistic circuit imperfections, Fig.3(a) shows the simulated half-scale *SNDR* as a function of the amplifier DC-gain for $M = 16$. Fig.3(b) shows the *SNDR* histograms obtained from MonteCarlo simulation assuming 0.1% sigma in capacitor ratios (0.05% is currently featured by MiM capacitors in standard CMOS processes [7]).

Under these conditions, mainly because of the matching sensitivity, the 7th-order architecture is not worth implementing. Nevertheless, the 6th-order modulator provides 90-dB worst-case *SNDR* with DC-gain of 2500. Especially robust is the 5th-order cascade requiring a DC-gain of 1000 to achieve 80-dB worst-case *SNDR* with $M = 16$. The required DC-gains are smaller for the remaining $L-2$ stages of the cascade, down to 500, which allows us to use simpler circuits and layouts for these otherwise identical stages.

As a concluding remark, note that since most degradations are due to imperfect cancellation of the first-stage quantization error, orders larger than $L = 7$ become feasible by applying the on-line digital correction strategy in [8].

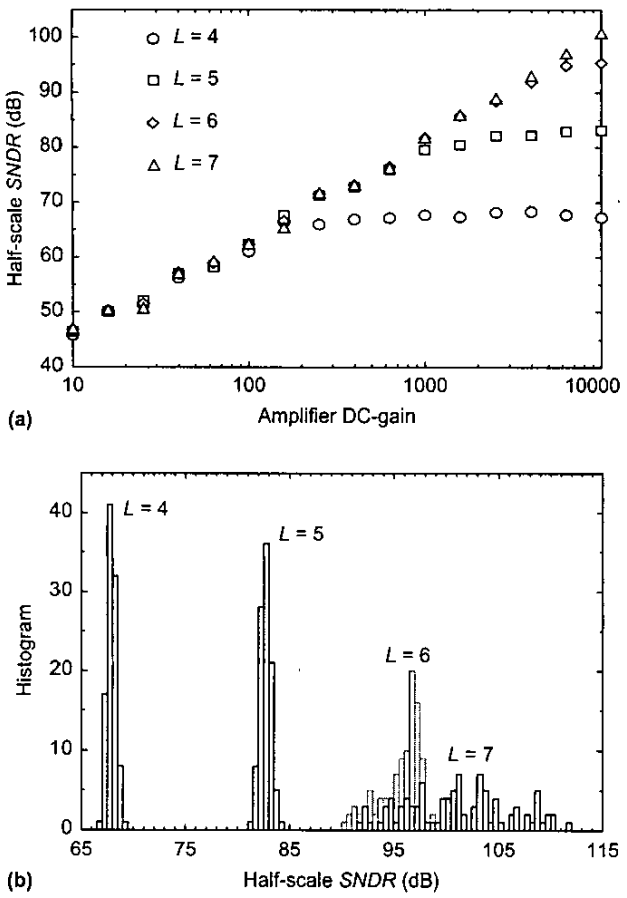

Fig. 3. Effect of (a) finite DC-gain and (b) weight mismatch on *SNDR* for $M = 16$.

ACKNOWLEDGMENT

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